MATHEMATICS

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1960

SovietRxiv

Abstract

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MATHEMATICS

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ON CIRCUITS OF A ONE-DIGIT ADDER

(Presented by Academician M. V. Keldysh, July 1, 1960)

0°. Let b, c, and e be three one-digit binary numbers corresponding to the two digits of some order of the addends and to the carry digit into this order from the adjacent lower one.

The circuits under consideration are built from the logical elements "and" ($\wedge$), "or" ($\vee$), and "not" ($\ominus$), and, from b, c, and e, produce the carry E into the next higher order and the sum B modulo 2 of the quantities b, c, e. The negation operation is allowed to be applied no more than once. The circuits are assumed not to contain cycles, i.e., closed paths beginning and ending at the same element. This makes it possible to consider that there is a one-to-one correspondence between circuits realizing a function F and formulas for F containing the indicated logical operations and parentheses.

This note solves the question: under these conditions, what is the minimal number of diodes required in an adder circuit, and what are these most economical circuits ([1])?

Notation: the vector (b, c, e) is called unitary if exactly one of the quantities b, c, e is equal to 1, and binary if exactly two of them are equal to 1. In formulas the sign $\wedge$ is omitted, the sign $\vee$ is replaced by the sign $+$, and the result of applying the negation operation to a function F is denoted by F'.

In items 1°–3° the circuits are assumed to be optimal and to contain only the elements $\vee$ and $\wedge$.

1°. The circuit contains no identity functions: the function $\alpha \equiv 0$ need not be fed to the input of an element $\vee$, and the element $\wedge$ itself, having an input $\alpha \equiv 0$, is not needed in the circuit. The analogous assertion is also true for $\alpha \equiv 1$.

2°. Let all lines beginning at the function α pass through the element $\vee_\alpha$. If, in addition, α is an input of the element $\vee_\alpha$, then α is not an input of any other element (i.e., there are no a priori possible lines drawn in Fig. 1a by dotted lines). Indeed, feeding, along the dotted lines, instead of α, the function $\alpha_1 \equiv 0$ can reduce the other inputs of $\vee_\alpha$ only on vectors where $\alpha = 1$. The input α itself will remain unchanged (because of the absence of cycles in the circuit),

Fig. 1

Figure 1: Fig. 1

and therefore $\vee_\alpha$ will produce the previous result, but identity functions will appear in the circuit, contrary to 1°.

3°. Let the function f be taken from the output of the element $\vee_f$, having two inputs, which in turn are the outputs of certain elements (these latter will obviously be elements $\wedge$) $\wedge_1$ and $\wedge_2$. Let the function α enter the inputs of $\wedge_1$ and $\wedge_2$. Then each of $\wedge_1$ and $\wedge_2$ has at least three inputs.

Indeed, the circuits in Figs. 1 and 1 give one and the same result, but when $m = 1$ the circuit in Fig. 1 is more economical by at least one diode (the need for the logical multiplication $\beta_1 \cdots \beta_m$ disappears).

Let us return to adder circuits. The function B, by virtue of its nonmonotonicity in b, c, e, cannot be obtained from them with the aid of only one ···

of the monotone operations $\vee$ and $\wedge$, and for its realization requires an inverter.

4°. In any (possibly nonoptimal) circuit for obtaining B, the function E is fed to the input of the inverter. Indeed, the circuit contains one inverter, and therefore

$$B = Fx' + G,$$

where the functions F, G, x are monotone. The functions F and x' take the value 1 on any unary vector (otherwise $G = 1$ on some unary vector, and hence on some binary vector, and then on this latter vector $B = 1$).

Fig. 1.

The monotone F is equal to 1 on all binary vectors, and therefore on them $x' = 0$. From the monotonicity of x it follows that $x \equiv E$, as was required to prove. It is easy to see that

$$B = (b + c + e)E' + bce.$$

Thus, the function E must be obtained before the inverter.

5°. The circuit for obtaining E, used in the NAREC machine and containing 8 diodes (see Fig. 2), is the unique optimal one (up to permutations of b, c, and e, and replacement of $\vee$ by $\wedge$, $\wedge$ by $\vee$).

Indeed, the self-duality* of E allows us to assume that E is obtained at the output of the element $\vee_E$. The inputs of $\vee_E$ cannot be the variables b, c, or e, since $E = 0$ on any unary vector. Consequently, each of the inputs of $\vee_E$ requires at least two diodes for its formation, and therefore there cannot be more than two such inputs, since already for three inputs one needs at least

$3 \cdot 2 + 3 = 9 > 8$ diodes. But at least one of the two inputs of $\vee_E$ (call it α) must take the value one on two binary vectors. To form α, both elements $\vee$ and elements $\wedge$ are necessary, since the use of only $\vee$' s gives $\alpha > b$, which, as we have seen, is impossible, while the use of only $\wedge$' s cannot give a function equal to 1 on more than one binary vector. Taking into account 2° and 3°, we obtain that the only possible circuit is that of Fig. 2, where the original quantities themselves are fed to inputs 1–5. We may assume that b is fed to input 1, and c to input 2. But input 3 then becomes zero on $(1,0,0)$ and $(0,1,0)$, i.e. is equal to e. The function β must take the value one on $(1,1,0)$; consequently, b is fed to input 4, c is fed to input 5, and the resulting circuit repeats the NAREC circuit.

We proceed to the construction of the function B, bearing in mind the limit of 16 diodes (see the NAREC circuit in Fig. 4b). We shall consider only the lines that leave

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* The function $\Phi(b,c,e)$ is called self-dual if $\Phi(b',c',e') = \Phi'(b,c,e)$.

from the inverter, and the elements (under our limit there can be no more than four of them) through which these lines pass.

Here two cases are possible (which lead to two essentially different circuits with 16 diodes):

A. Two lines leave some element (including the inverter). According to 2° and 3°, they go directly from the inverter, and all four elements allowed by the limit are used; the only possible circuit is Fig. 3a, where inputs $1, 2, 3$ have already been formed in obtaining E.* We write out our stock (taking into account the possible replacement in the circuit for E of signs: $\vee$ by $\wedge$; $\wedge$ by $\vee$):

$$b,\ c,\ e,\ bc,\ bc+e,\ b+c,\ (b+c)e,\ E.$$

Let B be taken from the output $\vee_B$. Then the arrangement of signs must be as in Fig. 3a. Each of the functions in our stock becomes zero on at least one unit vector. The same is true for input β. If input 1 were to become 1 on two binary vectors, then input 2 would become 0 on them, and consequently also on each unit vector; and then B would be equal to 0 on the same unit vector as β. Thus, only the function bc can arrive at input 1; at input 2, a function equal to 0 on $(1,1,0)$ and equal to 1 on $(0,0,1)$, i.e. e itself. But then input 3 is equal to 1 on $(1,0,0)$ and $(0,1,0)$, i.e. is equal to $b+c$. It is easy to see that the circuit so constructed in fact realizes the function B (see Fig. 4a).

Fig. 2

Fig. 3

B. From each element one line leaves, i.e. there is no branching. But then at each of the elements after the inverter one obtains a function equal to 1 on

Fig. 4

Figure 2: Fig. 4

the unit vectors and 0 on the binary ones (otherwise we shall not obtain B). Consequently, every monotone factor must have the form $b + c + e$, and every monotone term the form bce. Therefore each element after the inverter must have two inputs, and there must be two such elements.

In an optimal circuit the function bce does not participate in the construction of E. Indeed, sending, instead of bce, the identically zero function can change E only on the vector $(1, 1, 1)$. But such a sending preserves the monotonicity of the result, and therefore E will not change. By the same considerations bce does not participate in the construction of the function $b + c + e$.

The analogous assertion is true for the function $b + c + e$. But, since after the inverter we must spend at least 4 diodes, and on constructing the functions bce and $b + c + e$ also at least 4, then 8 diodes remain for constructing E, and the whole circuit coincides with that used in NAREC.**

Thus, under conditions 0°, in any circuit for obtaining B, the function E is applied to the inverter; moreover the optimal circuits: a) contain 16 diodes; b) the pre-inverter part is realized by the NAREC circuit, or by its dual; c) the post-inverter part is realized either by the circuit of Fig. 3a, or by the NAREC circuit, or by their dual circuits. Statements b) and c) are valid up to permutation of the quantities b, c, e. Any of the two variants

* The circuit in Fig. 3b is impossible because $B(1, 1, 1) \neq 0$.

** It should be noted that $b+c+e$ can be obtained both in accordance with the formula $b+c+e = (b+c)+e$ and with the formula $b+c+e = (b+c)+(bc+e)$. We do not regard this distinction in circuits as essential.

of the pre-inverter part is combined with any of the four variants of the post-inverter part.

If, in addition to the quantities b, c, e, the inverse of one of them (b', c', or e') is also available, then the preceding results are completely preserved: E must still be supplied to the inverter, and in the optimal circuits the additionally given quantity (b', c', or e') is not used.

0^{00}. We shall assume that, under conditions in which some set of the quantities b, c, e, b', c', e' is available to us from the very beginning, the adder must produce the carry in the form in which it uses it. We shall call admissible those sets for which such an adder can be constructed. Then, for admissible sets containing e and e', the optimal circuits with no more than 16 diodes are exhausted by the circuits in Figs. 4a and 4b.

Fig. 4

In the other cases:

1) In the case of three quantities, only the sets b, c, e and b, c', e' are admissible. The first corresponds to conditions 0^0; for the second, the optimal circuit contains more than 16 diodes.

2) Of four quantities, only the following sets are admissible: b, c, c', e; b, b', c', e'; b, c, c', e'. The case of the first set was discussed above; in the other two there are no circuits with no more than 16 diodes.

3) In the case of five quantities, to each of the sets b, b', c, c', e; b, b', c, c', e' there corresponds a unique (up to a permutation of the quantities b, c and dual transitions) optimal circuit (see Figs. 4b and 4e) with 16 diodes.* The circuit in Fig. 4e is the only one among all 16-diode circuits in which the carry used is obtained in the post-inverter part.

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Received
28 VI 1960

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1. M. A. Kartsev, *Arithmetic Devices of Digital Computing Machines*, Moscow, 1958.

* To the second set there corresponds, in fact, one more circuit, which, however, is very close to 4b: it is only necessary in 4b to transfer the inverter to the other input of the element giving B, change the sign of this element to the dual one, and throughout the entire circuit make the replacement $b \rightleftarrows b'$, $c \rightleftarrows c'$, $e \rightleftarrows e'$.

Note: Figure translations are in progress. See original paper for figures.