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Abstract

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Full Text

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Study on Parameter Optimization of an FPGA-Based Active-Discharge QTC

An Yilang1,2, Zhang Lele1,2, Yu Qianshun1,2, Yan Junwei1, Wen Shihai1,2, Ma Jinchao3, Li Yangbo3, Liu Junliang1,2, Zhang Yongjie1,2, Gan Meng4, Kong Jie1,2

(1. Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000;
2. School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing 100049;
3. College of Materials Science and Engineering, Hunan University, Hunan 410082;
4. College of Physics Science and Technology, Hebei University, Hebei 071002)

Abstract: The FPGA-based active-discharge QTC readout method is a readout circuit capable of simultaneously and accurately measuring the time and charge of particle-detector signals using only a small number of components. However, owing to the parasitic capacitance of FPGA I/O ports, this method can produce significant overshoot when processing small-charge signals. In this work, a circuit model including the parasitic parameters of the FPGA ports is established; the QTC shaping circuit is analyzed and numerically simulated;

and the component parameters and control logic of the shaping circuit are optimized. Signal overshoot is effectively suppressed, thereby improving the stability of the circuit under high-count-rate conditions. At present, a QTC readout electronics system designed on the basis of this method has completed laboratory performance tests and joint tests with a microchannel plate (MCP). Within a dynamic range of 4–84 pC, the charge-measurement resolution of this QTC readout circuit is better than 0.88%, the integral nonlinearity is 1.50%, and the time resolution is better than 42.3 ps. In joint tests with an MCP delay-line detector, dark-count imaging was able to produce an image with the same shape as the MCP. The test results show that the circuit designed on the basis of this method satisfies the readout requirements of MCP delay-line detectors.

Keywords: field-programmable gate array; charge-to-time conversion; charge resolution; time resolution; delay-line detector

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Introduction

Microchannel plate (MCP) delay-line detectors (DLDs), as experimental devices capable of simultaneously obtaining particle time-of-flight (TOF) and deposited-energy information while providing good position resolution, have numerous applications in nuclear and particle physics experiments as well as in space-detection missions [1-2]. In recent years, MCP detectors have been developing toward higher signal gain, faster readout rates, and better position resolution [3], which has correspondingly imposed higher requirements on the performance of readout electronics. Timing-measurement methods based on high-precision time-to-digital converters (TDCs) [4-5] and waveform-sampling methods based on analog-to-digital converters (ADCs) [6], as the two most common technical approaches, have been widely used in the design of MCP DLD readout electronics. However, although the former offers extremely high time–position resolution and excellent scalability, it is difficult to obtain sufficiently ideal energy resolution; although the latter has both time- and energy-measurement capabilities, its system structure is complex and the pressure on data transmission is high, making large-scale design difficult in application scenarios with limited space and power consumption. Therefore, it is necessary to find a readout method that can realize parallel readout of particle time and energy information while also possessing excellent scalability, so as to meet the future readout requirements of MCP detectors on the ground and in space.

The time-over-threshold (TOT) measurement method is a readout method that converts signal amplitude into pulse width. With the aid of a high-precision timing system, this method can extract particle time and energy information simultaneously with a relatively simple circuit structure. In the conventional TOT measurement method, the signal is compared with a reference level; the con-

version relationship between the input signal amplitude and the over-threshold pulse width exhibits relatively serious nonlinearity, which limits the energy-measurement precision of the method. To solve this problem, a TOT measurement method that optimizes the falling edge of the over-threshold pulse by means of linear discharge has emerged. On the basis of a charge integrator, the output port of a field-programmable gate array (FPGA) device is used as a constant-voltage source to ingeniously construct a constant discharge current, enabling a linear conversion between input charge and the pulse width of the shaped signal. By using a high-precision tapped-delay-line (TDL) TDC [7] based on an FPGA to time the leading and trailing edges of the shaped signal separately, this method can achieve high-precision measurement of particle time and energy information with a small number of components. It has the advantages of a simple structure and good scalability, and is currently widely used in time-of-flight (TOF) [[unclear: the text continues after the visible character "探"]] in positron emission tomography (PET).

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Author biography: An Yilang (1998–), male, from Chengdu, Sichuan, doctoral student, engaged in research on nuclear technology and applications; E-mail: anyilang@impcas.ac.cn
Corresponding author: Kong Jie, E-mail: kongjie@impcas.ac.cn

readout of detectors [8-9].

To meet the readout requirements of MCP DLD, this paper optimizes this method and designs and implements a readout electronics system for MCP DLD readout based on an active-discharge charge-to-time converter (Charge-to-Digital Converter, QTC). By establishing an accurate circuit model that includes the parasitic parameters of the FPGA ports, the influence of these parameters on the shaped signal is quantitatively analyzed; a new method is proposed to eliminate signal overshoot by optimizing peripheral components and introducing an adjustable gate-closing delay; finally, systematic experiments verify the performance of the optimized circuit and its feasibility for MCP-DLD readout.

1 FPGA-Based Active Linear-Discharge Shaping Method

1.1 Influence of the Electrical Characteristics of FPGA Ports

According to preliminary tests, the charge of the output signal from the MCP detector used in this work is mainly concentrated in the range of 5 $\sim$ 10 pC;

therefore, the integrating capacitor in the circuit is selected as 10 pF. However, FPGA chips are devices designed for processing digital signals, and their I/O ports have relatively large parasitic capacitance. Taking as an example the Xilinx FPGA chip model XC7K325TFFG900 used in this readout electronics system, the total parasitic capacitance of a single I/O port—including the die pad, package pins, and PCB-level distributed capacitance—is approximately 25 pF [10-11], which is of the same order of magnitude as the selected integrating capacitance. Therefore, the influence of the FPGA parasitic electrical parameters on the shaping circuit must be incorporated into circuit analysis and design.

1.2 Principle of FPGA-Based Active Discharge

The principle of the FPGA-based active-discharge circuit is shown in Figure 1. On the basis of a charge-sensitive amplifier circuit composed of an operational amplifier (hereinafter referred to as the op amp) and discrete components C_f, R_1, and R_2, two additional FPGA I/O ports are introduced, serving respectively as a voltage comparator and a constant-current discharge driver. According to the electrical characteristics of an FPGA I/O port when configured as a low-voltage differential signal (Low-Voltage Differential Signal, LVDS) receiver [12], when the differential-mode voltage between the positive and negative inputs of the port is less than zero, the receiver outputs logic "0" to the FPGA chip; otherwise, the receiver output is logic "1". By taking advantage of this characteristic and providing a fixed level V_{th} to its negative input, the receiver can be used to implement the function of a voltage comparator. Another I/O port is configured as a tri-state buffer for controlling the operating state of the peripheral circuit. The tri-state output port provided by the FPGA can be configured to output logic "0", logic "1", and a high-impedance state; among these, when outputting logic "1", the level output to the peripheral circuit is determined by the FPGA supply voltage [13]. When the output of this port is set to the high-impedance state, the peripheral circuit behaves as a charge integrator with a time constant $\tau = C_f(R_1 + R_2)$. When the output of this port is set to logic "0" or logic "1", it provides a constant level to the peripheral circuit, namely 0 V or a level equal to the FPGA supply voltage. At this time, the feedback loop containing the resistor is cut off, and the peripheral circuit no longer behaves as a charge integrator; instead, through the virtual short of the op amp, a fixed voltage difference is formed across the two ends of resistor R_1. The three output states of this output port are controlled by FPGA logic.

Figure 1 (color online) Block diagram of the FPGA-based active-discharge circuit

In Figure 1, C_p denotes the parasitic capacitance at the output terminal of the tri-state buffer. Because the input impedance of an FPGA port is very high when it is used as an input, the influence of its parasitic capacitance can be neglected; therefore, the influence of the output-terminal parasitic capacitance C_p is mainly considered. In the design of this paper, the tri-state buffer is con-

figured with an LVCMOS level standard that provides relatively strong output drive capability [12]. Therefore, when it outputs logic "0"or "1", i.e., a fixed level v_s, its strong drive capability can compensate for the influence of the parasitic capacitance C_p. At this time, the circuit satisfies the following state equations:

$$\begin{cases} v_s = i_1 R_1 \\ i_f = i_1 + i_{\text{in}} \\ i_f = -C_f \dfrac{dv_o}{dt}, \end{cases} \tag{1}$$

where v_o is the circuit output voltage; i_1 and i_f are the currents flowing through R_1 and C_f, respectively; and i_{in} is the current pulse signal from the detector, whose integral is the total charge Q of the input signal.

By simplifying and integrating equation set (1), one obtains:

$$v_o = v_o\big|_{t=0} - \frac{v_s}{R_1 C_f} t - \frac{1}{C_f} \int i_{\text{in}}\, dt, \tag{2}$$

When the tri-state buffer outputs logic "0", $v_s = 0$ in equation (2), and the change in the output voltage v_o is completely determined by the input charge signal; that is, the circuit operates in the "integration only" state. When the tri-state buffer outputs logic "1", v_s in equation (2) is equal to the FPGA supply voltage (3.3 V in the design of this paper). In addition to the input signal from the detector, there is also a constant discharge current supplied by the FPGA tri-state buffer in the circuit; that is, the circuit operates in the constant-current discharge state.

On this basis, the control logic shown in Figure 2 is used to actively discharge the integrating circuit. When the comparator identifies the input signal accumulated on the integrating capacitor C_f, the electronics system controls the output state of the tri-state buffer to implement a shaping process of "integration only" followed by constant-current discharge, where T_{delay} denotes the duration of the "integration only" process. Figure 3 presents a schematic waveform of the shaped signal of the active-discharge circuit. During this shaping process, the circuit output voltage v_o successively crosses the preset threshold V_{th} twice, respectively be comp

recorded by the comparator as T_{start} and T_{end}.

Figure 2 (Color online) Logic diagram of the FPGA-based active-discharge control. The output of the tri-state buffer is labeled "Z" when it is in the high-impedance state.

Figure 3 (Color online) Schematic diagram of the active-discharge signal shaping.

By setting a sufficiently long T_{delay}, greater than three times the detector-signal decay time constant, the input signal can be guaranteed to have been completely integrated on the integrating capacitor C_{f} before that moment. During the interval from $t = 0$ to $t = T_{\mathrm{delay}}$, the output voltage of the tri-state buffer is $v_s = 0$. From Eq. (2), the circuit output voltage v_o at T_{delay} satisfies

$$v_o\big|_{t=T_{\mathrm{delay}}} = v_o\big|_{t=0} - \frac{1}{C_{\mathrm{f}}}\int_{t=0}^{T_{\mathrm{delay}}} i_{\mathrm{in}}\,\mathrm{d}t, \tag{3}$$

It can therefore be seen that, when the circuit output voltage v_o returns again to the comparison threshold V_{th} at T_{end}, the following relation holds:

$$v_o\big|_{t=T_{\mathrm{end}}} = v_o\big|_{t=T_{\mathrm{delay}}} - \frac{v_s}{R_1 C_{\mathrm{f}}}\left(T_{\mathrm{end}} - T_{\mathrm{delay}}\right) \tag{4}$$

$$V_{\mathrm{th}} = -\frac{Q}{C_{\mathrm{f}}} - \frac{v_s}{R_1 C_{\mathrm{f}}} T_{\mathrm{discharge}}. \tag{5}$$

That is, the input-signal charge Q has a linear relationship with the active-discharge duration $T_{\mathrm{discharge}}$. This method can linearly convert the charge of the input signal into the time-over-threshold of the shaped signal. By measuring the timing of T_{start} and T_{end}, the time and charge information of the detector input signal can be obtained.

2 Parameter optimization of the active-discharge circuit

In the above analysis, the circuit state after the end of the active-discharge process, i.e., after the moment T_{end}, was not considered. At T_{end}, the circuit output voltage is $v_o = V_{\mathrm{th}}$. Ideally, the small amount of charge remaining on the integrating capacitor will be slowly discharged through the R_1 and R_2 resistor branches, so that the output voltage eventually returns to the baseline. During testing, it was observed that, under certain resistance–capacitance selections and V_{th} settings, a relatively large overshoot appears on the falling edge of the shaped signal, as shown by the green waveform in Fig. 4. This is because, although the output of the tri-state buffer has been turned off at T_{end}, some charge still remains on the parasitic capacitance C_{p} of the FPGA I/O port. After being divided through R_1 and R_2, this charge replaces the tri-state buffer and continues to provide discharge current to the integrating capacitor. When the amount of charge shunted to the integrating capacitor is relatively large, a significant overshoot is formed at the output. This overshoot prolongs the time required for the output voltage to return to the baseline and affects circuit performance at high event rates.

Figure 4 (Color online) Waveforms of the active-discharge shaped signal acquired using an Agilent Technologies MSO7034B oscilloscope. The yellow and

green waveforms are the shaped waveforms of the same input signal under different circuit electrical parameters. The scales in the x and y directions are 100 ns/div and 100 mV/div, respectively.

To determine the relationship between the above overshoot and the selection of the circuit parameters C_{f}, R_1, R_2, and V_{th}, this work analyzes the circuit behavior after T_{end}. When the tri-state buffer is turned off at T_{end}, the input signal from the detector has already ended. At this time, according to the virtual-open effect at the operational-amplifier input terminal, $i_f = i_1$. The active-discharge circuit then satisfies the following set of state equations:

$$\begin{cases} i_s = i_1 + i_2, \\ i_1 = -C_{\mathrm{f}}\dfrac{\mathrm{d}v_o}{\mathrm{d}t}, \\ v_s - \dfrac{1}{C_{\mathrm{p}}}\displaystyle\int i_s\,\mathrm{d}t = i_2 R_2 + v_o, \\ v_o = i_1 R_1 - i_2 R_2, \end{cases} \tag{6}$$

where i_1, i_2, and i_s are the currents flowing through R_1, R_2, and C_{p}, respectively. From this system of equations, the differential equation for v_o can be obtained as

$$C_{\mathrm{p}}C_{\mathrm{f}}R_1R_2\frac{\mathrm{d}^2v_o}{\mathrm{d}t^2} + C_{\mathrm{f}}(R_1+R_2)\frac{\mathrm{d}v_o}{\mathrm{d}t} + v_o = 0, \tag{7}$$

with characteristic equation

$$C_{\mathrm{p}}C_{\mathrm{f}}R_1R_2\lambda^2 + C_{\mathrm{f}}(R_1+R_2)\lambda + 1 = 0, \tag{8}$$

which gives

$$\lambda = -\frac{R_1+R_2}{2C_{\mathrm{p}}R_1R_2} \pm \frac{1}{2C_{\mathrm{p}}R_1R_2}\sqrt{(R_1+R_2)^2 - 4\frac{C_{\mathrm{p}}}{C_{\mathrm{f}}}R_1R_2}. \tag{9}$$

Let

$$D = (R_1+R_2)^2 - 4\frac{C_{\mathrm{p}}}{C_{\mathrm{f}}}R_1R_2, \tag{10}$$

If $D < 0$, the two roots λ_1 and λ_2 of Equation (8) are complex; in this case v_{o} exhibits relatively large oscillations. Therefore, this paper considers only the case $D \geq 0$. The general solution of the original differential equation (7) is then

$$v_{\mathrm{o}} = C_1 e^{-\frac{1}{2C_{\mathrm{p}}R_1R_2}(R_1+R_2-\sqrt{D})t} + C_2 e^{-\frac{1}{2C_{\mathrm{p}}R_1R_2}(R_1+R_2+\sqrt{D})t}, \tag{11}$$

where C_1 and C_2 are constants. The above analysis starts from the circuit state at time T_{end}, when the circuit output voltage satisfies $v_{\mathrm{o}}|_{t=0} = V_{\mathrm{th}}$. Substituting this boundary condition and the general solution of differential equation (7) into the original Equation (6) gives

$$\begin{cases} C_1 = -\dfrac{1}{2\sqrt{D}}\left[2\dfrac{C_{\mathrm{p}}}{C_{\mathrm{f}}}v_{\mathrm{s}}R_2 - (R_1+R_2)V_{\mathrm{th}}\right] + \dfrac{1}{2}V_{\mathrm{th}} \\ C_2 = \dfrac{1}{2\sqrt{D}}\left[2\dfrac{C_{\mathrm{p}}}{C_{\mathrm{f}}}v_{\mathrm{s}}R_2 - (R_1+R_2)V_{\mathrm{th}}\right] + \dfrac{1}{2}V_{\mathrm{th}}. \end{cases} \tag{12}$$

It can be seen from this that, after the tri-state buffer is turned off at T_{end}, the time evolution of the output waveform after the discharge has ended is determined directly by C_{f}, C_{p}, R_1, R_2, and V_{th}, and is independent of the input signal. The test results shown in Figure 5 verify this conclusion: after discharge ends, signals of different amplitudes exhibit consistent trailing-edge undershoot waveforms.

Figure 5 (online color figure) Active-discharge shaping-signal waveforms acquired by an oscilloscope in persistence mode. A trailing-edge undershoot with consistent shape and amplitude, independent of the signal peak value, can be observed. The horizontal and vertical scales in the figure are 500 ns/div and 200 mV/div, respectively.

According to the data sheet provided by the FPGA manufacturer, when the I/O port of the FPGA chip used is configured for the LVDS level standard, the recommended maximum input voltage is 2.5 V [12]. When the FPGA I/O port discriminates the signal by means of a comparator, its timing precision is largely determined by the rate of change of the signal voltage at the threshold-crossing time, and this rate of change is mainly determined by the chosen values of C_{f} and R_1 [14]. Taking into account the need to ensure normal system operation while achieving as large an amplification factor as possible to improve resolution, the selected integrating capacitance is $C_{\mathrm{f}} = 10$ pF.

This selected value was substituted into Equation (11) for numerical simulation, in order to study the influence of different circuit-component values on the signal overshoot. Figure 7 shows the variation of the trailing-edge overshoot of the shaped signal when R_1, R_2, and V_{th} are changed, respectively. It can be seen that, by selecting appropriate circuit parameters, the additional charge from the parasitic capacitance C_{p} can cancel the residual charge on the integrating capacitor. Thus, while eliminating the shaped-signal overshoot, the current from the parasitic capacitance is used to replace the natural discharge process of the residual charge through the resistor branch. As shown by the yellow waveform in Figure 4, this can shorten the time required for the trailing edge of

the signal to recover to the baseline and improve the circuit' s ability to process high-event-rate signals. To achieve this goal, the specific values of each circuit parameter must be determined.

In an actual circuit system, because PCB-level distributed capacitance exists, the true value of the parasitic capacitance C_{p} differs from the parasitic parameters of the FPGA I/O port. To determine the specific value of C_{p}, the trailing-edge waveform obtained by numerical simulation was compared with the signal waveform acquired from the actual circuit. To make the difference between the two clearly observable, the parameter settings $C_{\mathrm{f}} = 10$ pF, $R_1 = 10$ k , $R_2 = 2$ k , and $V_{\mathrm{th}} = 80$ mV were selected so that the shaped signal exhibited a pronounced trailing-edge undershoot. Figure 6 compares the actual shaped-circuit output waveform acquired by the oscilloscope with the overshoot shape obtained by numerical simulation. The yellow waveform is the actual signal, while the blue dash-dotted waveform is the trailing-edge undershoot obtained by numerical simulation when $C_{\mathrm{p}} = 26$ pF. It can be seen from the figure that the two agree well; therefore, in the subsequent analysis and design, 26 pF is used as the estimated value of the parasitic capacitance C_{p}.

Figure 6 (online color figure) Comparison between the active-discharge waveform signal acquired by the oscilloscope and the numerical simulation result. The yellow waveform is the actual circuit output, and the blue dash-dotted waveform is the numerical simulation result. The horizontal and vertical scales in the figure are 100 ns/div and 200 mV/div, respectively.

Because of component precision errors and physical fluctuations in the electrical characteristics of the FPGA I/O port, it is difficult to determine the exact value of the parasitic capacitance C_{p}. On the other hand, during joint testing with the detector, the discrimination threshold V_{th} must be adjusted according to the actual signal conditions. These factors all affect the overshoot of the shaped signal, making it impossible to obtain a signal-shaping effect consistent with the optimal circuit parameters obtained by simulation. To address this problem, this paper introduces an adjustable delay t_0 before the tri-state buffer is turned off, as shown in Figure 8. Here, T_{end} and T'_{end} denote, respectively, the time at which the amplitude of the shaped signal drops to the threshold level and the time at which the tri-state buffer is turned off. From Equation (2), the actual circuit output voltage v'_{o} at time T'_{end} is

$$\begin{aligned} v'_{\mathrm{o}} &= v_{\mathrm{o}}\big|_{t=0} - \frac{v_{\mathrm{s}}}{R_1 C_{\mathrm{f}}} t \\ &= V_{\mathrm{th}} - \frac{v_{\mathrm{s}}}{R_1 C_{\mathrm{f}}} t_0. \end{aligned} \tag{13}$$

By adjusting this delay t_0, the actual time at which the tri-state buffer is turned off can be changed.

Figure 7 Simulation of the trailing edge of QTC shaped signals under different circuit parameters

(Online color figure) (a) Signal trailing edges for different R_1 values when C_f = 10 pF, R_2 = 300 Ω, and V_th = 50 mV; (b) signal trailing edges for different R_2 values when C_f = 10 pF, R_1 = 50 kΩ, and V_th = 50 mV; (c) signal trailing edges for different V_th values when C_f = 10 pF, R_1 = 50 kΩ, and R_2 = 300 Ω. In the simulation, C_p = 25 pF, and the signal baseline $v_o = 0$ is indicated by a dashed line.

Figure 8 (Online color figure) Gate-control logic of the tri-state buffer after introducing the delay

Figure 9 (Online color figure) Waveform of the active-discharge shaped signal under the optimized parameter design, acquired with an Agilent Technologies MSO7034B oscilloscope. The scales in the x and y directions are 200 ns/div and 200 mV/div, respectively.

[[unclear: beginning of sentence]] actual circuit output level, so that the trailing edge of the shaped signal can satisfy, as far as possible, the ideal condition of no overshoot. Meanwhile, as shown in Figure 8, what is changed by this delay is only the control logic of the tri-state buffer, rather than the actual signal threshold-crossing time identified by the discriminator. The duration of the linear discharge can still be obtained by measuring the time difference between T_end and T_delay.

Finally, according to the simulation results, the selected circuit component parameters are C_f = 10 pF, R_1 = 200 kΩ, and R_2 = 300 Ω. The operational amplifier is the AD8066 chip from ADI, with a bandwidth of 145 MHz [15], to ensure that the bandwidth requirement corresponding to the shaping-circuit time constant $\tau = C_\mathrm{f}(R_1 + R_2)$ is satisfied. Figure 9 shows the shaped waveform acquired by an oscilloscope under these circuit-component parameter conditions.

3 Readout Electronics Performance Test

To verify the performance of the QTC readout electronics under these parameters, this work tested the electronics using a signal generator and an MCP detector, respectively, as signal sources.

A Tektronix AFG3252C pulse signal generator was used as the signal source. The square-wave signal it outputs passes through a voltage-to-charge conversion circuit built with a capacitor, is converted into a charge pulse, and is then input into the active-discharge shaping circuit. The charge amount of the pulse is therefore the product of the square-wave amplitude and the conversion capacitance. At the same time, an additional pulse signal with the same frequency and phase was drawn from the signal source as a reference and directly input into the FPGA, for measuring the timing performance of the electronics. Figure 10 shows, for an input charge of 20 pC, the distributions of the time differences between the timing results $T_\mathrm{discharge}$ and T_start measured by the QTC electronics and the reference signal.

By changing the amplitude of the square-wave signal, the timing and charge-measurement performance of the readout electronics were measured for an input charge range of 4 ∼ 104 pC. Figure 11 shows the measurement results under these test conditions. It can be seen that, over the charge range of 4 ∼ 84 pC, the circuit output exhibits good linearity. Within this input range, the charge-measurement accuracy of the QTC circuit is better than 0.88%, the integral nonlinearity is INL = 1.50%, the timing resolution is better than 42.3 ps, and the average resolution is 13.0 ps.

In addition, to verify the readout function of the QTC readout electronics for MCP DLD signals, this work carried out a preliminary imaging test in combination with the detector. Figure 12 is a schematic diagram of the imaging principle of the MCP DLD detector. Electrons released by the probe are multiplied by the MCP, drift in a high-voltage electric field, and are finally received by the delay line serving as the anode wire. After a particle reaches the anode wire, the generated signal propagates from the hit position toward the two ends of the delay line. By measuring the time difference between the arrival of the signal at the two ends of one delay line, the hit position of the particle on that anode line can be obtained. Using two mutually perpendicular delay lines, the coordinates of the signal hit position on a two-dimensional plane can be obtained [16]. In the actual test process, in addition to measuring the four output signals of the delay-line anode wires, an additional

Figure 10 (color online) Signals measured by the QTC electronics for an input charge of 20 pC: (a) distribution of the time difference between the T_{start} timing result and the reference signal; (b) distribution of $T_{\text{discharge}}$.

One signal is taken from the MCP for coincidence with the anode-wire signals.

In this work, the QTC readout circuit is used to time the MCP output signal and the four anode-wire output signals, respectively, to measure MCP dark counts. For the MCP detector used in the test, the dark-count event rate is usually no more than 50 Hz [17]. As can be seen from Fig. 11, within the dynamic range of input charge from 4 to 84 pC, the discharge time $T_{\text{discharge}}$ does not exceed 6 μs; therefore, it can be used for MCP dark-count readout. During the test, the criterion is that, after an MCP trigger, each of the four anode-wire outputs has one and only one trigger. The arrival times of the signals from the two ends of the anode wires in the X and Y directions at the QTC readout electronics are calculated as follows:

$$\begin{cases} T_{\text{x1}} = t_{\text{x1}} - t_0 \\ T_{\text{x2}} = t_{\text{x2}} - t_0 \\ T_{\text{y1}} = t_{\text{y1}} - t_0 \\ T_{\text{y2}} = t_{\text{y2}} - t_0, \end{cases} \tag{14}$$

where t_0 is the MCP signal timing result, and t_{x1}, t_{x2}, t_{y1}, and t_{y2} are the timing results of the readout signals from the two ends of the anode wires in the

x and y directions, respectively. All coincidence events are accumulated into a two-dimensional distribution according to $(T_{x1}-T_{x2}, T_{y1}-T_{y2})$, finally yielding the uniform circular-disk image with the same shape as the MCP shown in Fig. 13.

Figure 11 (color online) (a) For an input charge range of 4–104 pC, the charge-measurement linearity and resolution of the QTC circuit, expressed in terms of the discharge time $T_{\mathrm{discharge}}$. The circuit output has better linearity when the charge range is 4–84 pC. (b) Timing-measurement resolution of the QTC circuit for an input charge range of 4–84 pC.

Figure 12 (color online) Schematic diagram of the imaging principle of the MCP DLD detector.

4 Conclusion

This paper analyzed and simulated the circuit behavior of an FPGA-based actively discharged QTC shaping circuit under the influence of FPGA parasitic parameters, and proposed a solution based on optimization of circuit parameters and control logic to address the overshoot defect of this readout method when processing small signals. On this basis, a QTC readout circuit suitable for MCP DLD signal readout was designed,

Fig. 13 (color online) Imaging result of the background disk of the MCP DLD

Preliminary performance tests were also carried out using a pulse-signal generator and an MCP detector. In the test using the pulse-signal generator as the signal source, the QTC readout circuit achieved a charge resolution better than 0.88% over an input range of 4–84 pC, an integral nonlinearity of charge measurement of 1.50%, and a time resolution better than 42.3 ps, meeting the application requirements of the MCP detector. In the preliminary joint test with the MCP DLD detector, by measuring the MCP dark-count signal, a pattern with the same shape as the MCP was obtained. In subsequent work, imaging tests of the MCP DLD detector will be carried out with the aid of a perforated mask, to further investigate the overall temporal and spatial resolution of the system.

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Design and Parameter Optimization of an FPGA-Based Active-Discharge QTC

AN Yilang1,2, ZHANG Lele1,2, SHE Qianshun1,2, YAN Junwei1, WEN Shihai1,2, MA Jinchao3, LI Yangbo3,
LIU Junliang1,2, ZHANG Yongjie1,2, GAN Meng4, KONG Jie1,2

(1. Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China;
2. School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing 100049, China;
3. College of Materials Science and Engineering, Hunan University, Hunan 410082, China;
4. College of Physics Science & Technology, Hebei University, Hebei 071002, China)

Abstract: An FPGA-based active-discharge QTC readout method is a compact and efficient approach that enables simultaneous high-precision measurements of timing and energy for particle-induced signals using a relatively small number of components. Owing to the presence of parasitic capacitance associated with FPGA I/O ports, this method suffers from excessive signal overshoot when processing low-charge signals. In this work, a circuit model incorporating the parasitic capacitance of the FPGA I/O ports is established to analyze and numerically simulate the QTC shaping circuit. The component parameters and control logic of the shaping circuit are optimized to effectively suppress signal overshoot, thereby improving the stability of the circuit under high count-rate conditions. At present, a QTC readout electronics system designed using this method has completed laboratory tests and preliminary joint tests with an MCP delay-line detector. Within a dynamic range of 4–84 pC, the QTC readout circuit achieves an input charge resolution better than 0.88% and an integral nonlinearity of 1.50%. For time measurements, a best resolution of 42.3 ps has been achieved. In the joint test with the MCP delay-line detector, the dark counts can be used to correctly reconstruct an image with the same shape as the MCP. The test results indicate that the circuit designed based on this readout method satisfies the readout requirements of the MCP delay-line detector.

Key words: Field-programmable gate arrays; charge-to-time converter; charge resolution; time resolution; delay-line detector;

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Corresponding author: KONG Jie, E-mail: kongjie@impcas.ac.cn

Note: Figure translations are in progress. See original paper for figures.

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