Development and Preliminary Testing of the BEPCII Transverse Feedback System Electronics

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Abstract

This paper presents the development and preliminary testing of a digital bunch-by-bunch feedback system for suppressing transverse beam oscillations in BEPCII. In the high-current, multibunch operation mode, transverse coupled-bunch instabilities can induce beam oscillations, which in severe cases lead to reduced collision luminosity and degraded beam lifetime, and therefore must be suppressed by a feedback system. This work is based on a commercial Micro TCA hardware platform, employs a field-programmable gate array (FPGA) as the core processor, independently designs a finite impulse response (FIR) digital filter suitable for transverse feedback, and completes the development of the corresponding signal-processing electronics. Two filter design methods, the time-domain least-squares method and the selected-filter method, are compared and analyzed in detail, and the optimal algorithm and parameters are ultimately determined. Beam experiments show that the system can effectively suppress transverse oscillations, with a damping time of 0.3 ms, meeting the expected target of within 0.5 ms, successfully fulfilling the BEPCII design requirements and marking a key step toward domestic development.

Full Text

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Abstract This paper introduces the development and preliminary testing of the electronics for a digital bunch-by-bunch feedback system designed to suppress transverse beam oscillations in the BEPCII. Transverse coupled-bunch instabilities generated under high-current, multibunch operation can lead to beam oscillations and, in severe cases, reduce collision luminosity and degrade beam lifetime; therefore, they must be suppressed by a feedback system. Based on a commercial MicroTCA hardware platform and using a field-programmable gate array (FPGA) as the core processor, this work independently designed a finite impulse response (FIR) digital filter suitable for transverse feedback and completed the corresponding signal-processing electronics development. A comparative analysis was conducted focusing on two filter design methods—time-domain least squares and selective filtering—and the optimal algorithm and parameters were ultimately determined. Beam experiment results show that the system can effectively suppress transverse oscillations, with a damping time of 0.3 ms, meeting the expected target of within 0.5 ms. The system

successfully satisfies the BEPCII design requirements and represents a key step toward domestic development.

Key words Transverse feedback system, BEPCII, Coupled-bunch instability, Digital filter

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Development and preliminary testing of the BEPCII transverse digital feedback system

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Abstract This paper presents the development of a digital bunch-by-bunch feedback system designed to suppress transverse beam oscillations in the BEPCII. Transverse coupled bunch instabilities arising due to high-current and multi-bunch operation mode can lead to beam instabilities, significantly degrading collision luminosity and beam lifetime, thus active feedback is necessary. Based on a commercial MicroTCA.4 hardware platform and using a field-programmable gate array (FPGA) as the core processor, a finite impulse response (FIR) digital filter tailored for transverse feedback was independently designed, and the corresponding signal processing electronics were developed. A comparative analysis was conducted between two filter design methods—time-domain least squares fitting and selective wave filtering to identify the optimal algorithm and parameters. Beam test results demonstrate that the system effectively suppresses transverse oscillations, achieving the damping time of 0.3ms and successfully meeting the design requirements 0.5ms of BEPCII. This system provides critical technical support for the high-luminosity stable operation of the facility.

Key words Transverse feedback system, BEPCII, Coupled bunch instability, digital filter

The Beijing Electron Positron Collider upgrade project (Upgrade of Beijing Positron Electron Collider, BEPCII) is a facility operating at

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an internationally leading high-energy physics experimental facility in the τ-charm physics energy region, with an energy range from 1.0 GeV to 2.1 GeV (up to 2.8 GeV in the latest upgrade), and an optimized luminosity of 1.0×10^{33} cm^{-2} s^{-1} at the 1.89 GeV energy point[1-2]. Owing to the effects of higher-order modes in the RF cavities and resistive-wall impedance, transverse beam instabilities can occur very readily, leading to reduced beam lifetime and lower collision luminosity, and thus becoming a key bottleneck limiting improvement of the facility performance. According to simulation calculations by Researcher Wang Jiuqing, the instability growth time of the fastest transverse mode is 4.3 ms[3]. In 2009, beam-measurement personnel and Dmitry measured the instability growth time using the commercial iGp feedback system; extrapolating from the test data, the instability growth time at a beam current of 1 A is 0.63 ms[4]. One effective means of suppressing instabilities is a bunch-by-bunch feedback system, which can rapidly damp beam oscillations by detecting bunch positions in real time, quickly computing correction signals, and applying excitation. In general, the system damping time must be shorter than the beam instability growth time; therefore, the design value for the damping time of the BEPCII feedback system was chosen to be 0.5 ms.

At present, accelerator facilities in China and abroad commonly use commercial bunch-by-bunch feedback systems, such as iGp12, to suppress beam instabilities. Internationally, for example, during the initial commissioning of the SuperKEKB collider at the High Energy Accelerator Research Organization (KEK) in Japan, damping times of 1.1 ms and 0.6 ms were achieved in the vertical direction for the LER and HER, respectively[5]. The European Synchrotron Radiation Facility (ESRF) obtained damping times of 0.2–0.9 ms through single-bunch commissioning[6]. At the Pohang Accelerator Laboratory (PAL) in Korea, the PLS-II light source can suppress beam instabilities within 0.5 ms; when the bunch-by-bunch feedback system is turned on again after more than 0.5 ms, it cannot completely suppress the oscillations and can only slow the instability growth rate[7]. In China, the bunch-by-bunch feedback system developed by the Shanghai Synchrotron Radiation Facility (SSRF) achieved a damping time of 0.37 ms[8]; with the facility upgrade, the transverse feedback electronics will adopt the iGp-720 feedback processor and the matching FBE-500LT RF front end[9].

The BEPCII transverse feedback system uses commercial iGp-396 electronics, which have worked well at BEPCII and can effectively suppress beam oscillations[10]. However, problems also exist, such as limited customization capability, high upgrade and maintenance costs, and lack of control over core technologies; for example, the filter order cannot be changed at the underlying level. For this reason, this paper carries out the independent development of a BEPCII digital bunch-by-bunch feedback system. The research goal is to design a dedicated FIR filter suitable for BEPCII based on the MicroTCA.4 hardware platform

and an FPGA real-time processing architecture, to achieve the target of a transverse beam-oscillation damping time better than 0.5 ms, and to complete online verification under high-current multibunch conditions. The main contributions of this work include:

(1) Completing an initial attempt at the domestic development of BEPCII transverse digital feedback electronics and verifying the implementation of the filter algorithm in the FPGA;

(2) Proposing and comparing two filter design schemes, and providing an optimal selection basis suitable for the BEPCII operating point;

(3) Achieving sub-millisecond stable damping, with key performance indicators reaching the level of comparable international facilities.

1 Design of the Bunch-by-Bunch Feedback System

Large accelerator facilities in China and abroad have conducted research on bunch-by-bunch feedback systems tailored to the characteristics of their own accelerators. For example, the Deutsches Elektronen-Synchrotron (DESY) designed a new bunch-by-bunch feedback system according to the characteristics of the Positron–Electron Tandem Ring Accelerator (PETRA IV)[11]. The United Kingdom's Diamond Light Source (DLS) has phased out the Libera platform and developed a set of high-performance feedback processors integrating transverse and longitudinal functions based on the MicroTCA platform[12], which is still under development. In China, the transverse bunch-by-bunch feedback electronics system independently developed by SSRF realizes two-stage precision delay adjustment and bunch-by-bunch gain adjustment, enabling transverse suppression[13-14]. Different accelerators'

The machine parameters (such as chromaticity and impedance) differ greatly, and BEPCII has a unique double-ring structure and a specific tune value (approximately 0.57 in the vertical direction). This requires the feedback filter to provide an accurate -90° phase shift near tune points that are neither integer nor half-integer. The main difference between this work and the systems described above is that, for the specific physical parameters of BEPCII, the electronics hardware configuration is designed and the FIR filter coefficient calculation method is optimized, so as to achieve the maximum damping efficiency under limited hardware resources.

As shown in Fig. 1, in the BEPCII bunch-by-bunch feedback system, the beam signal acquired by the beam position monitor (Beam Position Monitor, BPM) is fed into the Hybrid, where addition and subtraction operations are performed to obtain the oscillation signals in the X and Y directions. After processing by the front-end electronics, this signal is transmitted to the digital signal-processing electronics, where the correction signal is calculated. The correction signal then passes through a power amplifier and is fed into the kicker, where an excitation electromagnetic field is generated on the kicker stripline electrodes to act on

the corresponding bunches and suppress transverse oscillations. The BEPCII transverse digital feedback system developed in this work focuses only on the digital signal-processing electronics, namely the green module marked in Fig. 1, which is responsible for real-time processing of the beam oscillation signal and output of the correction signal. The detailed architecture is described in the next section.

Figure 1 diagram labels (translated): BPM; A, B, C, D; Hybrid; X/Y; front-end electronics; digital signal-processing electronics; power amplifier; kicker.

Fig. 1 Schematic diagram of the transverse feedback system

Fig.1 Schematic diagram of the transverse bunch by bunch feedback system

1.1 Hardware Architecture of the Bunch-by-Bunch Feedback System

The RF frequency of BEPCII is 499.8 MHz. To sample and feed back each bunch, the sampling rate of the ADC/DAC should not be lower than this frequency. The FPGA processing unit is responsible for turn-by-turn data processing as well as the computation required by the FIR filtering algorithm; therefore, the multiplier resources of the FPGA must satisfy the requirements of the filter design. On this basis, the system adopts a MicroTCA.4+FPGA architecture, selecting Vadatech AMC725, AMC516, and FMC212 as the core hardware components. The system hardware structure is shown in Fig. 2: the AMC725 is responsible for high-speed data communication and system expansion; the AMC516 serves as an FPGA carrier with an FMC (FPGA Mezzanine Card, VITA standard) interface and is equipped with a Xilinx Virtex-7 690T FPGA for implementing real-time digital signal-processing algorithms; the FMC212 daughter card provides dual-channel ADCs (supporting a sampling rate of 1.5 GSPS) and dual-channel DACs (supporting a sampling rate of 2.8 GSPS), which are responsible for analog-to-digital conversion of the beam signal and analog output of the correction signal, respectively.

Fig. 2 Schematic diagram of the hardware architecture of the transverse feedback system

Fig. 2 Schematic diagram of the hardware architecture of the transverse feedback system

1.2 Signal Processing Flow

The principle of the bunch-by-bunch transverse feedback system is to extract information on the centroid oscillation of each bunch, obtain a correction signal after signal processing, and apply it one by one to the corresponding bunches, thereby suppressing coherent oscillations between bunches. The processing flow is shown in Fig. 3. The system first samples the received bunch-by-bunch analog signal with an ADC and converts it into a digital signal; the data are then sent through the FMC interface to the FPGA for processing, and the correction signal

is converted by the DAC into an analog signal for output. Because the bunch-by-bunch feedback signal is calculated on the basis of the oscillation signals from several preceding turns of the bunch, three processes are required in the FPGA: extracting the multi-turn digital signal of each bunch according to the bunch number; calculating the transverse feedback signal after this signal is filtered by the designed N-th-order filter; and finally recombining it into a bunch-by-bunch signal for output.

In a transverse feedback system, the filter order is directly proportional to the system resource overhead and processing latency. Therefore, the key to developing a bunch-by-bunch feedback system lies in the design of the filter, which is used to realize two core functions: first, filtering out the DC component in the signal; and second, providing an accurate 90° phase shift [15]. If the filter order is too low, the amplitude–frequency response characteristics of the designed filter will be unsatisfactory, the DC signal cannot be completely removed, and the amplifier may easily become saturated or even be damaged. If the filter order is too high, a large delay will be introduced, lengthening both the signal acquisition time and the signal processing time, which is unfavorable for real-time feedback. In view of the requirement that the damping time of the BEPCII transverse feedback system be controlled within 0.5 ms, and after comprehensively weighing the amplitude–frequency characteristics, resources, and latency constraints, this system ultimately adopts a 20th-order filter.

Fig. 3 Signal-processing flowchart

1.3 Filter Design

At present, filter design for feedback systems mainly adopts two methods: the time-domain least-squares fitting method (Time-Domain Least-Squares Fitting, TDLSF) and the selective-filter method.

The TDLSF method was first proposed by Nakamura[^16] and has been applied in the feedback systems of many accelerator laboratories, such as Hefei Light Source[^17], SSRF[^18–^20], APS[^21], and other light sources. For filters designed by this method, within the allowable drift range of the operating point (Tune), the feedback system provides the same gain and phase. The selective-filter method was first applied to longitudinal feedback systems. The core idea of this method is to digitally sample a sine wave with the same frequency as the Tune frequency, and to use the sampling points as the impulse response. Its advantages are simple design and the absence of complex matrix calculations. By adjusting the modulation coefficient of the sine-wave frequency and its phase, the maximum amplitude-frequency response and a linear phase can be obtained at the Tune frequency. A low-order filter can improve the adaptability of the filter and obtain a suitable phase over a wider range of operating-point drift; a high-order filter can improve filter performance[^22], but increases hardware overhead and time delay. Table 1 shows the filter configurations of digital feedback systems in several similar accelerator facilities in China and abroad.

Table 1 Filter Order

Accelerator	Platform	Order
BEPCII	iGp12	23
SSRF	PXI-6U	20
HLS-II	TED	20
TLS	SPring-8 architecture	20
DAΦNE	iGp	16
DELTA	iGp12	24
BESSY-II	iGp12	32
SuperKEKB	iGp12	18
Australian Synchrotron	I-tech	16

For similar accelerator facilities, the order used ranges from 16 to 32, and order 20 is a common choice for multiple facilities. To determine the optimal order, as introduced in Reference 23, when the ratio of the filter order N to the operating point ν is close to an integer, the sinusoidal sequence approximately completes an integer number of periods, and good DC suppression can be obtained. This paper comprehensively considers the following factors:

(1) **DC-component suppression capability:** select a filter design that can maximally suppress the DC component.

(2) **FPGA resource constraints:** based on the Xilinx Virtex-7 690T, multiplier resources are limited, and it is necessary to ensure that sufficient resour···

···sources are used for other logic.

Based on the selective-filter method, this paper systematically evaluated the performance of filters of orders 4–30. As shown in Fig. 4, the filters that can achieve a filtering depth of more than 50 dB are those of orders 5, 10, 15, and 20. Moreover, the passband at the operating point of a higher-order filter is narrower, which is conducive to filtering out oscillatory signals unrelated to feedback. Therefore, this paper takes order 20 as the optimal order.

Fig. 4 The filter' s ability to suppress DC components

The 20th-order filter selected in this paper, while satisfying the performance requirements, also takes into account small-range drift of the operating point.

The amplitude-frequency response and phase-frequency response of the 20th-order filters designed by the two methods are shown in Fig. 5. Both can meet the requirements of suppressing the DC component and detecting a 90° phase shift in the signal; their difference lies in the position of the amplitude-frequency response under the condition of satisfying the 90° phase shift.

(a) The filter designed by the TDLSF method

(b) The filter designed by the selective waveform filtering method

Fig. 5 The filters designed by the TDLSF method and the selective wave filtering method

For the TDLSF method, the fractional part of the operating point, 0.43, is located at the maximum of the gain curve, with a magnitude of 26.00 dB. Within the acceptable range of operating-point drift, the passband is relatively smooth and can provide the same gain, so the gain of the output signal can remain unchanged. In addition, this method can actively set multiple parameters, such as the phase and gain at the operating point, to obtain 20 independent coefficients, which helps adjust the output-gain matching of the feedback system.

For the selective-filter method, the fractional part of the operating point, 0.43, is located on the descending segment of the gain curve, with a magnitude of 13.11 dB, which is smaller than that of the TDLSF method. The smoothness of the passband near the operating point is inferior to that of the former; when the operating point drifts, the output gain must be readjusted. Moreover, this method is generated by a fixed formula,

Its frequency response has a fixed shape determined by the sinusoidal sequence itself; it can only passively accept the gain at the target tune and is not conducive to adjusting the output-gain matching of the feedback system.

After comparing the two, we use the 20th-order filter designed by the TDLSF method as the filter for the transverse feedback system.

The measured amplitude–frequency response curve of the filter is shown in Fig. 6. The figure expands the amplitude–frequency response curve near the 159th harmonic frequency, which can filter out the revolution frequency of 200.678 MHz and extract the working-point frequency in the Y direction.

Fig. 6 Amplitude–frequency response curve of the electronics
Fig.6 Amplitude–frequency response of digital electronics

2 Measurement of Transverse-Oscillation Suppression

The suppression effect of the transverse feedback system on beam transverse oscillations can be directly quantified by the damping time. After gain-matching adjustment of the output correction signal, the self-developed feedback system acts on the kicker through a power amplifier to suppress the transverse oscillation of the bunch. When debugging the feedback system, the FMC212 functional module needs to be connected to a clock signal and a trigger signal, as shown in Fig. 7. An analog phase shifter is used to realize fine adjustment of the clock-signal phase, so that the peak value of the transverse oscillation signal can be accurately sampled and obtained. At the same time, the output signal of this functional module must be adjusted to match the system gain, that is, the amplitude of the output signal must be adjusted: if the gain is too small,

the correction force provided by the kicker is insufficient to suppress the oscillation; if the gain is too large, noise will saturate the amplifier and instead excite beam oscillations. When measuring the damping time, data from the Libera electronics were used. The natural damping time without the feedback system and the total damping time with the feedback system were measured separately, and the damping time of the feedback system was then calculated according to formula (1).

Fig. 7 FMC212 Signal Connection Diagram

The damping-time calculation formula is:

$$\tau_{FB} = \frac{\tau_0 \times \tau}{\tau_0 - \tau} \tag{1}$$

Here, τ_{FB} denotes the system damping time; τ denotes the damping time measured after the feedback system is turned on; and τ_0 denotes the natural damping time.

Figure 8(a) shows the test results for a single bunch at a beam current of 5.7 mA. The injection kicker excites the beam to generate oscillations. The blue curve is the multi-turn data, the red curve represents the raw data after the DC component has been removed, and the green curve is the portion of the data used for curve fitting. The fitting formula is:

$$y = ae^{-\frac{x}{\tau}} + c \tag{2}$$

where a is the curve-fitting amplitude, representing the amplitude of the beam-current signal; τ is the damping time; and c is noise.

The fitting curve in Matlab is shown in Fig. 8(b). After fitting, the natural damping time τ_0 is obtained as 13.06 ms.

(a) Beam oscillation data

(b) Fitting curve of data

Fig. 8 Natural damping time measurement

After the feedback system is turned on, the injection kicker is used to excite the beam. The test results are shown in Fig. 9. At this time, the measured system damping time τ is 0.28 ms. Substituting into Eq. (1) gives $\tau_{FB} = 0.29$ ms, indicating that the system provides effective damping capability.

(a) Beam oscillation data

(b) Fitting curve of data

Figure 8 Damping time measurement with feedback system on
Fig.9 Damping time measurement with feedback system on

Tests were carried out in the multi-bunch injection mode of the BEPCII storage ring. Under operating conditions of 82 bunches and a beam current of 100 mA, repeated measurements were performed with the self-developed feedback system switched on. The representative single measurement result in Fig. 10(a) and the statistical results of repeated measurements in Fig. 10(b) show that the system can achieve a stable damping time of $\tau_{FB} = 0.31 \pm 0.03$ ms. Here, 0.03 ms is the range of the experimental results under multi-bunch testing after removing the maximum and minimum values, demonstrating the stability and reliability of the system performance.

(a) Beam oscillation data

(b) Statistical results

Figure 10 Statistics of repeated damping-time measurements
Fig.10 Statistics of damping time

The repeated measurement results consistently show that the independently developed digital transverse feedback system can effectively suppress transverse beam oscillations in the BEPCII storage ring. The damping time is approximately 0.31 ms, better than the design target of 0.5 ms. In addition, comparative experiments with the feedback system switched on and off were performed at a beam current of 100 mA. When the feedback system was turned off, the beam was lost; when the feedback system was turned on, the beam could operate stably, ensuring stable operation of BEPCII in high-current multi-bunch mode.

3 Discussion

The bunch-by-bunch feedback system studied in this paper demonstrates that, in terms of hardware, the use of general commercial boards—Vadatech AMC725, AMC516, and FMC212—together with a filter algorithm can suppress transverse instabilities in BEPCII; in terms of the algorithm, the TDLSF algorithm was successfully verified on BEPCII.

practicality; stable operation of a 20th-order FIR filter in the FPGA balances resource consumption and processing latency. This has accumulated experience in IP-core development for future feedback requirements that are higher-order and more complex. As introduced in the introduction, the damping time of comparable international systems is about 0.5 ms; the 0.31 ms damping time of this system has reached the same international level. Subsequent work will carry out debugging and performance verification of the horizontal feedback system, complete two-dimensional closed-loop feedback operation, and evaluate its effect on improving overall beam-current stability.

4 Conclusion

Based on a commercial MicroTCA hardware platform and a self-developed FPGA processing architecture, a digital transverse bunch-by-bunch feedback system for BEPCII was successfully designed, and beam verification experiments were carried out, verifying the effectiveness of the vertical feedback. The system uses a 20th-order FIR filter and completes real-time processing of beam signals in the FPGA. The experimental results show that the system can significantly suppress transverse coupled-bunch instabilities during multi-bunch operation and achieves the design goal of a damping time of less than 0.5 ms.

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Note: Figure translations are in progress. See original paper for figures.