ChinaRxiv 中X

AI translation · View original & related papers at
chinarxiv.org/items/chinaxiv-202603.00134

Comparative Study of Single-Event Leakage Current Effects in Double-Trench and Asymmetric-Trench SiC MOSFETs Under84Kr Heavy-Ion Irradiation

Authors: Chen, Dr. De-xin, Wang, Dr. Ying, Huang, Dr. Huo-Lin, Song, Dr. Yan-Xing, Cao, Dr. Fei, Wang, Dr. Ying

Date: 2026-03-24T18:13:08+00:00

Abstract

To clarify the degradation mechanism of leakage current in trench-type silicon carbide power devices, this study conducted 84Kr ion irradiation experiments and TCAD simulations on double-trench MOSFET (DT-MOSFET) and asymmetric-trench MOSFET (AT-MOSFET) devices. The results indicate that the degradation of drain-source current is primarily attributed to the shift in the subthreshold characteristic curve caused by irradiation-induced trapped charges. Meanwhile, the increase in gate leakage current originates from gate oxide damage induced by the high electric field effect at the moment of ion incidence. Using the midgap voltage method to quantify trapped charges, it was found that the AT-MOSFET, due to its asymmetric structure and gate oxide process, exhibits less charge accumulation and thus superior resistance to leakage degradation. Furthermore, the excessively strong electric field in the source trench oxide layer of the DT-MOSFET creates an additional leakage path independent of the gate. This study clarifies the distinct failure mechanisms of the two trench devices, providing critical theoretical support for the radiation-hardened design of future trench-type power devices.

Full Text

Preamble

Comparative Study of Single-Event Leakage Current Effects in Double-Trench and Asymmetric-Trench SiC MOSFETs Under Kr Heavy-Ion Irradiation De-Xin Chen, Ying Wang, Huo-Lin Huang, Yan-Xing Song, and Fei Cao 1 School of Information Science and Technology, Dalian Maritime University, Dalian

116026, China School of Optoelectronic Engineering and Instrumentation Science, Dalian University of Technology, Dalian 116024, China To clarify the degradation mechanism of leakage current in trench-type silicon carbide power devices, this study conducted Kr ion irradiation experiments and TCAD simulations on double-trench MOSFET (DT- MOSFET) and asymmetric-trench MOSFET (AT-MOSFET) devices. The results indicate that the degrada- tion of drain-source current is primarily attributed to the shift in the subthreshold characteristic curve caused by irradiation-induced trapped charges. Meanwhile, the increase in gate leakage current originates from gate oxide damage induced by the high electric field effect at the moment of ion incidence. Using the midgap volt- age method to quantify trapped charges, it was found that the AT-MOSFET, due to its asymmetric structure and gate oxide process, exhibits less charge accumulation and thus superior resistance to leakage degradation.

Furthermore, the excessively strong electric field in the source trench oxide layer of the DT-MOSFET creates an additional leakage path independent of the gate. This study clarifies the distinct failure mechanisms of the two trench devices, providing critical theoretical support for the radiation-hardened design of future trench-type power devices.

Keywords

Heavy-Ion Irradiation, Single-event leakage current (SELC), Silicon carbide (SiC), Radiation protection, Double trench MOSFET (DT-MOSFET), Asymmetric-trench MOSFET (AT-MOSFET)

INTRODUCTION

Silicon carbide (SiC) power MOSFETs have become core components for enhancing the efficiency and power density of aerospace power systems due to their low conduction and switching losses [ ]. With the continuous advancement of fabrication processes, various commercial SiC products, such as planar-gate (VDMOSFET) and trench-gate (UMOS- FET) devices, have been successively introduced. Trench- gate MOSFETs, in particular, by embedding the gate within

the substrate to form a vertical channel structure, significantly 10

reduce on-resistance and parasitic capacitance. When em-

ployed in aerospace electronic equipment, they help improve 12

switching speed and reduce energy consumption, thereby supporting high-frequency, high-efficiency, and low-loss sys- tem operation [ ]. However, the high-energy particle ra- diation environment in space can induce device performance

degradation, posing significant challenges to the long-term re- 17

liable operation of spacecraft [ ]. In practical applications, although derating

designs are commonly implemented to mit- igate radiation effects—keeping operating voltages below the thresholds that trigger Single Event Gate Rupture (SEGR) or Single Event Burnout (SEB)—the Single Event Leakage Cur- rent (SELC) effect remains difficult to avoid [ ]. This effect leads to a continuous increase in leakage current after

irradiation, severely constraining the reliable application of 25

SiC power MOSFETs in the aerospace field.

Research on the degradation mechanism of leakage cur- 27

rent in SiC MOSFETs can currently be summarized into the

This work was supported in part by National R&D Program for Ma- jor Research Instruments of China (Grant No. 62027814) and in part by Basic Research Development Program of Liaoning Province of China (2022JH2/101300266).

following three aspects: 1. Multiple studies [ ] have conducted experiments on VDMOS devices using various ra- diation particles and identified that defects in the gate oxide structure within the JFET region are the primary cause of gate oxide damage. This conclusion has been further validated by transmission electron microscopy analyses in]. 2.

A comparative study [ ] analyzing simultaneous radiation experiments on PiN diodes and VDMOS devices observed Single Event Leakage Current degradation in both, indicating

that damage to the P-N junction is also a significant factor in- 38

ducing leakage degradation. 3. References [ ] observed that the subthreshold characteristics of the devices exhibited

significant degradation, causing difficulties in turning off the 41

devices properly and consequently leading to an increase in drain-source current. This phenomenon exhibits similarities

to the total ionizing dose (TID) effect [22 , 23]. Notably, the 44

aforementioned studies have primarily focused on the VD- MOSFET structure. It has been suggested that UMOSFETs, which offer superior electrical performance, possess greater resilience against Single Event Leakage Current degradation]. However, systematic investigations into their leakage

degradation mechanisms remain scarce. Therefore, an in- 50

depth exploration of the leakage degradation mechanisms 51

in UMOSFET devices, which exhibit superior performance,

holds significant research importance and application value 53

for enhancing the reliability of aerospace electronic systems. 54

In this study, single-event irradiation experiments were conducted on double-trench MOSFETs (DT-MOSFETs) and asymmetric trench MOSFETs (AT-MOSFETs) using

ions. By monitoring real-time current variations during irra- 58

diation and comparing electrical characteristics before and af- ter irradiation, the following key phenomena were observed:

the DT-MOSFET exhibited significant source-drain current 61

degradation at an irradiation bias as low as

20 V

, whereas the AT-MOSFET showed similar degradation only when the

bias was increased to 100 V. Under higher irradiation bi- ases, gate leakage current degradation occurred in both de-

vice types. Based on this, by combining subthreshold char- 66

acteristic measurements with the midgap voltage method, the amount of irradiation-induced trapped charge was quantita- tively extracted, confirming that such defect charge is the pri- mary factor responsible for source-drain current degradation.

The AT-MOSFET, owing to its asymmetric structure and opti- mized gate oxide process, accumulated fewer trapped charges and thus demonstrated superior resilience to leakage degra- dation. TCAD single-event radiation simulations further con- firmed that an excessively high electric field in the oxide layer is the key cause of gate oxide damage and gate leakage cur-

rent degradation. In addition, due to the unique double-trench 77

structure of the DT-MOSFET, the local electric field in the source trench oxide layer becomes excessively strong, creat- ing an additional leakage path indepen- dent of the gate.

EXPERIMENTAL DETAILS irradiation experiments conducted Space Environment Simulation and Research Infrastructure (SESRI) [ ], as illustrated in Fig.

Kr ions were used as the radiation source, with an effective energy of 449.2 MeV and a linear energy transfer (LET) value of 37.9 MeV • cm /mg. The irradiation direction was perpendicular to the device surface, and the beam spot covered an area of , which was sufficient to cover and penetrate the active region of the devices. The average flux of Kr ions was 1.64 , and the maximum irradiation fluence was set at 1.64 (corresponding to an irradia- tion time of 100 s). c illustrate the schematic cross-sections of the double-trench silicon carbide MOSFET and the asym- metric trench silicon carbide MOSFET, respectively. The DT-

MOSFET employs a unique source trench structure to allevi- 97

ate the electric field concentration in the gate oxide, whereas the AT-MOSFET achieves a similar effect through an asym- metric trench design [ ]. Both devices feature a break- down voltage of 1200 V, providing a sound basis for comparatively investigating the changes in electrical characteristics before and after irradiation, evaluating their radiation toler-

ance, and revealing the underlying degradation mechanisms. 104

The irradiation tests consisted of two components: real-

time monitoring of leakage current during single-event 106

strikes, and comparative measurements of electrical charac-

teristics before and after irradiation. Real-time monitoring 108

was performed using a transient current measurement system, which continuously recorded the reverse leakage current (I of the devices during irradiation at different drain bias volt- ages (V), with a sampling interval of 10 ms. Electrical char- acterization was conducted using a Keysight B1500A semi- conductor parameter analyzer to measure changes in transfer characteristics, drain-source leakage current (I), and gate leakage current (I) before and after irradiation, as well as to extract the evolution of the devices' capacitance character- istics. (a) Schematic illustration of the single-event irradiation experiment on trench SiC MOSFETs using Kr ions;(b) Cross- sectional structure of the DT-MOSFET;(c) Cross-sectional structure of the AT-MOSFET.

EXPERIMENTAL RESULTS The experimental results of leakage current variations dur- ing single-ion incidence are presented in Fig. . Both devices exhibited periodic fluctuations in leakage current with a cy- cle of approximately 12 seconds, a phenomenon correspond- ing to the periodic particle emission pattern of the radiation

source. Comparative analysis revealed significant differences 125

in the leakage current degradation behavior between the two device types. As shown in Fig. a, the DT-MOSFET exhib- ited pronounced leakage degradation at a drain-source volt- age as low as 20 V, with the leakage current increasing to the microampere (A, 10) range and further intensifying increased. When V reached 400 V, the leakage cur- rent rose rapidly and triggered the current compliance protec- tion threshold of the measurement system. In contrast, the

AT-MOSFET showed no significant degradation within the 134

V DS range of 20-50 V, with the leakage current remaining in 135

the nanoampere (nA, 10) range. However, when V increased to 100 V, its leakage degradation behavior intensi- fied, exhibiting characteristics similar to those observed in the double-trench device under high bias conditions.

The drain-source leakage current measurement was per-

formed at V DS = 200 V and V GS = 0 V to evaluate the leak- 141

age degradation of the three terminals. As shown in Fig. during irradiation of the DT-MOSFET at drain bias voltages ranging from 20 V to 50 V, the drain-source current exhibited a rapid increasing trend, while the gate current showed no

significant change. This indicates that this phase is primarily 146

dominated by the formation of a direct conduction path from drain to source induced by radiation. However, when the ra- diation drain voltage increased to 100 V and above, the gate leakage current also increased markedly, suggesting direct damage to the gate dielectric layer. In contrast, as illustrated

in Fig. 3 [FIGURE:3] b, the AT-MOSFET exhibited no significant leakage 152

increase within the radiation drain voltage range of 20-50 V.

Only when the drain voltage reached 100 V was simultaneous degradation of both drain-source and gate leakage currents observed. These phenomena indicate that irradiation-induced leakage degradation is primarily associated with the forma- tion of a direct drain-source conduction path and damage to

the gate, which directly explains the degradation mechanisms 159

underlying the leakage current increases observed in Fig.

Since the two trench devices employ asymmetric and double-trench structures, respectively, to protect the gate ox- ide region, it is difficult to directly determine whether the gate oxide sustained direct damage from Kr ion irradiation based solely on the gate current variations observed in the afore- mentioned drain-source leakage current tests. Therefore, a gate leakage current measurement was further performed by applying a gate voltage sweep from -4 V to +20 V (within the safe operating gate voltage range of the devices) to more sen- sitively characterize the degradation degree of the gate oxide.

As shown in Fig. a, for the DT-MOSFET device, no sig-

nificant degradation in gate current was observed when the 172

radiation drain voltage did not exceed 100 V. However, when the radiation drain voltage increased to 150 V, severe gate ox- ide degradation occurred. As the gate oxide bias increased, the leakage current rapidly rose to the measurement system' s protection threshold, with the degradation degree intensifying increased. In contrast, as illustrated in Fig. b, the AT- MOSFET device exhibited gate oxide degradation behavior at a radiation drain voltage as low as 100 V.

The capacitance characteristic test was further conducted to assess gate oxide damage. The drain and source terminals of the device were shorted and grounded (GND), and an AC small signal with a frequency of 1 MHz was applied to the gate, with the gate voltage swept from -15 V to 10 V. The results are shown in Fig. . The experiments indicate that for the DT-MOSFET, the

post-irradiation capacitance curve began to exhibit a negative shift at a radiation drain voltage of 200 V. When the radiation drain voltage increased to 300 V, the degree of this shift intensified. This phenomenon is attributed to gate oxide damage inducing leakage current in the device, causing the gate oxide layer to lose its ideal in- sulating properties, which in turn leads to changes in capac-

itance characteristics. It is noteworthy that although Fig. shows gate oxide damage in the double-trench device at a ra- diation drain voltage of 150 V, the capacitance curve under the corresponding conditions did not show a noticeable shift.

Analysis suggests that this may be related to the leakage cur- rent not yet reaching the critical threshold required to induce

significant changes in capacitance characteristics. When the 200

leakage current is below approximately 10 A, the gate ox- ide may still maintain a certain degree of insulating property, which is insufficient to cause an observable shift in the ca- pacitance curve. In other words, 10 A can be considered as a critical reference value for the onset of capacitance curve shift. This inference was further validated in tests on the AT- MOSFET: at a radiation drain voltage of 200 V, the leakage current did not reach the 10 A range, and the capacitance

characteristic curve showed no significant change. However, 209

when the radiation drain voltage was increased to 300 V and the leakage current exceeded this threshold, the capacitance The transfer characteristic measurements provide clearer

insight into the leakage degradation mechanisms of the two 214

devices. The tests were performed with a fixed drain bias of 0.05 V, while the gate voltage was swept from -4V to 10V. of the DT-MOSFET before and after irradiation under differ- ent irradiation bias voltages. A notable phenomenon is that the subthreshold curve of the DT-MOSFET shifts regardless

of the irradiation bias magnitude, with the shift increasing 221

as the irradiation bias rises. This directly results in a drain- source current even at a gate voltage of 0 V (off-state), thereby

explaining the increased off-state leakage observed in Fig. 2 [FIGURE:2] 224

. Furthermore, when the gate voltage is negative, the

drain-source current degrades to the order of 10 A and re- mains independent of gate voltage, indicating that in addition to the subthreshold curve shift, other degradation paths con- tribute to the leakage increase in the DT-MOSFET. Regard- ing gate current, degradation occurs when the irradiation bias reaches 150 V, consistent with the gate oxide damage obser- vations in Fig.

MOSFET. It can be observed that its subthreshold curve also undergoes degradation. However, at an irradiation bias of 50 V and a gate voltage of 0 V, the device can still be prop- erly turned off without leakage degradation, which directly

explains the absence of significant off-state leakage degrada- 238

tion in the asymmetric trench device observed in Fig. . Unlike the DT-MOSFET, the AT-MOSFET does not ex- hibit other degradation paths. Its gate current degradation oc- curs at an irradiation bias of 100 V, consistent with the results shown in Fig.

DISCUSSION

Based on the systematic testing and analysis of the elec- trical characteristics of DT-MOSFET and AT-MOSFET, it can be concluded that subthreshold curve shift is the pri-

mary mechanism responsible for drain-source current degra- 248

dation in both trench devices, while gate oxide damage is the dominant factor inducing gate leakage current degradation.

The differences in degradation behavior between the two de-

vices mainly stem from variations in the magnitude of the 252

subthreshold curve shift and the extent of gate oxide dam- age. Additionally, the DT-MOSFET exhibits an additional drain-source current degradation path, making its degrada-

tion mechanism more complex than that of the AT-MOSFET. 256

This chapter will further elucidate the intrinsic mechanisms 257

of leakage current degradation induced by Kr ion irradia-

tion by combining experimental measurements with TCAD 259

simulations. Subthreshold characteristic shift is typically attributed to radiation-induced oxide trapped charges and interface state charges. During the penetration of Kr ions through the gate oxide layer, the high-energy particles deposit energy and gen- erate electron-hole pairs. Within the oxide layer, electrons rapidly drift toward the gate under the influence of the electric field, while holes migrate toward the SiC substrate. Some holes are captured by deep-level traps when migrating to the /SiC interface, forming positively charged oxide trapped charges, which consequently induce a shift in the subthresh- old curve. Furthermore, irradiation may also increase the interface state density within the SiC bandgap, further affecting the subthreshold characteristics.

To quantitatively distinguish the effects of oxide trapped charges from interface state charges, this study employs the midgap voltage method for their separation [ ]. This method is based on the subthreshold current expression. By extracting parameters such as threshold voltage and mobility,

and combining them with the device structural parameters, 279

the midgap current is calculated, thereby obtaining the corre- 280

MOSFET; (b) AT-MOSFET. sponding midgap voltage. For a MOSFET, the drain-source current in the linear region can be expressed as:

I ds = (W

where W/L represents the channel width-to-length ratio,

and C OX is the gate oxide capacitance per unit area. By substi- 285

tuting two sets of experimentally measured I and V ues, the threshold voltage V and mobility can be solved simultaneously. Substituting the obtained parameters into the subthreshold current formula:

I ds = µ (W

where N is the channel doping concentration, N is the in- trinsic carrier concentration, and the constants and surface potential are given by the following equations:

$\alpha = 2$ ϵ SiC ϵ OX

$\alpha = \phi$ b = (kT

Where L is the Debye length, d is the gate oxide thick- ness, and are the dielectric constants of SiC and SiO ,respectively. Substituting the above parameters into Equ. ( ), the midgap current value I can be calculated. For the DT-MOSFET and AT-MOSFET, the calculated I ues are 5.86*10 A and 5.52*10 A, respectively, which are closely matched. Due to the extremely low intrinsic carrier concentration in SiC, the midgap current is exceptionally small; therefore, the corresponding midgap voltage cannot be directly read from the measured curve. It can only be approx- imated by extending the subthreshold I-V characteristic curve to this current level to obtain the voltage point, as illustrated in Fig. . Although this method inevitably introduces some deviation, it helps ensure relative accuracy in the separation results under the given constraints.

Based on the aforementioned method, the midgap volt- age and threshold voltage of the devices before and after irradiation can be extracted, respectively. Experimental re- sults reveal that after Kr ion irradiation, the threshold voltage of both devices remains essentially unchanged, while the midgap voltage exhibits a noticeable shift. This phenomenon indicates that irradiation primarily induces changes in the two types of trap charges, with a relatively minor effect on the threshold voltage, reflecting the distinctive degradation char- acteristics under single-event effects. The voltage shift caused by oxide trapped charges

and the voltage shift induced by interface state charges can be separated using the following equations:

$\Delta V_{ot} = \Delta V_{mg} = V_{mg2} - V_{mg1}$ (5) 325

$\Delta V_{it} = (V_{th2} - V_{th1}) - (V_{mg2} - V_{mg1})$ (6) 327

As shown in Fig. a, due to the essentially unchanged thresh- old voltage, ex- hibit an approximately inverse relationship. The corresponding changes in trap charge con- centration can be further calculated as follows:

$\Delta N_{ot} = C_{OX} \cdot \Delta V_{ot} / q$ (7) 332

$\Delta N_{it} = C_{OX} \cdot \Delta V_{it} / q$ (8) 334

the two devices under different irradiation biases. As can be observed, with increasing irradiation bias, the concentra- tions of both types of trap charges gradually increase and tend to saturate. This trend aligns with the progressively di-

minishing shift of the subthreshold curve. A comparison be- 340

tween the two devices reveals that the AT-MOSFET exhibits

significantly lower trap charge concentrations than the DT- 342

MOSFET under all irradiation bias conditions, demonstrating

) for DT-MOSFET and AT-MOSFET, along with the corresponding oxide trapped charge component ( ) and interface state charge component) as functions of irradiation bias voltage; (b) Oxide trapped charge concentration (N) and interface state charge concentration (N functions of irradiation bias voltage.

Simulated subthreshold characteristics reconstructed using the extracted trap charge concentrations: (a) DT-MOSFET; (b) AT- MOSFET. superior radiation tolerance. This also explains why the AT-

MOSFET showed no significant leakage degradation under 345

irradiation biases of 20-50 V—its subthreshold curve shift is relatively small, allowing the device to maintain normal turn- off characteristics.

The superior radiation tolerance of the AT-MOSFET pri- marily stems from two factors: First, its gate oxide fabrica- tion process is more advanced, resulting in fewer irradiation- induced oxide trapped charges. Second, its asymmetric trench structure forms a conductive channel on only one side, effec- tively reducing the total amount of trap charges affected by irradiation compared to the double-trench device.

To verify the accuracy of the total trap charge concentra- tions extracted using the midgap voltage method, this study employed the Sentaurus TCAD simulation platform. The trap charge concentrations quantified in Fig. b were used as in- put parameters to simulate the subthreshold characteristics of the devices after irradiation, and the results were compared with experimental data. The

simulation models for the DT- MOSFET and AT-MOSFET had been calibrated in previous studies] and demonstrated high reliability. As shown in Fig. , after incorporating the trap charges extracted by the midgap voltage method, the simulated subthreshold char- acteristics were consistent with the experimental results pre- sented in Fig. . This indicates that irradiation-induced trap charge accumulation is the direct cause of drain-source cur- rent degradation. It is worth noting, however, that the simu- lation results also show that the introduction of trap charges alone cannot reproduce the leakage degradation observed in the DT-MOSFET in the negative gate voltage region. This

suggests that the degradation mechanism of this device in- 374

volves other, more complex physical mechanisms that war- 375

rant further investigation. In addition to the degradation of drain-source current, the results in Fig. also indicate that irradiation leads to the degradation of gate leakage current.

We first consid-

Kr ions under different bias conditions: (a) DT- MOSFET; (b) AT-MOSFET. ered whether this degradation could be attributed to trap- assisted tunneling effects induced by the introduction of trap charges. However, TCAD simulation results suggest that the trap charge concentrations extracted from Fig. b are insuf-

ficient to generate significant trap-assisted tunneling current. 384

Therefore, the dominant mechanism underlying gate leakage 385

degradation is more likely attributable to gate oxide damage induced by the high electric field during irradiation, which subsequently enhances Fowler-Nordheim (FN) tunneling or direct tunneling (DT) effects [

To gain a deeper understanding of the damage mechanisms 390

in the gate oxide of the two devices induced by Kr ion ir- radiation, this study employed Sentaurus TCAD to simulate the single-event irradiation process in both DT-MOSFET and AT-MOSFET structures [ ]. To accurately model the radiation response of silicon carbide devices, various physi- cal models were incorporated into the simulations, including doping concentration- and temperature-dependent Shockley- Read-Hall (SRH) recombination models, Auger recombina- tion models, and, given that the single-event burnout process

involves electron-hole pair generation through impact ioniza- 400

tion, impact ionization models were also considered [34]. In 401

the single-event burnout simulation, the number of electron-

hole pairs generated per unit volume along the ion incidence 403

path is defined by Equ. (

G (l, w, t) = LET · exp − w w t (l)

1 + erf

where LET represents the linear energy transfer (in units of 406

MeV · cm /mg), w denotes the ion track radius, w is the lat-

eral position of ion incidence, t 0 is the initial charge genera- 408

tion time (in seconds), s characterizes the eigenvalue of the Gaussian function for the charge generation time distribution (in seconds), and t is the simulation time (in seconds). The specific parameter values used in the simulations are detailed in Table SIMULATION

Parameter Value LET (MeV · cm 2 /mg) 37.9 Track Radius w t (µ m) 0.05 Initial Charge Generation Tim t 0 (s) 4 × 10 − 12

The irradiation simulation was performed by analyzing the peak electric field location in the bottom gate oxide at the moment of ion incidence. Fig. illustrates the horizontal distribution of the gate oxide electric field for both devices when an ion strikes vertically at the center of the bottom gate oxide. As shown in Fig. a, under Kr ion irradiation, the gate oxide electric field in the DT-MOSFET approaches ap- around 150 V. In contrast, Fig. b reveals that for the AT-MOSFET, the gate oxide electric field already reaches this same critical field strength at an irradiation bias of 100 V.

Such an electric field level is sufficient to induce gate oxide damage, consequently leading to the degradation of gate leak- age current, a phenomenon consistent with the experimental

The primary mechanism by which ion irradiation induces 429

a high electric field in the gate oxide can be explained as follows: When a high-energy ion strikes the silicon carbide drift region, it generates a dense track of electron-hole pairs along its path, effectively forming a transient low-resistance path between the drain and the gate. The formation of this path causes the drain voltage, originally distributed across the drift region, to be increasingly applied across the gate oxide

layer instead, leading to a significant rise in the electric field 437

strength within the gate oxide. As the drain-source voltage gate oxide intensifies further, ultimately resulting in gate ox- ide damage. Fig. a-d illustrates the evolution of the gate oxide electric field distribution for both devices under differ- ent irradiation biases, providing a visual representation of this process.

Kr ions under different bias conditions: (a-b) DT-MOSFET; (c-d) AT-MOSFET.

Kr ion irradiation under different bias conditions.

Due to its unique double-trench structure, the DT- 445

MOSFET achieves source contact through a deep trench.

Compared to the bottom of the gate oxide, the source trench has a greater depth and can effectively shield the electric field under high drain voltage, thereby providing protection for the gate oxide. However, single-event strikes are random, and it is possible for ions to strike along the source trench region, potentially causing damage to the oxide layer in that region and forming a leakage path originating from the source.

As shown in Fig. , at an irradiation bias of 50 V, the elec- tric field in the oxide layer at the bottom of the source trench can already exceed 3 MV/cm, reaching the damage thresh- old. This explains the phenomenon observed in Fig. : under an irradiation bias of 50 V and negative gate voltage condi-

tions, the DT-MOSFET still exhibits significant source-drain 459

current, and this current remains largely independent of gate voltage. This occurs because the leakage current path origi- nates from oxide damage in the source trench and is unrelated to the gate; therefore, the gate voltage has a weak modulating effect on it.

SUMMARY

In summary, this paper systematically compares and in- vestigates the radiation-induced leakage degradation mech-

anisms of two types of silicon carbide power MOSFETs, 468

namely DT-MOSFET and AT-MOSFET, through Kr heavy ion irradiation experiments and TCAD simulations. perimental results indicate that the degradation behavior of both devices is jointly dominated by trap-charge-induced subthreshold shift and gate oxide damage caused by high electric

fields. However, significant differences exist in their degrada- 474

tion thresholds and leakage paths. The DT-MOSFET exhibits drain-source current degradation at a relatively low bias of 20 V and introduces an additional gate-independent leakage path due to an excessively high electric field in the source trench oxide layer. In contrast, the AT-MOSFET, benefiting from its asymmetric structure and superior gate oxide pro- cess, accumulates fewer trapped charges, exhibits a higher degradation threshold of 100 V, and shows no additional leak- age path interference, demonstrating enhanced radiation tolerance. Based on the comparative analysis of failure mecha-

nisms, this paper proposes the following three approaches for 485

radiation-hardening design: 486

ity of the gate oxide layer to reduce process-induced de- fect charges, thereby lowering the trap charge density at the source. the saturation characteristic of the subthreshold shift by ap-

propriately increasing the initial threshold voltage of the de- 493

vice to ensure reliable turn-off capability even after irradia- tion.

Structure: Focus on enhancing the radiation tolerance of the bottom gate oxide layer and explore novel trench shielding structures to mitigate the threat posed by high electric fields, generated by radiation-induced carriers, to gate oxide relia- bility.

Acknowledgements: The authors would like to express special thanks to Space Environment Simulation Research In- frastructure of Harbin Institute of Technology.

Metzger, Henschel, Sili- carbide radiation detector harsh environ- ments.

Trans. (2002). J. Ebersberger, M. Hagedorn, M. Lorenz et al., oten- tials Comparison Inverter Topologies All-Electric Aircraft Propulsion.

Emerg- ing Sel. Top. Power Electron. 5264–5279 (2022).

C. Farnell, A. Corbitt, W.G. Schwartz et al., Develop- ment, Integration, and Flight Testing of a Silicon Carbide Propulsion Drive for a Hybrid Electric Aerospace Applica- tion. IEEE Trans. Power Electron. , 18437–18447 (2025).

A. Oraon, S. Shreya, R. Kumari et al., A double trench 4H −SiC MOSFET as an enhanced model of SiC UMOSFET, in 2017 7th International Symposium on Embedded Com- puting and System Design (ISED) (Durgapur,2017), pp. 1-5.

L. Wang, Y. Jia, X. Zhou et al., Heavy-ion induced gate damage and thermal destruction in double-trench SiC MOSFETs. Microelectron. Reliab. 114770 (2022). ence on multiple-cell upsets in small sensitive volumes: from standard to high energies. Nucl. Sci. Tech. , 85 (2024).

Q. Sun, B. Liang, Y. Chi et al., Quantitative investiga- tion of well contact impact on single-event transient in sub- 20 nm FinFET process. Nucl. Sci. Tech. , 54 (2026).

Peng, Zhang Mono-Energetic Proton Induced Damages Power MOSFETs.

IEEE Trans. Device Mater. Reliab. 64–71 (2026). C. Martinella, T. Ziemann, R. Stark et al., Heavy-Ion Mi-

crobeam Studies of Single-Event Leakage Current Mechanism 541

, 1381–1389 (2020). P.P. Hu, L.J. Xu, J.S. X. Zhang et al., Failure mecha-

nisms of AlGaN/GaN HEMTs irradiated by high-energy heavy 545

ions with and without bias. Nucl. Sci. Tech. , 13 (2025).

L. K. Liu, Z. L. Liu, L. Wu et al., Drain-Leakage Degradation During Single-Event Burnout Experi- ments N-Channel Power VDMOS Transistors.

IEEE Trans. Electron Devices. 4906–4913 (2024). M. Luo, Y. Zhang, Y. Wang et al., Investigation of Heavy- Ions-Induced Leakage Current Modes and Degradation Mech-

anism in SiC MOSFETs Under Complex Heavy Ion Condi- 555

tions. IEEE Trans. Electron Devices. , 6573–6580 (2024).

X. Zhou, H. Pang, Y. Jia et al., Gate Oxide Dam- MOSFETs Induced Heavy-Ion Strike.

IEEE Trans. Electron Devices. 4010–4015 (2021). M. Ji, N. Ren, Y. Li et al., Influence of JFET Re- gion on Heavy-Ion-Induced Gate Damage in SiC Power , 1726–1733 (2025).

Y. Wang, J. Tao, Y. Zhong et al., Experimental Investiga-

tion and Hardening of Single-Event Gate Rupture in 100-V 567

, 71–79 (2024). Y. Xiao, C. Liu, J. Zhou et al., Microstructural Evolution of Gate Oxide in SiC Power MOSFETs Under Heavy-Ion Irradi- ation. IEEE Trans. Device Mater. Reliab. , 189–194 (2025).

L. Wu, F. Liu, S. Dong et al., Analysis of Single-Event Leak- age Current Degradation Induced by Heavy-Ion Irradiation in SiC MOSFETs. IEEE Trans. Electron Devices. , 3489–3496 (2025).

Y. Xiao, C. Liu, J. Zhou et al., SiC Damage Induced by Heavy Ion Irradiation and Post-Gate Stress in SiC MOS- FETs. IEEE Trans. Device Mater. Reliab. , 189–194 (2025).

L. Qiu, Y. Bai, J. Ding et al., Microstructure Damage for Single-Event Leakage Current II in SiC MOSFETs Induced by Heavy Ion. IEEE Trans. Electron Devices. , 2233–2239 (2025).

Z. Chen, J. Xu, Z. Lei et al., Microdose Effect of SGT MOSFETs induced Heavy Ions, ternational Conference Radiation Effects Elec-

tronic Devices (ICREED) (Kunming,2023), pp. 1-4. 589

Degradation Under Low Drain Bias Induced by Heavy Ion in SiC MOS- FETs.

Trans. (2024). Wang, Effects total-dose irradiation on the threshold voltage of H-gate SOI NMOS devices. Nucl. Sci. Tech. 117 (2016).

S.F. O. Abubakkar, N.F. Zabah, Y. Abdullah et al., Effects of electron radiation on commercial power MOSFET with buck converter application. Nucl. Sci. Tech. , 31 (2017).

X. Dong, M. Huang, Y. Ma et al., Study on Differ- ences in Single-Event Leakage Current of Planar-Gate Asymmetric Trench-Gate MOSFETs, 37th International Symposium on Power Semiconductor De- vices and ICs (ISPSD) (Kumamoto,2025), pp. 485-488.

L.W. Yao, J.H. Yang, Y.Z. Liu et al., Back-gate bias and sup- ply voltage dependency on the single-event upset susceptibil- ity of 6 T CSOI-SRAM. Nucl. Sci. Tech. , 164 (2025).

J.H. Lee, E.G. Kang, A Study on the Electrical Prop- erties Voltage Power MOS-FET Double Trench Structures, Work- Bandgap Power Devices Applica- tions (WiPDA Asia) (Hsinchu,2023), et al., Reliability Compari- son of Commercial Planar and Trench 4H-SiC Power MOSFETs, International Reliability Physics Symposium (IRPS) (Monterey,2023), Schwank, Fleetwood, Shaneyfelt et al., A critical comparison of charge-pumping, dual-

transistor, and midgap measurement techniques (MOS tran- 626

1666–1677 (2024).

[29] B. Djezzar, H. Tahi, A. Mokrani, Why Is Oxide- 629

Charge-Pumping

Method

Appropriate Radiation-Induced Depiction MOSFET? Trans.

Device Mater. Reliab. (2009). Chen, Wang, voltage-

dependent mechanisms of single-event leakage current in 635

SiC trench MOSFETs: Heavy-Ion irradiation and TCAD simulation study.

Nucl. Technol. (2025). Z. Zhang, H. Yuan, K. Liu et al., New Gate Leakage

Degradation Behavior and Mechanism Induced by Heavy- 640

Ion Irradiation in High-Voltage Silicon Carbide MOSFETs.

IEEE Trans. Electron Devices. 5524–5530 (2025). Z.G. Zhang, Y. Huang, Y.F. En et al., Investigation of maximum proton energy for qualified ground-based evaluation of single event effects in SRAM devices. Nucl. Sci. Tech. , 47 (2019).

[33] B.C. Wang, C.X. Tang, M.T. Qiu, A machine learning approach 648

to TCAD model calibration for MOSFET. Nucl. Sci. Tech. 192 (2023).

S. Selberherr, Analysis and Simulation of Semiconductor De- vices. New York, NY, USA: Springer-Verlage. 80–120 (1984). 10.1007/978-3-7091-8752-4 S.A. Iakovlev, V.S. Anashin, P.A. Chubunov, et al., MOSFETs SEB & SEGR Qualification Results with SOA Estimation, in 2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS) (Geneva,2017), pp.

D.X. Chen, Y. Wang, H.L. Huang et al., Hardened design and practical effect of 60 V trench MOSFET resistant to irradiation.

Figure 11

Figure 1: Figure 11

Nucl. Sci. Tech. , 61 (2026). X. Deng, H. Zhu, X. Tong et al., Investigation and Failure Mode of Asymmetric and Double Trench SiC mosfets Under Avalanche Conditions. IEEE Trans. Power Electron. , 8524–8531 (2020).

Figures

Source: ChinaXiv —Machine translation. Verify with original.