Impact of incident direction on atmosphere neutron-induced single event upset in 128-layer dual-deck 3D NAND flash memories

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Abstract

Based on the meV-GeV wide-energy neutron beam from the China Spallation Neutron Source (CSNS), this study investigates the direction dependence of single-event upsets (SEUs) in 128-layer dual-deck CT 3D NAND Flash memories. Irradiation tests were performed from the front, side, and back of the chip. By mapping SEU addresses into 3D distributions, multiple-cell upset (MCU) patterns and formation mechanisms were analyzed. Results show the front direction is the "worst case", with SEU cross-section 27.3% higher and MCU count 52.5% greater than side/back incidence. MCUs are mainly double-bit upsets(DBUs), with a maximum size of 7 bits, and primarily exhibit "string-like" patterns along through-holes, along with some L-shaped distributions along word lines(WL). Neutron transport simulations further reveal that secondary particles in the sensitive region are predominantly nitrogen and silicon ions; side and back incidence additionally yields minor high-Z species (Er, Yb, Ta, Lu, W) owing to tungsten layers. The frontal incidence produces 13.77% of secondary particles with LET > 5 MeV $\bullet$ cm^2 $\bullet$ mg^{-1}, markedly higher than side (4.87%) and back (9.96%) incidence. This explains the elevated SEU cross-section for frontal incidence and the experimentally observed directional sensitivity variation. The work clarifies the directional dependence of atmospheric neutron sensitivity in CT 3D NAND Flash, supporting accurate reliability prediction and radiation-hardening design.

Full Text

Preamble

Impact of incident direction on atmosphere neutron-induced single event upset in 128-layer dual-deck 3D NAND flash memories Hong-De Li1,2 Hong Zhang1

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Irradiation tests were performed from the front, side, and back of the chip. By mapping SEU addresses into 3D distributions, multiple-cell upset (MCU) patterns and formation mechanisms were analyzed. Results show the front direction is the "worst case", with SEU cross-section 27.3% higher and MCU count 52.5% greater than side/back incidence. MCUs are mainly double-bit upsets(DBUs), with a maximum size of 7 bits, and primarily exhibit "string-like" patterns along through-holes, along with some L-shaped distributions along word lines(WL).

Neutron transport simulations further reveal that secondary particles in the sensitive region are predominantly nitrogen and silicon ions; side and back incidence additionally yields minor high-Z species (Er, Yb, Ta, Lu, W) owing to tungsten layers. frontal particles with LET $> 5\,\mathrm{MeV \cdot cm^2 \cdot mg^{-1}}$, markedly higher than side (4.87%) and back (9.96%) 13.77% of secondary incidence produces incidence. This explains the elevated SEU cross-section for frontal incidence and the experimentally observed directional sensitivity variation. The work clarifies the directional dependence of atmospheric neutron sensitivity in CT 3D NAND Flash, supporting accurate reliability prediction and radiation-hardening design.

Key word: Incident direction, 3D NAND Flash, Atmospheric neutron, Single-event Effects (SEE) This work was supported in part by the National Key Research and Development Program of China under Grants (No.2024YFB4303700) and (No.2023YFF0616600), the National Natural Science Foundation of China under Grant (No.U25A203277), and the National Key Laboratory Fund (No. 6142806240104).

1 Introduction

vertical density. employs limitation, architecture planar NAND technology continues to scale according to Moore' s law, key reliability metrics such as charge retention and endurance have significantly degraded[1]. To overcome stacking technology has been introduced into flash memory architectures[2]. Among these developments, charge-trapping 3D NAND flash memory cell design and vertical cylindrical substantially structure, channel increasing storage gate-all-around greatly enhances interference immunity, leading to a systematic improvement in data retention under radiation exposure[3-6].

However, charge-trapping memory cells shrinks further, electrons number representing a single bit of information decreases considerably. This reduction sharply increases sensitivity of modern flash memory to single-event Consequently, ionization compared with earlier technology nodes, contemporary experience single-event upsets induced lower ionization energy. flash memory particles with relatively effects. feature effects research been made In recent years, significant progress single-event in flash (SEE) memory devices, with multiple teams systematic conducting worldwide studies across various flash memory types[7-16]. heavy-ion Regarding irradiation, charge-trapping (CT) 3D NAND flash memory by Yang Jiao et al. analyzed the correlation between the number and size of multiple-bit upsets and the linear energy transfer (LET) of heavy ions[17]. experimental work influence examined susceptibility currently latch-up (SEL) In studies of irradiation mechanisms, M.

Bagatin et al. observed significant threshold voltage shifts in floating-gate (FG) 3D NAND flash memory under irradiation[18]. neutron atmospheric Through irradiation heavy-ion experiments, Xuesong Zheng et al. revealed single-event in the peripheral circuits of commercial CT 3D NAND flash memory [19]. Furthermore, D. Peyronel et al. investigated the sensitivity of 3D NAND flash memory to broad-spectrum neutron-induced SEE multi-chip architectures and memory management data structures on device rates[20]. To error knowledge, there reported studies on the irradiation effects of atmospheric neutrons on CT 3D NAND flash memory. With expanding application of CT 3D NAND aviation, fields automotive communications, neutron electronics, induced SEE may pose a serious threat therefore to system reliability. imperative characteristics atmospheric neutron-induced SEE in this memory technology. Moreover, as these devices are often integrated into systems with complex three-dimensional layouts and may be exposed to radiation from various angles in real operating environments, understanding the angular dependence of their neutron sensitivity reliability evaluation effective radiation-hardening design. investigate and mechanisms atmospheric accurate essential This study employs a combined experimental Carlo simulation approach to investigate the and Monte influence of different incident directions neutron-induced atmospheric single-event upsets in 128-layer CT dual-deck stacked 3D NAND flash memory. The addresses of soft errors were converted into three-dimensional spatial distribution maps to analyze the formation mechanisms of multiple-cell upsets with different physical shapes. incident direction on The impact of single-event upsets in CT 3D NAND flash memory was systematically examined. Monte Carlo simulations were used to reveal how the key secondary particles characteristics of including particle type, linear energy transfer value, and range generated from neutron interactions with the sensitive volume (SV) under varying incident angles influence the SEU mechanisms. the spatial The results indicate that distribution particles produced by neutron irradiation within the three-dimensional memory array is a critical factor in determining both the shapes of MCUs and the physical number of across different incident directions. single-bit upsets secondary

2.1 Device under Test

This study used commercial CT 3D NAND flash memory chips (X2-9060) from Yangtze Memory Technologies (YMTC) as test samples. Atmospheric neutron beams were directed onto the device under test (DUT) from different incident angles. As shown in Fig.1: (a) Schematic neutron beams irradiating the DUT at various angles; (b) The device under test; (c) atmospheric Cross-sectional SEM image showing the chip' s typical three-layer structure, which consists from top to bottom of a passivation layer, a 128-layer stacked memory array (dual-deck structure, total thickness 8.7 μm), and a CMOS circuit layer; (d) The memory cell features a Macaroni structure design. angle incident (a) The Fig.1 atmospheric neutrons on DUT (b) Device under test (c) SEM view of the 128-layer 3D NAND flash memory (d) 3D CT architecture All tested chips were configured in single-level cell (SLC) mode, providing a total usable capacity of 23 GB. The memory architecture consists of 1980 blocks, each containing 768 pages.

Every 6 pages constitute one physical layer, resulting in a total of 128 layers.

Before irradiation, consecutive read operations were performed to screen and select 10 blocks free of random errors, establishing a baseline for subsequent error statistics. The final test sample size was 1006632906 bits. three study employed sealed-package test scheme to ensure the device operated under realistic working conditions. Prior memory cells in the device under test to irradiation, 25 °C. were programmed with an initial data pattern of "AA" . The experiment was performed under static bias at a constant Neutron temperature irradiation lasted for 30 minutes, during which the device was supplied with its and boron rated operating voltage, carbide shielding was used to suppress thermal neutron interference. As shown the neutron beam spot in Fig. 1 Figure 1: see original paper, measured fully 2.5 cm × 2.5 cm, covering the chip surface.

2.2 Neutron source

neutron Atmospheric using irradiation study were experiments the Atmospheric performed Neutron Irradiation Spectrometer (ANIS) at the China Spallation Neutron Source .

As shown in Fig. 2 [Figure 2: see original paper], ANIS generates a broad-spectrum neutron beam by tungsten target with bombarding a high-energy protons[21–23].

Its neutron energy spectrum, ranging from meV to atmospheric environment neutron defined by the JEDEC standard[24]. With a flux intensity approximately 10^9 times higher than the natural atmospheric flux, ANIS enables accelerated simulation of neutron-induced effects. closely matches Comparison Fig.2 Neutron Differential Energy Spectra between ANIS and JEDEC[24] The neutron fluence rate employed in this experiment was approximately conditions: results indicate 1\$×10^{6}\$ $\mathrm{cm}^{-2} \cdot \mathrm{s}^{-1}$. Test that the single-event upset cross-section of the device remained stable under two 1.09$\times10^{6}$ different $\mathrm{cm}^{-2}\cdot\mathrm{s}^{-1}$ and 1.21$\times10^{6}$ $\mathrm{cm}^{-2}\cdot\mathrm{s}^{-1}$. To ensure

experiment

fundamental principle of maintaining an error statistical preventing effectively deviation caused by error accumulation. reliability, adhered statistical strictly occurrence of <1

3.1 MCU Screening

number After each irradiation, the chip was immediately read back three consecutive upsets times. The occurring in the pre-selected error-free blocks was counted for each read cycle.

The median value from these three measurements was then taken as the effective number of upsets for that test run. Accurate identification of MCUs is especially critical, given the inherent structural characteristics of 3D NAND flash memory.

Identification Methodology:1)The logical addresses of all experimentally obtained soft errors were converted into physical addresses using table, yielding the three-dimensional physical coordinates of each upset.Multiple soft errors occurring in spatially adjacent memory cells were classified as a single MCU .2) For 3D NAND flash memory, an MCU is specifically defined as a fault in which multiple cells located event ion trajectory and along the physically within three-dimensional undergo simultaneous logic state flips. address mapping adjacent array In contrast to the planar MCU distributions typically observed in 2D NAND, MCUs in 3D NAND exhibit pronounced vertical propagation along the stacking direction. Such events are defined by three key criteria: 1) a common underlying bit-flip mechanism; 2) spatial adjacency in physical layout; 3) induction by a single high-energy particle. Notably, 3D NAND architecture, each WL corresponds to an independent page. As a result, bit flips single occurring vertically along a string—though physically adjacent—are mapped to different byte addresses at the logical level, and thus are registered and counted as single-bit upsets (SBUs).

3.2 Experimental Results

logical Through physical address mapping relationship, this study constructed the SEU spatial distribution maps with three dimensional coordinates for different incident direction.

String String Front direction Side direction String Fig.3 Three-dimensional distribution of SEUs under different incident direction[17] Back direction Heavy ion Fig. 3 [Figure 3: see original paper], illustrated characteristic distribution patterns of atmospheric neutron-induced SEU are observed within the three-dimensional memory array: 1) randomly distributed discrete upsets, 2) "string-like" clusters aligned along ion trajectories. Physically, during programming operations, the gate field driven electron injection leads to localized charge trapping within the charge trapping layer. When incident neutrons undergo nuclear reactions in the memory secondary array, particles generated can cause ionization.

The resulting ionization charge may be shared among adjacent sensitive nodes, giving rise to MCU. In contrast to the dense "string-like" clusters produced by irradiation ($\mathrm{LET} = 11.4\,\mathrm{MeV \cdot cm^2 \cdot mg^{-1}}$), as shown in Fig. 3(d)[17], the sparser "string-like" features in Fig. 3(a),(c) suggest that only secondary small atmospheric particles neutrons interacting with the memory layers are high-LET, long range heavy ions. fraction of generated As shown in Fig. 3, atmospheric neutron-induced MCU display diverse three-dimensional distribution patterns[25,26]. Based on the classification spatial and statistical analysis of MCU events of varying sizes, the key qualitative characteristics summarized in Table 1 were derived in this study.

Table 1 Logical sizes and shapes of different MCUs 2-bit MCU 3-bit MCU 4-bit MCU 5-bit MCU 6-bit MCU 7-bit MCU As summarized in Table 1, maximum observed neutron-induced MCU is 7 bits, and the spatial distribution of MCUs shows a pronounced dependence on the incident direction. MCU events predominantly extend along the direction of incoming neutrons. Under both front and back incidence, the MCU shapes are mainly "string-like," with only a few exhibiting "L-type" distributions. This pattern alignment between the neutron beam and the bit-line (BL) direction, which causes most secondary particles to travel along the BLs, with only a minor fraction deviating from this path. contrast, when neutrons are incident from the side (parallel to the word-line, explained direction), proportion "L-type"MCUs increases relative to the front/back cases. Since charge transfer in 3D NAND flash memory occurs primarily along the bit-line direction, "string-like" remain patterns three dominant morphology across all irradiation angles. their proportion MCU events show a distinct range dependence: significantly lower than that of SBUs.

This distribution characteristic correlates strongly with the atmospheric neutron energy spectrum, which is dominated by neutrons with energies below 10 MeV, while those above 10 MeV are relatively particles scarce. Most produced by neutron interactions with the memory cells possess low LET and secondary cannot traverse short ranges. Owing to their low LET and limited penetration depth, these adjacent particles their memory layers. Consequently, energy deposition is effectively confined to individual cells, making them the primary cause of SBUs. Conversely, a small fraction of secondary particles with high LET values and long ranges constitute the main mechanism inducing MCU events. Furthermore, all observed MCUs are randomly distributed within the memory array, confirming their neutron from atmospheric origin interactions.

Calculate the SEU cross-section and MCU cross-section atmosphere using the following formula: upset SEU j the number of In the equations, σSEU represents the SEU cross-section of the device; Nupset denotes single-event upsets; ϕ is the total neutron fluence, the total number of neutrons received by the device during the experiment; Nb is the test sample size; σMCU represents the MCU cross-section of the device; and NMCU is the number of MCU events.

Front Incident direction Fig.4 The number of SEUs and MCUs at different incident direction and the proportion of MCUs in SEUs Front Incident direction Fig.5 The cross sections of SEU and MCU under different incident direction number incidence represents As shown in Fig.4 and Fig.5, the front "worst-case" direction in terms of susceptibility. Under frontal irradiation, atmospheric neutron-induced SEUs is 25% higher than under side or back incidence, the SEU cross-section is 26.9% greater, and the number of MCUs is 50% higher. In contrast, the SEU and MCU counts side and back incidence are under comparable. directional primarily dependence differences in neutron interactions with materials outside the sensitive volume: first side incidence, neutrons under interact with material, whereas under back incidence, they interact mainly with copper (Cu) the metal Because interconnect layers. reactions with probability of nuclear tungsten and copper is higher than with silicon, sensitive volume in the side and back directions. Consequently, both SEU and these MCU counts are lower under tungsten-based neutrons tungsten fewer stems reach orientations incidence. compared frontal Pre-rad E > 1MeV Post-rad E > 1MeV Vth-Vref/mV Fig.6 Vth distribution before and after irradition at atmosphere neutron before circuit, current integrated Figure 6 [Figure 6: see original paper] illustrates the shift threshold voltage (Vth) before and after irradiation. As the tested device is a fully direct packaged voltage measurement characteristics after feasible. From the irradiation is not perspective effect single-event mechanisms, when high energy neutrons strike the memory array, the secondary particles generated along their tracks induce a shift in the Vth of the affected memory cells. A bit flip occurs when this shift exceeds the read reference voltage[24]. In the figure, the horizontal axis represents the voltage offset relative to Vref, and the vertical axis indicates the number of read errors at each voltage level. The experimental results reveal a threshold leftward shift voltage distribution after irradiation, accompanied by an increase in the error energy confirms count. This deposited generated secondary particles within the memory cell region leads to the flipping of cell states. in the overall neutron Fig.7 Schematic diagram of the sources of MCU of different sizes Fig.7 schematically illustrates the origins of MCUs of different sizes, where the red cells represent upset memory cells. Notably, due to the high aspect ratio of the via etching process, each via exhibits a tapered profile. This results in non-uniform charge-trapping characteristics across different memory layers, so that not all cells along the same ion trajectory experience an upset.

As shown in Fig.7, most secondary particles generated under front and back neutron incidence propagate along the BL direction. Spatially, they follow the the vias, creating axial direction of continuous that penetrate multiple memory layers and giving rise ion tracks to large, vertically (Z-axis) aligned MCUs. For side incidence, secondary particles travel mainly along the WL direction. Compared with 2D NAND flash, where transfer occurs charge predominantly along BLs, these particles readily induce upsets in neighboring cells along the

BL direction, forming large MCUs oriented vertically along the Z-axis. A small fraction of secondary particles deviate from the incident characterized by lower LET values, direction; these ranges, and a limited spatial short influence region.

Mechanism analysis reveals that large-size MCUs formation of depends primarily on two key factors: (1) the proximity of the ion track to the center of the sensitive volume,when a secondary particle passes close to the sensitive region center, the induced Vth shift becomes large enough to overcome the critical-charge variation caused by fluctuations; process the secondary particles properties of themselves—only those with sufficiently high LET and long ranges are likely to produce large MCUs. blocking layer. The 10 nm polysilicon channel, an 8 nm SiO_2 tunneling layer, an 8 nm Si_3N_4 charge trapping layer, and an 8 nm device Al_2O_3 back-end includes 17 layers of metal interconnects. In the simulations, 1$×10^{9}$ neutrons were incident from the front, side, and back directions, following the measured atmospheric neutron energy spectrum shown in Fig.2. A single charge-trapping layer was defined as the SV, with geometric dimensions of 92 nm (outer nm (inner diameter) × 34 nm (thickness). diameter) × 76 These experimental observations align well with theoretical expectations. neutron Because spectrum contains a relatively small fraction of neutrons with energies above atmospheric

10 MeV (Fig. 2), the yield of high-LET

secondary ions is low, which directly large explains the low proportion of MCUs observed. Moreover, neutrons undergo nuclear reactions more readily with tungsten (W) and copper (Cu) than incidence, a with silicon. Under front larger number of neutrons interact directly within the sensitive region, generation further secondary particles that can induce upsets. favoring

3.3 Monte Carlo Simulation

Based references[27,28] reverse-engineering data, a simulation model of a 128-layer 3D NAND flash memory cell was constructed in this study. As shown in Fig. 8 [Figure 8: see original paper], the structure Its A-A cylindrical via. features cross-section, from inside to outside, comprises: a 20 nm oxide filling layer, a Fig.8 Model of the NAND Flash device Front α Li B C N O F Na Mg Al Si Er Tm Yb Lu Hf Ta W Secondary ion species in the SV Fig.9 Atmospheric neutrons induced secondary particle distribution in the device SV (E > 1MeV) Fig. 9 [Figure 9: see original paper] presents the distribution of secondary particle species (with E >1 atmospheric generated incidence, neutrons within the SV. For front, side, dominant secondary ions are silicon and nitrogen.

Since the sensitive volume consists of nitride material, the primary interaction mechanism is elastic scattering between neutrons and the sensitive region, which produces particles.

Notably, under side and back incidence, particles secondary secondary generated these include a small fraction of high-Z ions, being higher reactions with both the variety and quantity of incidence. This difference arises from nuclear that occur before neutrons reach the sensitive volume: in side incidence, neutrons interact mainly with tungsten based gate material, whereas in back incidence they traverse multiple metal layers (containing W and Cu). The longer path in the back layers through metal direction leads to a greater diversity and interconnect The simulation results in Fig.10 show that most secondary particles have low LET values (<5 MeV • cm^2 • mg^{-1}) and short ranges (<100 nm), which are the primary cause of SBUs. A small fraction of ions, however, exhibit high characteristics MeV • cm^2 • mg^{-1}). The maximum LET of secondary particles within the sensitive volume reaches 12.11 MeV • cm^2 • mg^{-1}.

In the memory cell studied here (Fig.8), such particles can penetrate up to seven adjacent cells along the via direction, thereby inducing large-size MCU events.

The proportion of secondary particles with LET >5 MeV • cm^2 • mg^{-1} is 13.77% significantly incidence, under higher than under side (4.87%) or back incidence. Although more (9.96%) front high-Z secondary particles generated in side and back incidence, the number of neutrons that actually reach the SV is reduced due to absorption and abundance high-Z secondary scattering in the side-gate structures and particles. back-end metal layers. Furthermore, some high-Z particles produced in these explain why directions cannot reach the SV because limited range. These factors their total collectively front number of SEUs is higher incidence incidence. is worth noting that although secondary particles predominantly strike the active layers vertically, a small fraction near the center produce oblique which trajectories, fundamentally the variety of MCU accounts physical shapes observed in Table1. The agreement between simulation close Fig.10 LET and range of secondary ions in the SV induced by incident neutrons with various energies(E $>$ 1MeV) results and experimental data confirms the validity of the adopted physical model.

Based on Fig.10, the critical charge for SEU generation in the 3D NAND calculated. flash memory secondary

analysis

Statistical particles within the same critical charge interval is equivalent to determining the particles distribution within that interval. Using equation (5) from reference [29], the critical charge is derived. secondary Where QC is the critical charge (fC), LETth is the LET threshold for inducing an SEU (MeV • cm^2 • mg^{-1}), ρSi is the density of silicon material ($\mathrm{mg/cm}^3$), d is the thickness of the sensitive volume (cm). neutron irradiation Due to the significant mismatch between the sensitive volume area and probability charge distribution deposited by secondary particles within the sensitive volume was normalized using Equation (4). area, total Where WLET the distribution probability of the deposited charge from secondary particles, N is the number of incident neutrons within a specific deposited charge range, Ntotal is the total number of incident secondary particles, SSV is the incident area of neutrons on the sensitive volume, and SSi is the incident area of neutrons on silicon.

Front Chare deposited in the SV(fC) Fig.11 Probability of charge deposited in the SV by secondary ions induced by incident various neutrons energies(E > 1MeV) small deposited Fig.11 shows the distribution of charge atmospheric neutron-generated secondary particles within the device' s sensitive volume.

Owing geometric cross-section of the sensitive volume, the effective neutron flux reaching this region is relatively low. Simulations reveal the maximum charge deposited by secondary particles in the 4.26 fC. sensitive Further critical charge associated with secondary particles produced under side incidence is generally lower than that for front and back incidence. This difference explains why the deposited charge proportion of large-size MCUs to the total SEU count for side incidence is only 0.44%, which is markedly lower than the proportions for front incidence (1.18%) and back incidence (0.83%). reaches indicates

analysis

volume

4 Conclusion

Using meV–GeV broad-spectrum neutron beam from the Irradiation Neutron Atmospheric the China Spallation Spectrometer at study Neutron Source, that, contrast different directions systematically investigates the influence incident atmospheric neutron-induced SEUs in 128-layer CT dual-deck stacked 3D NAND flash memory. The

results

indicate that the dominant failure modes neutron broad-spectrum under irradiation are SBUs and MCUs. By reconstructing three-dimensional spatial SEU events, we distributions observed characteristic "string-like" distribution induced by heavy ions, neutron-induced SEUs exhibit a predominantly random spatial distribution, with only a limited number showing of MCU events "string-like" patterns. Both SEU and MCU counts are higher under front incidence than under side or back incidence. The MCU patterns are mainly "string-like", with a fraction appearing as "L" -shaped clusters. The maximum number of upset bits within a single MCU event was found to be 7 bits. small Based on experimental data and reverse-engineering analysis, a device model developed neutron-transport simulations were performed. The simulation results show that under front incidence, the secondary particles generated by neutrons within the sensitive volume are predominantly nitrogen and silicon ions. In contrast, incidence, and backside under high-Z particles such as Er, Yb, Ta, Lu, and W are also produced in addition to nitrogen and silicon ions, with the variety and abundance of these high-Z backside incidence. This outcome is mainly attributed to nuclear reactions that occur between the incident neutrons and the tungsten-based gate material or the copper and tungsten containing layers before the metal neutrons reach the SV. interconnect front under incidence, Further simulation analysis shows proportion of secondary particles with LET greater

$5\,\mathrm{MeV} \cdot \mathrm{cm}^2 \cdot \mathrm{mg}^{-1}$

reaches 13.77%, markedly higher than that under side incidence (4.87%) or back incidence (9.96%). This higher yield of high-LET particles results in a significantly larger SEU cross-section incidence compared to the other two orientations, which explains the experimentally observed directional dependence of SEU sensitivity. front Author contributions:

All authors contributed to the study conception design. Material preparation, data collection, and analysis were performed by Hong-De Li, Hong Zhang, and Yang Jiao. The first draft was written Zhan-Gang Zhang, and was critically reviewed for scientific rigor by Zhi-Feng Lei, Hui Li, and Guo-Guang Lu. All authors commented on previous versions and approved the final manuscript. by Hong-De Li Acknowledgments:

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References

[1] M. J. Marinella., Radiation effects particles being most pronounced for advanced emerging nonvolatile memories. IEEE Trans. (2024).

Nucl. Sci. 68, 546-572 (2021).doi: 10.1109/TNS.2023.3334949. 10.1109/TNS.2021.3074139. [7] E.P. Wilcox, M.J. Campola., A TID [2] A. Goda, 3-D NAND Technology characterization Achievements and Future Scaling multi-Terabit COTS 3D NAND Perspectives. IEEE Transactions on flash. Paper Presented at Electron Devices. 67, 1373-1381 Radiation Effects Data Workshop (2020). (San Antonio, USA 08-12 July 10.1109/TED.2020.2968079. 2019). [3] M. Bagatin, S. Gerardin, A. doi:10.1109/REDW.2019.8906606.

Paccagnella et al., A Heavy-Ion [8] L.Coïc, G. Augustin, L. Serrano et Detector Based on 3-D NAND al., Heavy ion induced SEU and Flash Memories. IEEE Transactions MBU sensitivity of 3D NAND flash on Nuclear Science. 67, 154-160 structures. Paper Presented at 2022 (2020). 22nd European Conference 10.1109/TNS.2019.2955776.

Radiation Its Effects [4] M. Bagatin, S. Gerardin, A.

Components and Systems(Venice, Paccagnellaet Secondary Italy 03-07 October 2022).doi:

Particles Generated by Protons in 10.1109/RADECS55911.2022.1041 3-D nand Flash Memories. IEEE Transactions on Nuclear Science, [9] T.R. Oldham, R.L.

Ladbury, M. (2022).

Friendlich et al., SEE and TID 10.1109/TNS.2022.3171521. characterization of an advanced [5] M. Bagatin, S. Gerardin, A. commercial 2Gbit NAND flash Paccagnella et al., Effects of heavy nonvolatile memory.

IEEE Trans. irradiation vertical Nucl. Sci. 53, 3217-3222 (2006).

NAND flash memories. IEEE Trans. doi:10.1109/TNS.2006.885843.

Nucl. Sci. 65, 318-325 (2018). doi: [10]H.Schmidt, D. Walter, F. Gliem et 10.1109/TNS.2017.2777887. al., TID and SEE tests of an [6] M. Bagatin, S. Gerardin, A. advanced 8 gbit NAND flash Paccagnella et al., Total ionizing memory. Paper Presented at 2008 effects 3-D NAND Radiation Effects Data replacement gate flash memory Workshop (Tucson, USA 14-18 July cells. IEEE Trans. Nucl. Sci. 74, 2008).doi: 10.1109/REDW.2008.13. [11] F. Irom, D.N. Nguyen, M. Bagatin [16] D. Chen, E. Wilcox, R.L. Ladbury et al., Catastrophic failure in highly et al., Heavy ion and proton-induced scaled commercial NAND flash single event upset characteristics of memories. IEEE Trans. Nucl. Sci. a 3D NAND flash memory. IEEE (2010).doi:

Trans. Nucl. Sci. 65, 19-26 (2018). 10.1109/TNS.2009.2035315. doi: 10.1109/TNS.2017.2764852. [12] M. Bagatin, S. Gerardin, A. [17] Y. Jiao, J.H. Yang,Q. Wang et al., Paccagnella al., Single Heavy ion induced SEUs and layer multiple cell upsets in 25nm NAND dependence in Dual-Deck flash memories. IEEE Trans. Nucl.

NAND flash memories. IEEE Trans. Sci. 60, 2675-2681 (2013). doi:

Nucl. Sci. 72, 2689-2696 (2025). 10.1109/TNS.2013.2273436. doi: 10.1109/TNS.2025.3541272. [13] E.P. Wilcox, M.L. Breeding, M.C. [18] M. Bagatin, S. Gerardin, A.

Casey al., Observation Paccagnella al., Atmospheric low-energy proton direct ionization neutron soft errors in 3D NAND in a 72-layer 3D NAND flash flash memories. IEEE Trans. Nucl. memory. IEEE Trans. Nucl. Sci. 68, Sci. 66, 1361-1367 (2019). doi: (2021). 10.1109/TNS.2018.2886401. 10.1109/TNS.2021.3063156. [19] X.S. Zheng, Y.H. Wang, R.G. Mo [14] P.M. Conway, M.J. Gadlage, J.D. et al., Experimental Study on SEL Ingalls Impact a COTS 3D NAND Flash elemental makeup of an IC in Memory and SEL Protection. Paper generating single-event upsets from Presented at 2025 6th International low-energy (<10 MeV) neutrons: A Conference on Radiation Effects of 3-D NAND flash case study. IEEE Electronic Devices (Yangzhou, Trans. Nucl. Sci. 66, 466-473 China 16-18 April 2025).doi: (2019). 10.1109/ICREED65908.2025.11036 10.1109/TNS.2018.2885847. [15] D. Chen, E. Wilcox, R.L. Ladbury [20] D. Peyronel,G. Lama,M. Valla et et al., Heavy ion irradiation fluence al., Neutron-induced Single Event dependence for single-event upsets Effects in 3D Managed NAND in a NAND flash memory. IEEE Memories, IEEE Transactions on Trans. Nucl. Sci. 64, 332-337 Nuclear

Science, (2017). 10.1109/TNS.2026.3650913. 10.1109/TNS.2016.2615719. [21] C. Cazzaniga, N. Bhuiyan, M.

Kastriotou, et al., Fast Neutron https://doi.org/10.1109/tns.2019.291 Measurements Characterization the ChipIr [26] S. Gao, X.Y. Li, S.W Zhao et al., Beamline.

IEEE Transactions on Heavy ion-induced MCUs in 28 nm Nuclear Science, 71, 1520-1526 SRAM-based FPGAs: upset (2024). proportions, classifications, 10.1109/TNS.2024.3416540. pattern shapes. NUCL SCI TECH. [22] T. Long, S. Ahmed, C.Y. Huang et Developing time-of-flight (2022).https://doi.org/10.1007/s413 polarized neutron capability at the China Spallation Neutron Source. [27] J. Park, J.W. Han, G. Yoon et al., NUCL SCI TECH. 34, 146 (2023).

Single-Event Upset https://doi.org/10.1007/s41365-023- Charge-Trap NAND flash memories.

IEEE Transactions on Electron [23] J.Y. Tang, Q. An, J.B. Bai et al.

Devices. 69, 6089-6094 (2020). doi: Back-n white neutron source at 10.1109/TED.2022.3207113.

CSNS and its applications. NUCL [28] YMTC's Xtacking 3.0 - Not what TECH. (2021).

TechInsights was expecting to see, https://doi.org/10.1007/s41365-021- https://www.techinsights.com/blog/ ymtcs-xtacking-30-not-what-techins [24] Q.Z Y., Evaluating the broad ights-was-expecting-see; neutron spectrum of ANIS. Applied [accessed 27 January 2026].

Radiation and Isotopes. 203,111075 [29] Z.G. Zhang, J. Liu, Y. M. Sun et al. (2023).

Supply voltage dependence https://doi.org/10.1016/j.apradiso.20 single event upset sensitivity in diverse SRAM devices.Paper [25] Z.G. Zhang, Z.F. Lei, T. Tong et al.

Presented Tibetan-Plateau-Based Real-Time International Conference Testing Simulations Reliability, Maintainability Single-Bit and Multiple-Cell Upsets Safety (Guangzhou, China 06-08 in QDRII+ SRAM Devices. IEEE August 2014).

Transactions on Nuclear Science. 66, 10.1109/ICRMS.2014.7107149. (2019).

Note: Figure translations are in progress. See original paper for figures.