A High-Precision Time-to-Digital Converter for TOF-PET Applications with MCP-PMTs

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Abstract

This paper presents the design and measurement results of a time-to-digital converter (TDC). This TDC is a part of an Application-Specific Integrated Circuit (ASIC) named FPMT Readout Chip (FPMROC), which is designed to read out signals from a Microchannel Plate Photomultiplier Tube (MCP-PMT, also called FastPMT/F-PMT). One of the applications is the detector for time-of-flight positron emission tomography (TOF-PET). FPMT is capable of detecting single photoelectrons with a rise time of less than 100 ps. It features an extremely low transit time spread (TTS), around 10 ps for multi-photoelectrons and under 50 ps for single photoelectrons. To achieve the required timing resolution, the TDC design employs 11 voltage-controlled differential delay cells combined with an interpolator for the measurement of the time-of-arrival (TOA) and time-over-threshold (TOT). A self-calibration scheme based on the system clock (CLK40M) is implemented to compensate for process, voltage, and temperature (PVT) variations. The TDC is fabricated using a commercial 55 nm CMOS technology. The overall performance of the TDC has been characterized. The TOA achieves a timing resolution of 13.5 ps across an effective range of 23.7 ns. The TOT bin size is measured to be 14.1 ps with a dynamic range of approximately 3.3 ns. The effective measurement precision reaches 42.4 ps for all TOA codes and 33.0 ps for all TOT codes. The TDC' s power consumption is about 20.01 mW at a hit rate of 40 MHz.

Full Text

A High-Precision Time-to-Digital Converter for TOF-PET Applications with MCP-PMTs*

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This paper presents the design and measurement results of a time-to-digital converter (TDC) developed as part of an Application-Specific Integrated Circuit (ASIC) named FPMT Readout Chip (FPMROC), designed to read out signals from a Microchannel Plate Photomultiplier Tube (MCP-PMT, also called FastPMT/F-PMT). One primary application is the detector for time-of-flight positron emission tomography (TOF-PET).

The FPMT is capable of detecting single photoelectrons with a rise time of less than 100 ps and features an extremely low transit time spread (TTS), measuring around 10 ps for multi-photoelectrons and under 50 ps for single photoelectrons. To achieve the required timing resolution, the TDC design employs 11 voltage-controlled differential delay cells combined with an interpolator for measuring both time-of-arrival (TOA) and time-over-threshold (TOT). A self-calibration scheme based on the system clock (CLK40M) compensates for process, voltage, and temperature (PVT) variations. Fabricated using commercial 55 nm CMOS technology, the TDC achieves a timing resolution of 13.5 ps across an effective range of 23.7 ns for TOA measurements. The TOT bin size is measured at 14.1 ps with a dynamic range of approximately 3.3 ns. The effective measurement precision reaches 42.4 ps for all TOA codes and 33.0 ps for all TOT codes, while consuming about 20.01 mW at a hit rate of 40 MHz.

Keywords: Time-to-Digital Converter, FPMT, TOF-PET, Integrated Circuit

INTRODUCTION

The Microchannel Plate Photomultiplier Tube (MCP-PMT, also called FastPMT/FPMT) is capable of detecting single photoelectrons with excellent time resolution [1, 2], enabling its use in various fields including high-energy physics, high-precision medical imaging devices, biofluorescence detection, and nucleic acid detection devices. The FPMT exhibits an extremely low transit

time spread (TTS), measuring around 10 ps for multi-photoelectrons and less than 50 ps for single photoelectrons [3]. To meet picosecond-level time resolution requirements, we have developed a TDC prototype called FPMROC to measure the time-of-arrival (TOA) against a specific clock and record the time-over-threshold (TOT) to correct the time-walk effect [4].

Time-of-flight positron emission tomography (TOF-PET) represents one of the state-of-the-art advances in PET imaging, significantly improving both spatial resolution and image quality compared to conventional PET systems. The TOF detector—especially those based on MCP-PMTs—is a critical component enabling TOF-PET functionality, placing stringent demands on readout electronics that require a time resolution of approximately 15 ps. Such high temporal resolution necessitates a high-precision time-to-digital converter (TDC), typically realized via analog signal quantization and time-to-digital conversion techniques. Application-specific integrated circuits (ASICs) emerge as a key solution to meet these rigorous requirements.

Broadly speaking, ASIC-based TDCs fall into two categories: analog TDCs and digital TDCs. Traditional analog TDCs leverage time amplifiers [5] or time-to-amplitude converters (TACs) [6] to attain high timing precision. While this approach offers superior resolution and ideal linearity, it is highly sensitive to process, voltage, and temperature (PVT) variations, posing challenges for calibration and rendering it vulnerable to noise. Digital TDCs, by contrast, convert time intervals directly into digital codes, thereby reducing PVT sensitivity and enabling seamless multichannel integration.

The most basic digital TDC architecture employs a high-frequency counter for time-interval measurement, where the time resolution is dictated by the clock frequency. To achieve higher precision, ring-oscillator TDCs have gained widespread adoption. A ring-oscillator (RO) TDC comprises multiple delay cells configured into a ring oscillator, with its time resolution defined by the intrinsic propagation delay of these cells. To push resolution even further, passive interpolation techniques have been developed, which utilize passive resistive interpolators to subdivide the propagation delay of individual delay cells. To extend the conversion range of passive-interpolator-based RO-TDCs, a coarse counter is incorporated to count the ring oscillator' s oscillation cycles without incurring significant increases in die area or power consumption.

The TDC in FPMROC performs precision time measurements of hit arrival times relative to the 40 MHz system clock. It comprises 11 voltage-controlled differential delay cells with a passive interpolator. According to TOF-PET application requirements, this TDC should measure the TOA with a bin size of less than 15 ps over a 23.5 ns dynamic range. It also measures the TOT of the input signal for time-walk correction with an identical bin size over a 2 ns dynamic range [7]. In this work, we present the TDC fabricated in 55 nm CMOS technology. This design achieves a TOA bin size of 13.5 ps across a 23.7 ns dynamic range and a TOT bin size of 13.9 ps across a 3.3 ns dynamic range. The TDC consumes approximately 20.01 mW from a 1.2 V power supply.

The remainder of this paper is organized as follows. Section II elaborates on the TDC design. Section III presents the test results. Finally, Section IV concludes the work.

II. DESIGN OF THE TDC

A. Design Approach

Common architectures for TDC implementation include delay-line-based TDCs [8, 9], vernier TDCs [10, 11], delay-locked-loop (DLL)-based TDCs [12, 13], pulse-shrinking TDCs [14, 15], and RO-based TDCs [16, 17]. Among these, RO-based TDCs stand out for their structural simplicity: by employing a delay loop rather than a delay line, they achieve significant chip area reduction. Moreover, they offer high linearity and fine resolution, benefiting from their inherent noise-shaping capability. To overcome the intrinsic resolution limit imposed by the delay cells, a prominent architectural solution has emerged: the passive interpolator method. Building on this approach, we propose an enhanced interpolation structure to further boost the time resolution of RO-based TDCs [18].

Our TDC design adopts a differential adjustable ring-oscillator delay line with an interpolation scheme. Specifically, a corresponding register array captures dual-edge timestamps—for both the leading and falling edges of the input pulse —from the RO delay line, with these timestamps sampled at the leading edge of the system clock. The position of the pulse signal transition within the RO delay line is encoded to represent the arrival time relative to the system clock.

The propagation delay of the differential delay cell is susceptible to PVT variations. To compensate for such variations, a self-calibration scheme is employed, which captures two successive timestamps using two consecutive leading edges of the system clock. For each input pulse, this dual-timestamp measurement calibrates the cell' s propagation delay and enhances the overall measurement precision.

B. TDC Structure

Fig. 1 presents the block diagram of the FPMROC TDC, which comprises a Controller, a Delay Line, a Ripple Counter, and an Encoder. The TDC' s input hit signal (Pulse) is derived from the discriminator output after pre-amplification. This TDC measures both the TOA and TOT of the input pulse; additionally, it captures two consecutive rising edges of the system clock to calibrate for process, voltage, and temperature (PVT) variations.

Based on the 40 MHz system clock (CLK40M) and the input pulse signal, the Controller generates three sets of dedicated clocks: the TOA clock (toa_{clk} and toa_{writeclk}), the TOT clock (tot_{clk} and tot_{writeclk}), and the calibration (CAL) clock (cal_{clk} and cal_{writeclk}). Time measurement is implemented using a delay line with an interpolator for fine time quantization and two groups of ripple counters for coarse time measurement. Three

recorders—each implemented in a D-flip-flop (DFF) chain—capture the fine and coarse time information for the TOA, TOT, and CAL at the falling edges of toa_{clk}, tot_{clk}, and cal_{clk}, respectively. At the falling edges of the toa_{writeclk}, tot_{writeclk}, and cal_{writeclk}, the TOA, TOT, and fine and coarse measurement of the CAL are written into the Encoder. Within the Encoder, the TOA, TOT, and CAL time information (both fine and coarse) are encoded into their corresponding digital codes: TOA_{Code}[11:0], TOT_{Code}[7:0], and CAL_{Code}[11:0]. The hit-flag signal indicates the presence of valid data within each 40 MHz clock (CLK40M_{Out}) cycle.

Fig. 2 illustrates the timing diagram of the key signals in the TDC. Clk40M is the 40 MHz system clock, with a period of 25 ns (from one rising edge to the next). The rising edge of toa_{clk} is aligned with that of the input pulse signal. To minimize the duration that DFFs remain in transparent mode and reduce power consumption, the toa_{clk}, tot_{clk}, and cal_{clk} signals are active-low for approximately 300 ps. At the rising edge of toa_{clk}, the DFFs capture the TOA fine time (toa_{finedata}[65:0]) and coarse time (toa_{ca}/cb[4:0]). The falling edge of the toa_{writeclk}, which latches the TOA fine and coarse time information into the Encoder, is aligned with the rising edge of the toa_{clk}. The timing relationships for tot_{clk}/tot_{writeclk} and cal_{clk}/cal_{writeclk} mirror those of toa_{clk}/toa_{writeclk}. At the rising edge of tot_{writeclk}, the DFF-captured fine time (toa/tot/cal_{finedata}[65:0]) and coarse time (toa/tot/cal_{ca}/cb[4:0]) values for TOA, TOT, and CAL are pushed into the asynchronous FIFO within the Encoder. To ensure compliance with timing requirements during data writing to the FIFO, the low-level duration of tot_{writeclk} is set to 1.45 ns.

Within each 25 ns period of the system clock (CLK40M), the TDC is configured to process only the first incoming pulse; any subsequent pulses in the same period are ignored, and the TDC is then ready to handle the first pulse of the next clock period. The pulse generated by the preamplifier and discriminator in the FPMROC typically has a width of 1 ns, with a maximum of 2 ns.

C. Fine Time Measurement

Fig. 3 shows the schematic of the TDC fine time measurement circuit. The delay line incorporates 11 differential amplifiers and forms a ring oscillator based on an interpolator scheme. Each delay cell is designed with interpolated differential delay stages to enable high-precision time measurement and achieve fine time resolution. At each rising edge of the toa_{clk}, tot_{clk}, and cal_{clk} signals, a DFF chain captures a snapshot of the interpolator outputs, yielding the TOA/TOT/CAL fine time information (A[65:0], T[65:0], and C[65:0]) for each delay cell.

The delay cell is a voltage-controlled differential amplifier (VCDA), as depicted by the blue dashed block in Fig. 3. Its propagation delay is approximately 78

ps. To achieve a bin size of 13 ps, a 6-stage passive interpolator is implemented to subdivide this propagation delay as illustrated in the red dashed box in Fig. 3.

D. Coarse Time Measurement

To extend the measurement range, the coarse time is generated by two groups of 5-bit ripple counters that count the number of oscillation cycles. The clock signal for this ripple counter (clk_{cnt}) is derived from the 65th tap of the delay line, as shown in Fig. 3. The clk_{cnt} is then buffered by a CLKBUFX2 to boost its driving strength. The coarse time measurement module comprises the 5-bit ripple counter and three groups of DFFs, with the latter capturing the coarse timestamps for the TOA, TOT, and CAL operations, respectively.

The TOA/TOT/CAL DFF chains may violate the setup and hold time constraints of the DFFs sampling the ripple counter outputs, potentially leading to metastability and unstable outputs from the DFF chains. To mitigate this metastability issue, the ripple counter and associated DFF chains are duplicated, with the clock signal for the duplicated counter inverted. If metastability arises in one set of DFF chains, the more stable output is selected via the corresponding fine time information.

E. Calibration Circuit

To compensate for propagation delay variations induced by PVT variations, a self-calibration mechanism is implemented, which records the cal_{clk} signal twice, as shown in Fig. 2. The cal_{clk} signal has two consecutive pulses with a known phase interval (25 ns), and this interval carries the calibration information. The CAL fine and coarse time measurements are captured by DFF chains, and the two consecutive sets of CAL fine and coarse time data are then written into the Encoder at the falling edge of the cal_{writeclk} signal. These two consecutive CAL fine and coarse timestamps are subsequently encoded into the CAL_{Code}[11:0] output.

F. Prototype Chip

The TDC was fabricated in a commercial 55 nm CMOS process. Fig. 5(a) shows the layout of the FPMROC single-channel chip, which occupies an area of approximately 3 mm × 1 mm. The FPMROC single-channel chip comprises two main parts: a single channel readout circuit integrating front-end electronics (FEE), TDC, scrambler (SCR), serializer (SER), and phase-locked loop (PLL); and a standalone TDC module including an LVDS receiver (RX), TDC, scrambler (SCR), and serializer (SER). Fig. 5(b) presents a photograph of the FPMROC single-channel chip wire-bonded on the test board, enabling direct access to the TDC signals for measurement.

This article presents the test results of the standalone TDC. The design and test results of the single-channel readout circuit will be reported in future work.

III. TEST RESULTS OF THE TDC

A. Test Setup

Fig. 6 presents the block diagram of the TDC test setup. A Clock Builder (Si5338 EVB) supplies a 25 MHz synchronous clock to the ROPLL board, which generates a 1.6 GHz clock for the TDC. Concurrently, the Clock Builder provides a 20 MHz or 5 MHz synchronous clock to drive two separate signal generators: the Keysight 8195A, which outputs a 40.001 MHz clock for TOA scanning, and the Agilent 81130A, which generates a 20 MHz clock with adjustable pulse width for TOT scanning. The Clock Builder also provides a 1.6 GHz clock, synchronous with both the 40.001 MHz and 20 MHz clocks, acting as the reference clock for the FPGA' s GTX transceivers. The 1.6 Gbps output data from the standalone TDC is buffered in an FPGA (AMD KC705 Development Kit) and transferred to a personal computer (PC) via an Ethernet cable for subsequent performance analysis. An FMC (FPGA Mezzanine Card) Fanout Board is employed to expand the FPGA' s general-purpose input/output (GPIO), enabling TDC configuration through the chip' s SPI interface. Finally, Fig. 7 displays a photograph of the fully assembled TDC test setup.

For dedicated TOA measurements, the pulse frequency is set to emulate the hit occupancy of the TDC. Specifically, in the actual test, a clock frequency of 40.001 MHz is used to generate pulses, emulating 100% hit occupancy. Owing to the small frequency offset (from 40 MHz to 40.001 MHz), the pulses continuously track the 40 MHz system clock in 0.625 ps steps [19], thereby covering the full measurement range. The pulse width, determined by the pulse generator, emulates the TOT and is set to a typical value of 1 ns for the dedicated TOA study.

For detailed TOT characterization, the pulse frequency is set to 20 MHz with a fixed TOA of 1 ns, which corresponds to a 50% hit occupancy of the TDC. The pulse width is varied using a dedicated pulse generator in 2 ps steps over the nominal TOT dynamic range from 0.1 to 3.4 ns.

B. Resolution

In TOA measurements, the TOA of the input pulse increments by a fixed step after each system clock cycle. Similarly, in TOT measurement, the input pulse width increases by a constant step after data acquisition. The TOA and TOT times are calculated based on the indices of the acquired data. Plotting the measured TOA/TOT codes against the corresponding TOA/TOT times yields a stair-shaped curve, which represents the transfer function.

Least-squares linear fits to the measured data are also plotted in Fig. 8(a) and (b). The reciprocal of the linear fit slope gives the quantization resolution (i.e., the average bin size) of the measurement. The bin size corresponds to the propagation delay of each tap in the interpolator. The time resolution for the TOA is estimated to be 13.5 ps, while the TOT bin size is approximately 13.9 ps. A

0.4 ps discrepancy in time resolution between TOA and TOT results from two factors: the different measurement approaches for the TOA and TOT transfer curves, as well as the varying performance characteristics of the employed instruments (Keysight 8195 and Agilent 81130A).

C. TDC Nonlinearity

The nonlinearity performance of the TDC is characterized using the code-density method. Differential nonlinearity (DNL) is defined as the deviation of each bin size from the ideal 1-LSB step width, while integral nonlinearity (INL) represents the cumulative sum of DNL values. As shown in Fig. 9(a) and (b), the INL and DNL of the TOA over its full dynamic range are within $±$1.9 LSB and $±$1.0 LSB, respectively. Elevated DNL values are observed at TOA code addresses corresponding to integer multiples of 132. This behavior stems from the delay chain architecture: the D65 output drives the clock signal of the coarse counter, which increases the bin size corresponding to the D65 tap.

The transfer functions for TOA and TOT are shown in Fig. 8(a) and (b), respectively. A magnified view of each transfer function at a typical TOA/TOT code is displayed in the lower-left corner. The effective dynamic range of the TOA is about 23.7 ns, which exceeds the required dynamic range of 23.5 ns.

The same approach is employed to analyze the nonlinearity of the TOT. The TOT exhibits an INL of $±$1.5 LSB and a DNL of $±$1.2 LSB across its full dynamic range, as depicted in Fig. 10(a) and (b), respectively.

D. Self-Calibration

The delay cells in the TDC block are differential amplifiers, whose propagation delays are sensitive to PVT variations. By using two strobes with a known 25 ns time interval, the system constantly measures propagation delay for each hit. Consequently, variations in the propagation delay of these delay cells can be self-calibrated during the offline analysis phase.

Fig. 13 shows the histogram of the measured calibration codes from the TOA scan test, which reflects the calibration results of the delay cells. The measured mean value (μcal_{code}) of all CAL codes is about 1844.94, with a standard deviation (σ) of 1.379 LSB. Using equation 2, the average bin size (bin_{{{size}}_{{average}}}) of the delay cell is calculated to be approximately 13.551 ps. This measured mean aligns with the theoretical average propagation delay within 0.1%.

The calibration verifies the proposed model and demonstrates effective compensation for PVT variations.

IV. CONCLUSIONS

A differential ring-oscillator TDC with a passive interpolator has been successfully designed, fabricated, and tested in a commercial 55 nm CMOS process, and its performance has been thoroughly characterized. The TDC achieves a resolution of approximately 13.5 ps with a dynamic range of 23.7 ns. For TOA operation, the INL and DNL are within $±$1.9 LSB and $±$1.0 LSB, respectively, and the effective measurement precision across all TOA codes is approximately 42.4 ps. For TOT operation, the TDC exhibits a bin size of 13.9 ps and a dynamic range of 3.3 ns. The corresponding INL and DNL are within $±$1.5 LSB and $±$1.2 LSB, respectively, with an effective measurement precision of approximately 33.0 ps across all TOT codes. The TDC core consumes 20.01 mW at a hit rate of 40 MHz. The measured performance of the proposed TDC fully satisfies the requirements of MCP-PMTs for TOF-PET applications.

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Table 1: Comparison with Previous Works

Reference	Process (nm)	Resolution (ps)	INL (LSB)	DNL (LSB)	Precision (ps)	Power consumption (mW/ch)
[20] (2025)			$±$0.64	$±$0.26		
[21] (2024)			$±$2.08	$±$0.46		
[22] (2023)			$±$1.07	$±$0.92		
[23] (2019)			$±$3.0	$±$0.77		
[24] (2021)			$±$0.5	$±$0.4		
[25] (2025)			$±$1.9	$±$1.0		
This work	55	13.5	$±$1.9	$±$1.0	42.4 (TOA), 33.0 (TOT)	20.01

Note: Figure translations are in progress. See original paper for figures.