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Abstract

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Full Text

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Abstract

Digital backends are critical for modern radio interferometers, enabling wideband signal acquisition and flexible data processing. We present the design of a new RFSoC-based backend developed for the Central China Array (CARRY), currently under construction in Hubei, China. The system, built on the RFSoC-xczu47DR platform, supports wideband sampling of eight inputs at 1 GSPS with polyphase filter bank processing, channel equalization, and high-speed 100 GbE data transmission. Experimental results confirm reliable synchronization, high linearity, and stable spectral processing. This design provides CARRY with a high-performance, scalable, and cost-efficient reference architecture that can be extended to other radio interferometer arrays.

Key words: Astronomical Instrumentation, Methods and Techniques –instrumentation: interferometers –techniques: interferometric

1. Introduction

To achieve higher spatial resolution beyond the diffraction limit of a single dish, radio telescope arrays are employed to perform interferometry [**?**, **?**, **?**]. The performance of an interferometer depends not only on site conditions and individual antenna sensitivity, but also critically on its digital backends [**?**, **?**]. Modern digital backends typically incorporate real-time channelization, correlation, and beamforming, thereby supporting high angular resolution and wide fields of view [**?**, **?**, **?**, **?**].

Fast Radio Bursts (FRBs) are millisecond-duration, highly energetic astrophysical transients whose origins remain one of the most compelling open questions in astrophysics [**?**]. Thousands of FRBs have been detected to date, yet only one Galactic event (FRB 20200428) has been confirmed [**?**]. To capture additional Galactic FRBs and probe their emission physics, our group is constructing the Central China Array (CARRY) in Hefeng County, Enshi City, Hubei Province. The CARRY pathfinder will consist of four 6 m dishes operating in the 1–1.5 GHz L-band, with the primary goal of monitoring magnetars in the Milky Way.

The digital backend for CARRY is developed on the RFSoC-xczu47DR platform. RFSoC devices have been widely adopted in radio astronomy backends. For example, ARGOS F-engine employs an RFSoC-based design with four Analog

Figure 1

Figure 1: Figure 1

to Digital Converter (ADC) channels, each supporting 1 GHz bandwidth, 2048 frequency channels, and 100 GbE data transmission [**?**]. The Qitai 110 m radio telescope (QTT) utilizes an RFSoC ZCU111 to implement eight ADC channels sampled at 4.096 GSPS, providing 512 frequency channels and 10 GbE outputs [**?**]. The APSERa experiment employs an RFSoC ZCU111 to implement a two-channel spectrometer with 2 GHz bandwidth and 16,384 frequency channels [**?**].

Building on this foundation, we have designed and implemented a new RFSoC-based digital backend board tailored for CARRY, as shown in Figure 1

. The system supports simultaneous sampling of eight ADC channels at 1 GSPS per channel, providing 512 MHz instantaneous bandwidth. Two operational modes are implemented: (1) raw baseband data and (2) real-time frequency channelization with 1024 frequency channels (reconfigurable to 2048 or 4096). The system also supports packetized high-speed data transmission via dual 100 GbE interfaces. While developed for CARRY, the design is scalable and readily extensible to other interferometer arrays, such as DSA-2000 [**?**].

An additional advantage of the system is its cost-effectiveness. A single RFSoC-xczu47DR board, priced at approximately USD 9800, can simultaneously acquire data from up to four dual-polarization antennas (eight ADC channels), making it well-suited for multi-element expansion. The main hardware specifications of the RFSoC xczu47DR board are summarized in Table 1 . Taken together, these attributes make the design a practical and versatile backend for next-generation radio-astronomy arrays.

2. System Design

Collaboration for Astronomy Signal Processing and Electronics Research (CASPER[1]) is the open-source toolflow for radio astronomy [**?**]. The CASPER toolflow[2] has become a widely recognized standard for digital backend prototyping in radio astronomy. Its hardware-software ecosystem has been deployed in a variety of telescope backends worldwide, ranging from large single-dish facilities such as the Five-hundred-meter Aperture Spherical radio Telescope (FAST) in China [**?**] and the QTT [**?**], to array projects such as the Tianlai pathfinder [**?**, **?**] and the Square Kilometre Array pathfinder [**?**]. By providing modular, reusable hardware platforms together with a flexible FPGA-based signal-processing toolchain, CASPER enables rapid prototyping and facilitates the development of scalable and efficient digital backends for diverse scientific applications [**?**, **?**].

[1] https://casper.astro.berkeley.edu/wiki/Main_Page
[2] https://casper-toolflow.readthedocs.io

A key feature of the digital backend is its support for two operational modes: frequency domain and time domain, which can be selected at initialization via Python scripts. The overall system architecture is shown in Figure 2 [FIGURE:2]. The architecture supports fast Fourier transform (FFT) channels of 1024, 2048, and 4096 via minor configuration changes. In this work, we adopt a 1024-channel configuration. Having outlined the overall system architecture and dataflow, we now describe the design and implementation of each functional module in detail, including the ADC, polyphase filter bank (PFB), FFT, equalizer (EQ), and RAM_{IO} components, as well as the 100 GbE transmission interface.

2.1. ADC Module

The first stage is the ADC, which digitizes the incoming antenna signals and produces baseband sample streams for subsequent channelization and spectral processing [**?**, **?**]. The ADC is implemented with the AMD/Xilinx RF Data Converter (RFDC) IP core, wrapped by a CASPER toolflow block [**?**, **?**]. The RFDC block automatically detects the target RFSoC device and infers the tile architecture, generating an appropriate configuration interface. This board uses a four-tile architecture, and its configuration interface includes options for tile enable selection, sampling rate configuration, internal phase-locked loop usage, multi-tile synchronization, and clock information display [**?**].

In this design, the sampling rate is set to 1024 MSPS. The RFDC presents four samples per clock cycle, each as a signed 16-bit word; the most-significant 14 bits carry valid data, and the two least-significant bits are zero-padded, per PG269 [**?**]. At run time, a mode flag set by the Python control scripts routes the digitized samples to different paths: Mode 1 (frequency-domain) feeds the ADC output to the PFB for channelization and then to FFT→EQ→RAM_{IO}; Mode 2 (time-domain) bypasses the channelizer and writes samples directly to RAM_{IO} for packetization and streaming of raw baseband data. In both modes, data are transmitted via the dual 100 GbE interfaces.

2.2. PFB and FFT Modules

In astronomical observations, minimizing spectral leakage is critical, as it can degrade calibration accuracy, introduce contamination from narrowband interference, reduce beamforming coherence, distort frequency-dependent delay corrections, and broaden dispersed time-domain signals—ultimately impacting the detection of pulsed and transient events [**?**]. To suppress spectral leakage and improve channel isolation, PFBs are widely adopted in radio astronomy backends [**?**, **?**].

In this design, we implement these two stages using the `pfb_{{{fir}}_{{real}}}` and `fft_{{{wideband}}_{{real}}}` modules from the CASPER `mlib_{devel}` library. The `pfb_{{{fir}}_{{real}}}` block partitions the input data into multiple parallel taps and applies FIR filtering. In our RFSoC terminal,

the ADC produces four parallel samples per clock cycle, which are fed into the four input ports of this block; each stream is convolved with the filter coefficients to produce filtered outputs. These outputs are then passed to the `fft_{{{wideband}}_{{real}}}` block, which applies a wideband FFT to channelize the signal. The module exploits the Hermitian symmetry of real-valued inputs by using a complex core, thereby reducing computational resource usage by half compared to a conventional implementation.

For this work, the FFT size is configured to 2048, and only the positive-frequency components are retained, resulting in 1024 frequency channels. Consequently, the number of FFT output ports is half the number of input ports—two ports in this design—with the 1024 channel values output sequentially across them. The input-output structure of the PFB and FFT stage is illustrated in Figure 3 [FIGURE:3].

2.3. Equalizer Module

Following channelization, the EQ operates on the complex FFT outputs prior to per-component (real and imaginary parts) 16-bit quantization. Each frequency bin is represented as a complex value with real and imaginary components. During quantization, the real and imaginary parts are each quantized to 16 bits and then combined into a 32-bit complex output. This procedure compensates for variations in the frequency response of the analog front end or signal chain, ensuring that quantization is performed within an appropriate dynamic range.[3]

In our design, each FFT output stream is associated with one BRAM for coefficient storage. With eight ADC channels and two positive-frequency output streams per channel, the system yields 16 FFT output streams in total; hence, 16 BRAMs are provisioned—one per stream. The EQ coefficients are stored in these BRAMs using the `UFix_{18}7` fixed-point format, with each BRAM containing 512 coefficients. The EQ module slices the FFT outputs into real and imaginary parts, multiplies each with the corresponding coefficient. In this step, the product of the input data and its associated coefficient is computed, and the most significant 16 bits of the result are obtained. This design enables independent equalization for every frequency channel, thereby flattening the passband response prior to quantization.

Although the architecture supports per-channel calibration, in practice, we adopt a simplified configuration by applying the same EQ coefficient uniformly across all inputs and channels. This reduces calibration complexity while still meeting the performance requirements.

2.4. RAM_{IO} Module

Following the EQ stage, the output consists of 16 parallel data streams, each containing 512 frequency channels. Pairs of streams are logically merged to

[3]https://casper.astro.berkeley.edu/wiki/PAPER_Correlator_EQ

reconstruct one 1024-frequency-channel spectrum per ADC, yielding eight post-merge data streams. These quantized frequency domain data are then transferred to the RAM_{IO} module for buffering and width adaptation before packetization. As shown in Figure 4 [FIGURE:4], the RAM_{IO} module is constructed from eight dual-port RAM blocks, each assigned to one of the eight data streams. Each RAM buffers data with a 64-bit write port and presents a 512-bit read port, i.e., it aggregates consecutive 64-bit writes into wide 512-bit read words. This word-width adaptation reduces downstream read beats and framing overhead, improving the efficiency of the packetizer.

A selector then sequentially reads out the data from the RAM blocks and forwards them to the subsequent packaging and distribution module. The addressing scheme of the RAM inputs and outputs, together with the selector control logic, is illustrated in Figure 5 [FIGURE:5]. In this scheme, the `sel` signal toggles every 256 clock cycles, implementing a round-robin mechanism that ensures the four ADC data streams are sequentially packaged and transmitted.

2.5. VDIF Module

After buffering and serialization in the RAM_{IO} module, the formatted data are prepared for network transmission. Since very long baseline interferometry (VLBI) is identified as one of the key scientific objectives of the CARRY, a standardized packet header must be adopted to ensure compatibility with global VLBI networks. To this end, the design employs the VLBI Data Interchange Format (VDIF) header, augmented with a counter, to form a 64-byte packet header. The VDIF portion itself occupies 32 bytes, with all fields defined according to international standards for VLBI data exchange. The 32-byte VDIF header is logically divided into eight consecutive 4-byte words, each storing a distinct set of information. Among these, the first two words form the core of the header, providing absolute time and frame identification.

In the first word, bits [29:0] record the system' s absolute time, defined as the number of elapsed seconds since 2000 January 1, as shown in Figure 6 [FIGURE:6]. During system initialization, the absolute second count at the start time is written into a register. A 1 pps signal then enables the counter once per second, incrementing it synchronously with real time. The resulting values are combined through an adder and stored in the appropriate header fields.

The second 4-byte word is reserved for the data frame number, as illustrated in Figure 7 [FIGURE:7]. This value is generated by the `data_{{{frame}}_{{ctr}}}` register. A 1 pps signal resets the frame counter once per second, while the `start_{{{of}}_{{frame}}}` signal asserts high once every 1024 clock cycles. Together, these mechanisms ensure that the counter resets at each new second and records up to 250,000 frames per second.

The packet header and payload are transmitted sequentially to the 100 GbE module for final packetization. As shown in Figure 8 [FIGURE:8], two packet

Figure 9

Figure 2: Figure 9

formats are supported, corresponding to the two operational modes of the system. The first module is assigned to transmit the packet streams from ADC0-3, while the second module handles ADC4-7. On the transmission side, the data streams are directed to two independent 100 GbE ports on the server. Each 100 GbE interface sustains an aggregate transmission rate of 66 Gbps. On the receiving side, the traffic arriving at one 100 GbE port is distributed across four sub-ports, with each sub-port handling approximately 16.4 Gbps.

3. Experimental Validation

To validate the performance and reliability of the digital backend, a series of experiments was conducted with emphasis on the behavior of key functional modules.

3.1. ADC Synchronization and Linearity Testing

To support real-time transport of high-throughput data, the RFSoC-xczu47DR device integrates two 100 GbE interfaces. In this design, two 100 GbE modules are instantiated, each corresponding to one of the physical network interfaces. Because the ADCs directly determine the sampling precision and timing reference of analog radio signals, their synchronization and accuracy are fundamental prerequisites for downstream signal processing. Therefore, the first stage of testing focused on evaluating the synchronization and accuracy of the eight ADC channels, specifically their alignment in sampling clocks and consistency in sampled data. This assessment is essential not only for ensuring correct multi-channel parallel processing but also for the proper operation of subsequent modules such as FFT, equalization, and packetization.

Three complementary test methods were designed to evaluate multi-channel sampling consistency from both the time and frequency domains.

Method 1: A 32 MHz single-tone signal was generated and split into eight paths using a power divider, feeding all eight ADCs simultaneously. The sampled waveforms were captured via the SNAP module and plotted to visually inspect time-domain alignment across channels, as shown in Figure 9

.

Method 2: Cross-correlations were computed between ADC channel 0 and each of the other seven ADC channels in order to estimate inter-channel time delays. This provides a quantitative measure of synchronization error relative to a common reference channel, as illustrated in Figure 10 [FIGURE:10].

Method 3: The sampled values from all eight ADCs were transformed into the

frequency domain via FFT, as shown in Figure 11 [FIGURE:11]. At the target frequency bin ν_0 (corresponding to the injected 32 MHz signal), the complex FFT output of channel m can be written as

$$S_m[\nu_0] = R\{S_m[\nu_0]\} + j \cdot I\{S_m[\nu_0]\},$$

where $R\{S_m[\nu_0]\}$ and $I\{S_m[\nu_0]\}$ denote the real and imaginary parts of the complex spectrum, respectively. The phase of channel m at this frequency bin is then obtained as

$$\phi_{m0} = \arg\{S_m[\nu_0]\} = \arctan \frac{I\{S_m[\nu_0]\}}{R\{S_m[\nu_0]\}},$$

where ϕ_{m0} is the phase angle in radians. The relative phase difference between channel m and the reference channel ADC0 is calculated by

$$\Delta\phi_{m0} = \phi_{m0} - \phi_{00}.$$

Finally, the corresponding time delay is obtained by

$$\Delta\tau_{m0} = \frac{\Delta\phi_{m0}}{2\pi f_0},$$

where f_0 is the known input tone frequency, and $\Delta\tau_{m0}$ gives the sampling time offset between ADC channel m and ADC channel 0.

The results from these three tests consistently indicate that the ADCs exhibit excellent synchronization performance. The measured clock offsets were on the order of 0.1 ns—well below a single sampling interval—demonstrating both high sampling accuracy and strong inter-channel coherence.

In addition, the linearity of the eight ADC channels was evaluated. Sampling data were acquired under varying input power levels, and the rms values were computed to characterize the relationship between input power and output amplitude. These rms values were logarithmically scaled and plotted to obtain input-output transfer curves for each ADC, as shown in Figure 12 [FIGURE:12]. All eight channels maintained good linearity across the tested input power range from -20 to +13 dBm.

3.5. Advantages and Comparison with Existing Radio Telescope Backends

CASPER' s FPGA boards are widely deployed at major radio facilities (e.g., FAST, QTT, TMRT [**?**], Tianlai, MeerKAT [**?**] and so on) and therefore serve as representative reference boards. The main hardware specifications of our RFSoC xczu47DR board are summarized in Table 1 . Because such boards can be paired

with different ADC mezzanines and firmware options, we adopt bandwidth-normalized cost metrics that are agnostic to specific firmware features. For readability, numerical units are reported once in Table 2 and omitted in the text; price entries are indicative (see table note).

We define the board-level cost per unit bandwidth as

$$C_{\mathrm{MHz}} = \frac{\mathrm{Price}}{\mathrm{Bandwidth\ (MHz)}},$$

and evaluate this metric for representative configurations (Table 2). Using Equation (5), we obtain $C_{\mathrm{MHz}} = 19.60$ (RFSoC), 168.00 (CASPER board A), and 112.00 (CASPER board B). Relative to RFSoC, the corresponding cost ratios are 8.5 (A/RFSoC) and 5.7 (B/RFSoC).

To account for the number of independent analog inputs, we further define

$$C_{\mathrm{MHz\cdot ch}} = \frac{\mathrm{Price}}{\mathrm{Bandwidth\ (MHz)} \times \mathrm{Channels}},$$

and obtain $C_{\mathrm{MHz\cdot ch}} = 2.45$ (RFSoC), 5.25 (CASPER board A), and 9.33 (CASPER board B), i.e., ratios of 2.1 and 3.8 relative to RFSoC. These results indicate a substantially lower capital cost per unit input bandwidth for the RFSoC backend compared with representative CASPER-class FPGA boards.

3.6. Observation: Galactic H I 21 cm Line Experiment

To provide an end-to-end validation under on-sky conditions, we carried out an astronomical test aimed at detecting the Galactic neutral hydrogen (H I) 21 cm line [**?**, **?**]. A 1.5 m radio telescope was used to observe toward the Galactic center—a sightline known to exhibit strong H I emission near the rest frequency of 1420.40575 MHz. The received signal was conveyed through the analog-digital chain to the RFSoC-based digitizer, where baseband time streams were recorded. The data were then processed offline by channelizing and averaging the time-domain records to form a power spectrum. As shown in Figure 16 [FIGURE:16], the H I spectral feature is clearly detected in the 1420.45–1420.70 MHz range, confirming the correct operation of the acquisition, transport, and spectral analysis pipeline.

3.7. Conclusion

We have developed a digital backend tailored for large-scale radio interferometers. The system integrates eight 1 GSPS ADCs, providing 512 MHz instantaneous bandwidth per input. It supports dual operating modes: direct baseband acquisition and polyphase filterbank channelization, with validated configurations of 1024, 2048, and 4096 frequency channels (1024 channels demonstrated in this work). Channel equalization and data quantization are implemented in

real time, and output is delivered via dual 100 GbE interfaces. This backend meets the requirements of high performance, scalability, and cost efficiency. It can serve the CARRY, and we also consider it a strong candidate for digital backends in other small- to medium-scale radio interferometers. Currently, we are in the prototype stage, with initial work completed in a laboratory environment. However, electromagnetic compatibility (EMC) considerations have not yet been addressed. We plan to thoroughly address this aspect during the actual deployment phase, ensuring that the equipment meets the necessary EMC requirements.

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