Research and Implementation of Wideband Radio Signal Channelization Based on RFSoC (Postprint)

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Abstract

This study addresses the requirement for real-time sampling and transmission of wideband signals in radio astronomy and develops a complete technical workflow spanning hardware implementation to firmware compilation. The system is built on the Xilinx ZCU111 Radio Frequency System-on-Chip (RFSoC) development board, incorporating both hardware modifications and customized development using the CASPER open-source toolflow. A channelization approach based on the Polyphase Filter Bank algorithm is adopted, for which the corresponding theoretical derivations are provided, and the scheme is implemented within the CASPER toolflow. The resulting firmware enables channelization (16 channels over a 128 MHz bandwidth) of ultra-wideband signals sampled at 4096 MHz on the RFSoC platform. Deployed on the Nanshan 26 m radio telescope for L-band (964–1732 MHz) observations, the system successfully produced high signal-to-noise ratio pulsar profiles after subsequent processing with the DSPSR software, thereby validating the reliability of the channelization algorithm. These results demonstrate the feasibility of RFSoC-based architectures for wideband signal channelization and provide a practical development pathway for future astronomical backend systems.

Full Text

Preamble

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Abstract

This study addresses the need for real-time sampling and transmission of wideband signals in radio astronomy by developing a comprehensive technical workflow from hardware implementation to firmware compilation. The system, based on the Xilinx ZCU111 Radio Frequency System on Chip (RFSoC) development board, incorporates hardware modifications and custom development using the CASPER open-source toolflow. We adopt a channelization method based on the Polyphase Filter Bank algorithm, provide the corresponding theoretical derivations, and implement the scheme on the CASPER open-source toolflow. The developed firmware enables channelization (16 channels, 128 MHz bandwidth) of ultra-wideband signals at a 4096 MHz sampling rate on RFSoC hardware. Deployed at the Nanshan 26 m radio telescope for L-band (964–1732 MHz) observations, the system successfully produced high signal-to-noise ratio pulsar profiles after processing with DSPSR software, validating the reliability of the channelization algorithm. These results confirm the feasibility of RFSoC-based architectures for wideband signal channelization, offering a practical pathway for future astronomical backends.

Key words: instrumentation: detectors –instrumentation: miscellaneous – methods: observational

1. Introduction

The advancement of radio astronomy and receiver technology has made signal processing demands increasingly stringent. Radio astronomy signal processing must achieve wider observation bandwidths, higher sampling frequencies, and faster data transmission rates to meet the growing requirements for high-precision astronomical data acquisition and analysis.

In early 2018, Xilinx introduced its Radio Frequency System on Chip (RFSoC), the industry' s only adaptive Radio Frequency (RF) platform. This device integrates FPGA logic, ARM processors, high-speed ADCs/DACs, and 10/40/100 GbE interfaces, enabling up to 16 channels at 2.5 GSPS or eight channels at 5

GSPS with 14-bit resolution, all while maintaining low power consumption and cost efficiency. This breakthrough technology has garnered significant attention in radio astronomy. Internationally, RFSoC-based systems have been applied in key astronomical projects, including the cryogenic ALPACA phased array feed [**?**], the CCAT-prime MKID readout [**?**], and the ultra-wideband receiver at Parkes [**?**]. The Australian ASKAP team has also developed the JIMBLE RFSoC board, which upgrades the cryoPAF and BIGCAT systems. In addition, RFSoC technology has been benchmarked for converter performance in astronomical applications [**?**], and acquisition systems have been successfully demonstrated [**?**]. In China, RFSoC is being adopted in digital backend development [**?**], phased array feed beamforming systems [**?**], and the planned ultra-wideband, multi-beam system for the QiTai Radio Telescope (QTT) [**?**, **?**], underscoring its rapidly expanding role in next-generation astronomical instrumentation. Additionally, RFSoC+GPU backends have been proposed for the QTT backend [**?**, **?**].

The Collaboration for Astronomy Signal Processing and Electronics Research (CASPER), developed at the University of California, Berkeley, is a versatile and reconfigurable platform for radio astronomy backend development. With high flexibility, broad compatibility, and support for rapid deployment, it has been widely adopted in large-scale radio telescope instrumentation worldwide [**?**, **?**]. CASPER continuously follows advancements in radio technology, adopts new technologies to develop radio signal processing platforms, and drives the upgrade of radio astronomy backends. Its hardware platforms have evolved from early series such as IBOB, BEE2, ROACH1/2, and SNAP to the current RFSoC series. Among them, ZCU111 is a prominent platform within the RFSoC series. CASPER is also continually improving the RFSoC development library by adding new digital platforms and designing hardware and digital signal processing modules based on the latest RFSoC architecture.

Channelization is a fundamental technique in radio astronomy, enabling wideband or ultra-wideband signals to be decomposed into multiple narrowband sub-channels for flexible and efficient processing. In this study, we developed a wideband channelization firmware based on the Polyphase Filter Bank (PFB) algorithm. The mathematical foundations of PFB implementations tailored to radio astronomy have been established [**?**]. Building on this basis, recent studies have demonstrated its effectiveness in practice: critically sampled PFBs have been simulated with Parkes telescope data [**?**], and oversampled designs have been shown to improve spectral isolation and suppress inter-channel leakage [**?**]. An oversampled PFB has also been implemented on a Xilinx RFSoC using Vivado HLS and PYNQ, achieving real-time performance suitable for ultra-wideband applications and highlighting the advantages of high-level synthesis for scalable, high-throughput backends [**?**]. Furthermore, oversampled PFBs have been shown to allow accurate inversion via Fourier transforms, enabling near-perfect reconstruction with minimal spectral leakage when designed properly [**?**].

In this study, we upgraded and optimized the ZCU111 RFSoC development board and customized the system using the CASPER toolflow, successfully building an efficient digital sampling platform for radio astronomy. The platform meets real-time broadband signal sampling and transmission requirements in radio astronomy and implements stable and reliable broadband signal channelization using the PFB algorithm. Field tests conducted with the L-band receiver system (964–1732 MHz) of the Nanshan 26m radio telescope (NSRT) yielded high signal-to-noise ratio observational data, validating the system' s performance and feasibility. This work not only offers a novel technical approach for real-time sampling and processing of radio astronomy signals but also lays a solid foundation for future, more complex radio astronomy experiments. Furthermore, the system' s scalability highlights its broad potential and applicability in other fields.

2. Hardware Architecture and Modifications

The AMD Zynq UltraScale+ RFSoC ZCU111 development board enables designers to rapidly initiate RF-class analog designs for wireless, wired access, electronic warfare (EW)/radar, and other high-performance RF applications. The kit supports eight 12-bit 4.096 GSPS ADCs, eight 14-bit 6.554 GSPS DACs, and eight soft-decision forward error correction (SD-FEC) units. It is equipped with Arm Cortex-A53 and Cortex-R5 subsystems, UltraScale+ programmable logic (PL), and ultra-high signal processing bandwidth from the Zynq UltraScale+ device, providing a fast, comprehensive RF analog-to-digital signal chain prototyping platform.

At the hardware level, the ZCU111 RFSoC development board was customized to better support the demands of radio astronomy signal acquisition. To improve clock stability and frequency precision, the onboard 122.88 MHz voltage-controlled crystal oscillator (VCXO) was replaced with a 100 MHz VCXO, ensuring compliance with the stringent timing requirements of astronomical observations. High-speed data transmission was enhanced by extending a 100 GbE Ethernet interface via the VITA57.4 connector, significantly boosting data throughput. Furthermore, a one-pulse-per-second (1 PPS) timing signal was integrated through the peripheral module interface (PMOD) interface, with added protection circuitry to safeguard against voltage variations. These enhancements collectively improved system synchronization, timing accuracy, and data handling performance.

2.1. Clock Optimization

Precise clocking sets the noise and spur floor of RF data converters. On ZCU111, all converters and PL references are synthesized by an LMK04208 driving an LMX2594, as shown in Figure 1 [Figure 1: see original paper]; the LMX2594 can feed the RFDC directly or serve as the RFDC PLL reference.

For radio-astronomy backends, convenient plans often use powers of two or

multiples of ten (e.g., 128, 256, 512, 1024 MHz; 500, 1000 MHz). The original 122.88 MHz VCXO complicates such integer-N plans in TICSPRO. We therefore replaced it with a 100 MHz VCXO to simplify divider planning for both PL and RFDC clocks.

We compared the phase noise of the original 122.88 MHz VCXO with that of the newly installed 100 MHz VCXO. Both options share the same cascaded chain: VCXO (100 or 122.88 MHz) driving the LMK04208 and LMX2594 to generate the final 4.096 GHz sampling clock. Using TI PLLatinumSim with an identical LMX2594 output plan, we evaluated the final 4.096 GHz phase-noise spectrum for the two references. As summarized in Table 1 , the spectra are broadly comparable: the 100 MHz case is equal or lower from 0.1 to 100 kHz offsets, while the 122.88 MHz case is marginally lower beyond 1 MHz (3 dB). At 10 MHz offset the levels are −149.0 and −150.0 dBc/Hz for the 100 MHz and 122.88 MHz chains, indicating near-identical performance. Thus, adopting a 100 MHz reference does not degrade the final clock and also simplifies integer-N/power-of-two divider planning.

Finally, we operate the LMK04208 in dual-loop mode, disciplining the on-board 100 MHz VCXO to the external 10 MHz reference (SMA Port J8). This arrangement combines the long-term frequency accuracy of the external reference with the VCXO' s ultra-low phase noise, yielding a sampling clock with high time-frequency stability suitable for wideband acquisition and processing.

2.2. IO Expansion

The ZCU111 provides four 25 GbE SFP28 interfaces, which can be configured as a single 100 GbE QSFP28 link. However, this bandwidth may be insufficient for high-speed data output in radio astronomy backends. To address this, two 100 GbE interfaces can be expanded via adapter cards connected to the VITA57.4 interface, as shown in Figure 2 [Figure 2: see original paper]. To validate the reliability of the expanded 100 GbE links, we conducted a continuous 24 hr IBERT test using Xilinx' s built-in transceiver diagnostic tools. The results demonstrated stable high-speed transmission with no data loss, and an eye diagram showing an open UI percentage of 88%, indicating excellent signal integrity. These outcomes confirm the robustness and suitability of the adapter cards for sustained astronomical data streaming.

As a general-purpose development board, the ZCU111 does not natively support a 1 PPS input, so we repurpose a PMOD header to receive the 1 PPS signal. Because 1 PPS levels vary across timing sources, the PMOD pin is protected with a 51–100 Ω series resistor and a low-capacitance Schottky clamp (e.g., BAT54SWT1), which provides over-voltage protection while preserving the fast edge. The same PMOD header can also be used to output auxiliary control signals, such as noise-source control.

3. CASPER-Based Firmware and Toolchain Workflow

To meet the specific requirements of this study, the software development tools were optimized, with customized modifications such as pin constraints tailored to the hardware extensions, ensuring proper operation of the newly integrated components. Additionally, the full development workflow—from front-end design through compilation and simulation to the generation of deployable configuration files—was systematically refined, ensuring tight integration between hardware and software and enabling efficient system performance.

3.1. Introduction to the CASPER Development Toolflow

The development toolflow provided by CASPER is built on Simulink in combination with Vivado System Generator, enabling a graphical design approach for FPGA development. Core components are drawn from two Simulink libraries: one for DSP modules and the other for hardware interface modules. By configuring module parameters and connecting graphical blocks, users can develop complete FPGA designs. The environment includes a wide range of radio astronomy-specific processing modules—such as PFB and FFT—as well as standard System Generator components. Upon invoking the CASPER toolflow, a Vivado project is generated, complete with the necessary infrastructure and constraints to support the user' s I/O requirements. Vivado then compiles this into a bitstream. The toolflow appends register mappings to the bitstream, enabling runtime software access to components in the firmware design. The resulting .fpg file, along with a .dtbo file for dynamic device tree loading, is programmed onto a compatible board using the casperfpga Python library. This interaction library also provides methods for register-level communication with the FPGA, facilitating firmware and device tree deployment.

The blocks of the DSP library are built entirely from low-level System Generator primitives and shown as green or brown blocks. Internal architectures are dynamically reconfigured via scripts based on user-defined parameters. Hardware platform modules—colored yellow—include ADCs, FPGA platforms, high-speed 10/100 GbE interfaces, BRAMs, and I/Os. These are tightly coupled with the underlying hardware and include HDL drivers, chip selection logic, clock configuration primitives, IP cores, and FPGA constraint files.

3.2. Constraint Modifications for IO Expansion

To enable 100 GbE Ethernet card expansion, we need to modify the ZCU111' s YAML file (zcu111.yaml). This file contains all the physical attributes of the hardware platform, such as pins, chip manufacturers, and clocks. It is the key for the CASPER toolflow to identify the hardware platform and perform compilation for the corresponding hardware platform. Based on the schematics of the ZCU111 board and the 100 GbE expansion module, appropriate pin and clock constraints must be defined. Figure 3 [Figure 3: see original paper] illustrates the QSFP28 Interface Definition.

Similarly, for the newly added 1 PPS and GPS 1 PPS input ports, corresponding GPIO constraints must also be added in the same file. In addition, the Python scripts within the jasper_{library}/yellow_{block} directory govern the Vivado project generation for each hardware block. These scripts serve as glue logic, combining IP cores and HDL modules into structured TCL scripts for project creation and compilation. Users with knowledge of Vivado can further adapt these files to accommodate specific hardware configurations and design requirements.

4. Algorithm Design and Implementation

To meet the real-time sampling and transmission demands of wideband radio astronomy signals, we developed a firmware architecture for coarse channelization based on a PFB. The design implements a 4096 MHz sampling rate with 16 channels, each with a 128 MHz bandwidth. Channelized baseband data are reordered and buffered via RAM, encapsulated with Very Long Baseline Interferometry (VLBI) Data Interchange Format (VDIF) headers, and transmitted through two 100 GbE QSFP interfaces to a switch or server for further processing.

4.1. Polyphase Filter Bank

A PFB enables the decomposition of a wideband signal into multiple parallel narrowband channels, thereby reducing sampling and processing rates [**?**, **?**, **?**]. In this subsection, we adopt the standard polyphase analysis filter-bank formulation and derive the equations used in our implementation.

Conventional channelization is based on digital down-conversion and low-pass filter banks, as shown in Figure 4 [Figure 4: see original paper]. Given a discrete-time input signal $x[n]$, the output of the kth channel in a uniform critically sampled filter bank can be written as:

$$y_k[m] = \sum_{n=-\infty}^{\infty} x[n]h[mD - n]e^{j2\pi kn/K}$$

where $h[n]$ is the prototype low-pass filter impulse response, D is the decimation factor, K is the total number of frequency channels (FFT size), $k = 0, 1, \ldots, K-1$ is the sub-channel index, and m is the time index after decimation.

The prototype filter $h[n]$ can be decomposed into K polyphase components as:

$$h[n] = \sum_{p=0}^{K-1} g_p[mK + p]$$

where $g_p[m]$ denotes the pth polyphase branch.

Substituting this into the convolution expression yields:

$$y_k[m] = \sum_{p=0}^{K-1} \sum_{l=-\infty}^{\infty} x[mD - lK - p] g_p[l] e^{j2\pi k(lK+p)/K}$$

To simplify implementation, the filtered outputs can be grouped and processed with a K-point inverse discrete Fourier transform (IDFT):

$$y_k[m] = \sum_{p=0}^{K-1} \left(\sum_{l=-\infty}^{\infty} x[mD - lK - p] g_p[l] \right) e^{j2\pi kp/K}$$

Defining the decimated input sequence assigned to the pth polyphase branch as $x_p[m] = x[mD - p]$ and letting $\omega_k = 2\pi k/K$, we obtain:

$$y_k[m] = \sum_{p=0}^{K-1} x_p[m] g_p[m] e^{j\omega_k p}$$

This results in a K-point IDFT over the filtered outputs. Finally, the channelized output of the kth channel can be expressed compactly as:

$$Y_k[m] = \mathrm{IDFT}\{x_p[m] \cdot g_p[m]\}$$

This result provides a stable, computationally efficient solution for wideband radio signal channelization. Equation (6) represents the channelized output of a critically sampled PFB with even sub-band partitioning. Figure 5 [Figure 5: see original paper] illustrates the computational structure of the PFB. The computation of the PFB is performed using the IFFT operation, which is actually implemented via an FFT conversion in the design. The IFFT is computed using the following formula: take the conjugate of $X(k)$, perform an FFT operation, then take the conjugate of the result and divide by N:

$$\mathrm{IFFT}\{X(k)\} = \frac{1}{N} \left(\mathrm{FFT}\{X^*(k)\}\right)^*$$

4.2. PFB Construction Based on CASPER

The high-speed processing capability of PFB technology allows the decimator to be moved ahead of the data processing, significantly reducing pressure on device speed while also decreasing resource demands compared to traditional data processing methods. Using polyphase filtering, large volumes of data are converted into multiple low-speed processes, alleviating the strain on device speed. The channelization in this system is implemented using the PFB algorithm. As shown in the derivation above, the PFB algorithm can be decomposed

into multi-stage filtering and Inverse Fast Fourier Transform (IFFT) operations. The input data stream is split, filtered by polyphase branches, and recombined via IDFT. Under the critical sampling condition, the decimation rate D and the number of channels K are equal, allowing for direct multiplication and accumulation for each decimated channel. We use an example where the decimation rate $D = 32$, the number of channels $K = 32$. For simplicity, the filter order is 128. The polyphase filter implementation is shown in Figure 6 [Figure 6: see original paper], where $H(*)$ represents the filter coefficients, $m = n/D$, and Z^{-1} is the clock delay under the current processing rate conditions.

The radix-2 FFT uses the Cooley-Tukey FFT algorithm [**?**], where an N-point DFT transformation can be expressed as two $N/2$-point DFT transformations. By recursively splitting the DFT into multiple stages, any radix-2 DFT can be implemented. The radix-2 algorithm is widely used, and an example of a 32-point FFT is shown in Figure 7 [Figure 7: see original paper].

4.3. Firmware Design Based on CASPER Toolflow

The signal acquisition and preprocessing data flow is shown in Figure 8 [Figure 8: see original paper]. Based on the theoretical framework outlined above, PFB and FFT modules were constructed. Simulation analysis confirmed that each module performs as required, with adjustable functionality and parameters. The data flow is then linked through wiring. After ADC acquisition, the signal is first cached in a first-in, first-out (FIFO) buffer, followed by channelization via the PFB. Next, FFT is applied to extract the signal' s spectral information. Finally, the signal undergoes gain adjustment and VDIF packaging before being transmitted to external devices. This entire process ensures signal quality and accuracy through efficient hardware design and clock synchronization.

The signal processing modules were constructed in Simulink based on the CASPER development environment, as shown in Figure 9 [Figure 9: see original paper]. The design was analyzed using Simulink' s simulation capabilities, and relevant module designs were adjusted iteratively based on the simulation results. Upon completion of the simulation, the FPGA firmware was compiled using CASPER-specific commands. An evaluation of FPGA resource utilization was also carried out on the ZCU111. The design occupied 22.3% of LUTs, 35.3% of flip-flops, and 30.2% of DSP slices, with BRAM usage reaching 85.5%. The relatively low LUT utilization highlights the efficiency of the PFB-based channelization algorithm, while the higher BRAM demand reflects the buffering and reordering requirements of sub-band data. High-speed transceivers (GTs) were fully employed to support 100 GbE links, whereas clocking resources such as BUFG and MMCM were only marginally used. As summarized in Table 2 , these results demonstrate efficient resource allocation with ample headroom for scalability and further system extension.

5. On-site Verification: NSRT Deployment

The RFSoC-based system developed in this study was tested with the L-band receiver (900–1732 MHz) of NSRT. The receiver operates with a 900 MHz local oscillator, but strong radio-frequency interference (RFI) restricts the usable RF range to 964–1732 MHz, corresponding to an Intermediate Frequency (IF) span of 64–832 MHz (768 MHz). This effective bandwidth maps onto six contiguous 128 MHz sub-bands. A single ZCU111 development board running custom firmware was used to acquire and transmit the L-band signals. The system delivered six dual-polarization sub-bands, each with 128 MHz bandwidth, spanning 964–1732 MHz, as illustrated in Figure 10 [Figure 10: see original paper].

Baseband data were recorded in PSRDADA format by a dedicated server. A five-minute observation of PSR J0332+5434 was conducted. Six sub-bands were recorded as separate PSRDADA baseband files, and each sub-band was processed independently with DSPSR. Manual RFI excision using PAZI significantly improved data quality, yielding clear pulse profiles across all sub-bands, as shown in Figure 11 [Figure 11: see original paper]. The sub-bands were then aligned and combined in frequency with PSRADD, producing an integrated profile spanning 768 MHz (964–1732 MHz), as shown in Figure 12 [Figure 12: see original paper].

Similarly, a 11,900 s observation of PSR J0534+2200 (Crab), covering an effective bandwidth of 768 MHz, yielded a clear folded pulsar profile, as shown in Figure 13 [Figure 13: see original paper]. The main pulse and a weaker interpulse are clearly visible.

6. Conclusion

We have developed and validated a wideband digital backend for radio astronomy using the Xilinx ZCU111 RFSoC platform. The system incorporates hardware enhancements, including a high-stability VCXO, 100 GbE connectivity, and 1 PPS synchronization, together with reconfiguration of the CASPER toolflow for firmware implementation. A PFB-based channelization scheme was theoretically derived and realized in firmware, enabling real-time decomposition of ultra-wideband signals into 16 sub-channels at a 4096 MHz sampling rate.

On-telescope tests at NSRT demonstrated stable operation. Pulsar observations of J0332+5434 yielded clear folded profiles after processing; observations of PSR J0534+2200 (Crab) likewise produced clean profiles. Going forward, we plan longer duration telescope observations, particularly of millisecond pulsars, to further assess the system' s long-term stability.

This study establishes a scalable, low-power, and rapidly deployable framework for next-generation ultra-wideband astronomical backends, with potential applications in pulsar timing, spectral-line studies, and VLBI.

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Note: Figure translations are in progress. See original paper for figures.