Timing Performance Comparison of Two FPGA-based Charge Readout Electronics for TOF PET applications

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Abstract

Timing performance plays a vital role in radiation detector applications. Recently, two types of FPGA-based charge readout methods, namely an FPGA-based charge-to-digital converter (FPGA-QDC) and an FPGA-based charge-to-time converter (FPGA-QTC), have been proposed. Compared with the traditional time-over-threshold (ToT) technique, these methods can not only achieve high-precision timing pickoff but also accurately measure the charge from radiation detectors. Both approaches employ mixed-signal circuitry. In each circuit, the analog section consists of an operational amplifier and a small number of resistors and capacitors, while in the digital section all functional modules are implemented in the FPGA. In particular, an FPGA LVDS receiver is used as a general-purpose voltage comparator, and a time-to-digital converter (TDC) is developed to measure the pulse width of the digital signal.

To compare the timing performance of the two circuits, a coincidence timing resolution (CTR) evaluation setup comprising two TOF-PET detectors was constructed. Each PET detector consisted of a 3\$$\times 3\times 10mm$^{3}\$ LYSO crystal bar coupled to a SiPM at one end. The results show that the best CTR values between the two PET detectors were 335.03 ± 2.00 ps and 357.86 ± 3.31 ps full width at half maximum (FWHM) for the FPGA-QDC and FPGA-QTC, respectively. Both circuits are promising candidates for power-efficient, multichannel, and low-cost front-end readout electronics for nuclear radiation detectors.

Full Text

Preamble

Timing Performance Comparison of Two FPGA-based Charge Readout Electronics for TOF PET Applications

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Timing performance plays a vital role in radiation detector applications. Recently, two kinds of charge readout methods based on field programmable gate array (FPGA), namely FPGA-based charge-to-digital converter (FPGA-QDC) and FPGA-based charge-to-time converter (FPGA-QTC), were proposed. In comparison with traditional time over threshold (ToT), they can not only achieve high-precision timing pickoff but also accurately measure charge from radiation detectors. Both of them are mixed-signal circuits. In both circuits, the analog part consists of an operational amplifier, few resistors and capacitors. In the digital part, all function modules are implemented in the FPGA. Specifically, an FPGA LVDS receiver works as a general voltage comparator. A time-to-digital converter (TDC) was developed to calculate the pulse width of the digital signal. To compare the timing performance of both circuits, a coincidence timing resolution (CTR) evaluation setup comprising two TOF PET detectors was constructed. Each PET detector was made up of one 3$×3×10$mm^{3} LYSO crystal bar coupled with a SiPM detector at one end. Results show the best CTR values between the two PET detectors were 335.03 ± 2.00 ps and 357.86 ± 3.31 ps full width at half maximum (FWHM) for the FPGA-QDC and FPGA-QTC respectively. Both are promising circuits for power-efficient, multi-channel and low-cost front end readout electronics for nuclear radiation detectors.

Keywords: TOF PET, timing performance, FPGA, charge measurement.

Introduction

Timing performance plays a significant role in high-quality image reconstruction for positron emission tomography (PET) scanners [1–3]. In time-of-flight positron emission tomography (TOF-PET), timing information is picked off at a lower discrimination threshold so that the fastest emitted photons including prompt Cherenkov lights can be detected. To achieve the best coincidence timing resolution (CTR) in TOF-PET, many readout schemes have been designed.

Considering power consumption, compactness and cost, the most commonly used front-end readout electronics for TOF-PET is the time-over-threshold (ToT) scheme [4] instead of full waveform digitization. In the ToT method, the input signal is compared to a preset lower threshold, and the leading-edge discrimination timing and the pulse width can be uniquely determined. Based on the ToT scheme, many application-specific integrated circuits (ASIC) have been developed, such as NINO [5], TOFPET2 [6] and HRFlexToT [7]. Although the best timing performance can be obtained using the lowest possible threshold, the pulse width of the digital signal after the discriminator is not proportional to the input charge to be measured. This strong nonlinearity can be improved with

Figure 1

Figure 1: Figure 1

the dynamic ToT method (dToT) [8], which generates a dynamic threshold to match the characteristics of the falling edge of signals. The dynamic threshold generators are different for different front-end electronics, such as preamplifiers and shaping amplifiers.

High-frequency readout electronics [9-11] for TOF PET opens a way to conduct high-precision CTR and energy measurements. In this scheme, the timing signal is amplified by radio frequency (RF) amplifiers, which helps extract the high-frequency components of the SiPM signals. The energy signal is picked up with a voltage amplifier (VA) or transimpedance amplifier (TIA). With this readout electronics, a 100 ps CTR can be achieved for single-pixel TOF PET applications [11]. In multi-channel design, however, it will consume more power than the ToT circuit. A tradeoff is made by use of timing multiplexed readout method [12].

Recently, FPGA-based charge-to-digital converter (FPGA-QDC) methods [13-15] have been investigated, which enable simultaneous timing and energy measurement with only one amplifier. Different from ToT, the energy is measured with good linearity without calibration and correction. In this scheme, it includes an analog circuit and a digital circuit. One channel of the analog circuit is made up of an operational amplifier (op amp for short), an integration capacitor C_f and several resistors. In the digital circuit, the FPGA can process signals from hundreds of analog circuits. In the FPGA, the SSTL or LVDS receiver works as a general-purpose voltage comparator. Time-to-digital converters (TDC) are used to calculate the timing and energy of the signals. One channel of the FPGA-QDC will consume two general-purpose input/output (GPIO) pins in the FPGA when the SSTL receiver is applied.

To further achieve a more compact design, an FPGA-based QTC (FPGA-QTC) scheme [16] was proposed. The circuit of the FPGA-QTC is a little similar to that of the FPGA-QDC. In this paper, we compared the two FPGA-based charge readout schemes for TOF PET detector applications. Circuit prototypes were built based on the op amp. Two TOF PET detectors consisting of the LYSO crystal bar and SiPM detector were assembled in a light-tight box. All details about the experimental setup will be described as follows.

II. Two FPGA-Based Charge Measurement Schemes

The charge readout schemes of the FPGA-QDC and FPGA-QTC are similar. Currently, both can process not only the negative charge but also positive charge. For simplicity, readout circuits for only negative charge are discussed.

A. Charge Readout Scheme

Both charge readout schemes are illustrated in Fig. 1. In Fig. 1(a), the FPGA-QDC comprises two parts: analog circuit and digital circuit. In the analog circuit, a current pulse from the detector is integrated on a feedback capacitor C_f of the QDC circuit. In the digital circuit, an FPGA achieves all digital functions, such as discharging, data buffering and pulse measurement. An LVDS receiver in the FPGA functions as a voltage comparator. For the LVDS receiver, the input/output bank voltage (V_{IO}) is 2.5 V. When the output signal of the QDC is higher than a preset threshold (V_{Th}), a 3-state buffer turns over from high-Z state to logic '1' . Then, a constant discharge current I_0 is generated, which is equal to V_{IO}/R_{dis}. The discharge time T_{dis} is theoretically Q_{DET}/I_0. The T_{dis} is digitized using a TDC. The timing information is indicated as the time crossing the preset threshold. The discharge process will not terminate until the output signal of the QDC is lower than the threshold V_{Th} once again.

In comparison with the FPGA-QDC, the analog circuit of the FPGA-QTC always discharges with a constant current $I_1 = (V_{dis} - V^+)/R_{dis}$ where V_{dis} and V^+ are applied by two power supplies. Before the arrival of current pulses, the output baseline of the QTC circuit is clamped at ground level through a diode. When the detector current comes, the output voltage of the QTC increases, which in turn makes the diode cut-off. The integrated charge on the feedback capacitor C_f discharges via the I_1. When the integrated charge discharges completely, the output of the QTC goes back to the baseline. Therefore, the width of the output pulse of the QTC is proportional to the injected charge Q. Detailed derivations were shown in our previous paper [16].

B. Charge Calculation

To digitize the pulse width T_{dis}, a 12-bit counter driven by a system clock f_s of 500 MHz was designed. A multiphase counter (MPCNT) with four clock phases [17] was also used to precisely quantify the pulse width, which corresponds to a 14-bit counter driven by an equivalent clock with a frequency $500\text{MHz} \times 4 = 2\text{GHz}$.

Experimentally, the discharging resistor R_{dis} is 5 kΩ and the feedback capacitor is 50 pF. For the FPGA-QDC, the output charge Q of the detector is quantified as [13–15]

$$Q = N \times Q_{LSB} = N \times \frac{V_{IO}}{R_{dis} \times f_s \times 4}$$

where V_{IO} is typically 2.5 V and Q_{LSB} is the Least Significant Bit (LSB) of the charge. However, the charge in the FPGA-QTC is given by [16]

$$Q' = N \times Q'_{LSB} = N \times \frac{V_{dis} - V^+}{R_{dis} \times f_s \times 4}$$

where the value of $V_{dis} - V^{+}$ is set to be 2.5 V. Under this configuration, the least significant bits for both circuits, namely Q_{LSB} and Q'_{LSB}, are the same. Theoretically, the Least Significant Bit (LSB) of the charge is given by $Q_{LSB} =$ 2.5V/(5k × 2GHz) = 0.25 pC.

C. Timing Pickoff

The timing is picked off through the leading edge of the digital pulse after the LVDS receiver. The timing information is digitized by a tapped delay line TDC (TDL-TDC) [18-20]. A 10 ps time resolution can be obtained using the TDL-TDC scheme, which is sufficient for current TOF PET detector evaluation. It has been proven that a resistor R_s in series with the feedback capacitor C_f can improve the timing performance for both circuits [16-21]. For R_s, 25 Ω and 50 Ω are applied.

III. Circuit Implementation

To compare the performance of the FPGA-QDC and FPGA-QTC circuits for TOF PET application, a prototype of a two-channel electronics system was built. The system includes two parts: QDC/QTC analog board and a commercial FPGA development board (KC705, Xilinx), as shown in Fig. 2.

The customized QDC/QTC analog board consists of op amps, a threshold generator, a linear regulator and some passive components. A high-performance op amp (AD8045, ADI) is chosen to integrate and amplify the injected charge signal. Trigger thresholds are generated by a two-channel Digital-to-Analog Converter (DAC70502, Texas Instruments). Due to the structure of the QDC and QTC circuits being very similar, they were designed together so that we can configure the analog board as one of both circuits through choosing the feedback loop of the op amp. The schematic of the analog board is shown in Fig. 3. In normal operation, the analog board was powered up by a $±$5V supply (2231A-30-3, Tektronix), and 36 mA and 45 mA average currents were observed when configured as QDC and QTC circuits respectively.

The KC705 development board is selected as the digital part. All signals, including analog outputs and thresholds, are connected to the KC705 through FPGA Mezzanine Cards (FMC). In the Kintex-7 FPGA, two LVDS receivers are configured as LVDS_{25} standard, working as general-purpose voltage comparators. In the FPGA, the pulse width and timing of signals are digitized by the MPCNT and TDL-TDC respectively. An Ethernet interface is implemented in the FPGA, transferring raw data to a computer. All the post-processings are achieved through ROOT software.

IV. Experimental Setup

To compare the timing performance of both circuits for TOF PET applications, a detector evaluation setup was performed. In the setup, two identical TOF

PET detectors are assembled on an Aluminum rack face-to-face. Each PET detector has a 3 × 3 × 10 mm^3 LYSO crystal bar side-coupled to the 1 × 1 SiPM (MicroFJ-30035, Onsemi). The SiPM is biased at 31 V. Besides the lateral surface coupled to the SiPM, all other surfaces are glued with reflective materials. The 1 × 1 SiPM is assembled on a customized adapter board. The anode and cathode signal of the SiPM are combined together. In the detector evaluation experiment, only the cathode signal of SiPM is connected with the QDC and QTC circuits. The pitch of the SiPM is 3.2 mm. The PET detector including LYSO and SiPM is mounted together using a user-designed holder by a 3-D printer. A Na-22 source was placed between two PET detectors. The whole setup was fixed in a dark box.

V. Results

[FIGURE:2]

At different trigger thresholds, the slew rate of the voltage signals crossing the threshold are not the same, resulting in different CTRs. The threshold can be adjusted at a step of 1 mV through the DAC chip. As mentioned above, the CTR performance will be enhanced when the feedback capacitor is in series with a resistor R_s (R4 in Fig. 3). 25 Ω and 50 Ω are applied to compare the CTR improvement. Fig. 4 shows coincidence energy spectra of the two TOF PET detectors using FPGA-QDC and FPGA-QTC circuits. To select 511 keV gamma photons, a photopeak energy window $(-1\sigma, +1.5\sigma)$ was applied. A Gaussian fitting method was used to calculate the CTR values.

[FIGURE:4]

Fig. 5 shows coincidence timing spectra for the QDC and QTC circuits at the threshold of 2 mV. Fig. 6 shows the plots of timing versus threshold at different series resistors R_s for FPGA-QDC and FPGA-QTC. With the FPGA-QDC circuit, the best CTR value is 335.03 ± 2.00 ps with a trigger threshold of 2 mV and a series resistor of 50 Ω. Using the FPGA-QTC, however, the best CTR value can only reach 357.86 ± 3.31 ps with a trigger threshold of 2 mV and a series resistor of 50 Ω.

[FIGURE:5]

[FIGURE:6]

VI. Discussion

Overall, two FPGA-based charge measurement schemes are very promising for TOF PET applications. With currently abundant FPGA LVDS resources, it is feasible to scale up to a whole TOF PET scanner at a very low cost.

From the view of power dissipation, the QTC circuit consumes more power than that of QDC because of the always-on constant discharge current I_1 (Fig. 1).

However, the discharge current I_0 in the QDC circuit is on only if the injected charge signal crosses the preset threshold.

For the timing analysis, the slew rate of the charge signal crossing the threshold in the QDC can be given by [13]

$$\left.\frac{dV_{out}}{dt}\right|_{t=T_{start}} = \frac{i_D(T_{start}) - \frac{V_{Th}}{R_{dis}+R_L}}{C_f}$$

where T_{start} is the time of crossing the threshold and i_D is the current signal from the TOF PET detector. However, the slew rate at the time T_{start} in the QTC circuit is [22]

$$\left.\frac{dV_{out}}{dt}\right|_{t=T_{start}} = \frac{[i_D(T_{start}) - I_1]}{C_f}.$$

Experimentally, I_1 is equal to $(V_{dis} - V^+)/R_{dis}$, namely 2.5V/R_{dis}. In the coincidence trigger threshold, V_{Th} is less than 15 mV. Then, we obtain $I_1 \gg V_{Th}/(R_{dis}+R_L)$. For both of the FPGA-based charge measurement circuits, the slew rate at the trigger time in the QDC circuit is higher than that in the QTC circuit, which is in agreement with the experimental results in Fig. 6. Besides, the resistor R_s in series with the feedback capacitor C_f further improved the timing performance.

VII. Conclusion

In this paper, we compared the timing performance for two compact FPGA-based charge readout methods, namely the FPGA-QDC and FPGA-QTC. The improvement of the timing performance was described in detail. The resistor in series with the feedback capacitor in both circuits further enhanced the timing performance. Experimental results show that the timing performance of the FPGA-QDC circuit is better than that of the FPGA-QTC. Taking advantage of multi I/O resources in the FPGA, it is feasible to build up hundreds of charge measurement circuits based on a single FPGA.

VIII. Acknowledgement

All the authors declare that they have no known conflicts of interest in terms of competing financial interests or personal relationships that could have an influence or are relevant to the work reported in this article.

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