A novel digital multi-channel analyzer for silicon drift detectors with stable energy resolution at high count rates

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Abstract

Conventional digital multi-channel analyzers (DMCAs) for silicon drift detectors (SDDs) employ CR differentiation circuits for pulse signal extraction. The non-ideal characteristics of the coupling capacitor cause signal tailing distortion after differentiation, exacerbating baseline drift and fluctuation, which leads to the degradation of energy resolution with increasing input count rate. To address this issue, this study proposes an innovative DMCA architecture using subtractor-based active pulse extraction technique. In this architecture, a digital-to-analog converter dynamically tracks the output of the charge-sensitive preamplifier, and the incident particle pulse signals are extracted with a subtractor circuit, thereby eliminating the need for an AC coupling capacitor and the associated signal distortion. This paper first introduces the characteristics of the SDD' s output signal and the factors affecting energy resolution, and then reveals the signal distortion caused by the CR differentiator through practical measurement. Subsequently, the hardware design and the key algorithms implementation of the proposed new DMCA were described in detail, followed by an experimental comparison with the CR configuration. Experimental results demonstrate that the newly developed DMCA exhibits excellent energy resolution stability, maintaining a resolution of 126.7$±$0.3 eV for the 5.89 keV X-rays across the input count rate range of 10 to 500 kcps. In contrast, the resolution of the CR differentiation scheme deteriorates significantly with input count rate, increasing from 124.7 to 133.3 eV. This study overcomes the critical challenge of resolution deterioration for DMCAs under high count rates, paving the way for the application of SDD in high-flux scenarios.

Full Text

Preamble

A Novel Digital Multi-Channel Analyzer for Silicon Drift Detectors with Stable Energy Resolution at High Count Rates

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Conventional digital multi-channel analyzers (DMCAs) for silicon drift detectors (SDDs) employ CR differentiation circuits for pulse signal extraction. However, the non-ideal characteristics of the coupling capacitor cause signal tailing distortion after differentiation, which exacerbates baseline drift and fluctuation and leads to degradation of energy resolution with increasing input count rate. To address this issue, this study proposes an innovative DMCA architecture using a subtractor-based active pulse extraction technique. In this architecture, a digital-to-analog converter dynamically tracks the output of the charge-sensitive preamplifier, and incident particle pulse signals are extracted using a subtractor circuit, thereby eliminating the need for an AC coupling capacitor and the associated signal distortion. This paper first introduces the characteristics of the SDD output signal and the factors affecting energy resolution, then reveals the signal distortion caused by the CR differentiator through practical measurements. Subsequently, the hardware design and key algorithm implementation of the proposed new DMCA are described in detail, followed by an experimental comparison with the CR configuration. Experimental results demonstrate that the newly developed DMCA exhibits excellent energy resolution stability, maintaining a resolution of 126.7 $\pm$ 0.3 eV for 5.89 keV X-rays across an input count rate range of 10 to 500 kcps. In contrast, the resolution of the CR differentiation scheme deteriorates significantly with input count rate, increasing from 124.7 eV to 133.3 eV. This study overcomes the critical challenge of resolution deterioration for DMCAs under high count rates, paving the way for SDD applications in high-flux scenarios.

Keywords: Silicon Drift Detector, Digital Multi-Channel Analyzer, High count rates, Energy resolution, FPGA

Introduction

Silicon drift detectors (SDDs) offer numerous advantages including high count rate capability, excellent energy resolution, and convenient cooling via compact thermoelectric coolers (TECs) [1–5]. Consequently, SDDs [6] have found extensive application in various nuclear technology fields such as X-ray fluorescence (XRF) spectrometry, scanning electron microscopy (SEM), synchrotron light sources, space science, astrophysics, and particle physics [7–13]. Energy resolution and count rate are key metrics for evaluating SDD and associated electronics system performance. With the continuous evolution of application demands—such as synchrotron radiation and free-electron laser facilities—and the ever-increasing power of X-ray sources, SDD systems are confronted with progressively higher X-ray flux. Consequently, preserving excellent energy resolution at high count rates has become a critical challenge for electronic system design.

SDD systems typically employ a reset-type charge-sensitive preamplifier followed by a digital multi-channel analyzer (DMCA) based on trapezoidal filtering [14–17] for signal acquisition. When an X-ray strikes the SDD, it generates a pulse of current that is integrated on the feedback capacitor of the preamplifier, resulting in a step voltage pulse output. By measuring the amplitude of this voltage step, the energy of the incident X-ray photon can be determined. Due to the inherent leakage current of the SDD, the output of the charge-sensitive preamplifier is a superposition of a ramp signal caused by leakage current and step pulses generated by incident particles [18, 19]. Typically, the output signal range of the preamplifier is much greater than the voltage step produced by a single X-ray event. For instance, with a typical gain of 3–5 mV/keV for SDD probes from Amptek and KETEK, the signal amplitude for 5.89 keV X-rays from a commonly used ^{55}Fe radioactive source is only approximately 18–30 mV [20, 21], whereas the preamplifier output spans several volts. To reduce the impact of ADC quantization noise and utilize the full scale of the ADC, the step pulse signals from incident particles must be extracted and amplified prior to digitization.

Currently, DMCAs for SDDs commonly employ a CR differentiation circuit (high-pass filter) [22–26] to block the slowly varying ramp signal caused by leakage current, thereby extracting the pulse signal of incident particles for further amplification. However, experimental results reveal an inherent drawback in this simple approach: the non-ideal characteristics of the coupling capacitor, such as dielectric absorption (DA) and equivalent series resistance (ESR), cause distortion in the CR-differentiated pulse signal, manifesting as a long tailing effect. At high count rates, this distortion significantly exacerbates baseline drift and fluctuation, severely deteriorating the system' s energy resolution and ultimately limiting detection system performance in high-flux scenarios. Consequently, mitigating the signal distortion introduced by AC coupling has become a critical challenge for improving energy measurement accuracy at high count rates.

To address this inherent drawback of CR differentiation circuits, this paper proposes an innovative DMCA architecture using a subtractor-based active pulse extraction technique. In this approach, a digital-to-analog converter (DAC) dynamically tracks the output signal of the preamplifier. The extraction of the incident particle pulse is achieved by subtracting the DAC output signal from the preamplifier' s output, followed by subsequent amplification. This approach utilizes DC coupling and does not require an AC coupling capacitor, thereby eliminating signal distortion caused by the capacitor' s non-ideal characteristics at its source. This paper first introduces the characteristics of the SDD output signal and the factors affecting energy resolution, then reveals the signal distortion caused by the CR differentiation circuit through practical measurements. Subsequently, the hardware design and key algorithm implementation of the proposed new DMCA are described in detail. Finally, comparative experimental tests are presented to validate the significant advantage of the new design in maintaining high resolution at high count rates. This research overcomes the limitation of deteriorated resolution in conventional DMCAs at high count rates, enabling the expansion of SDDs into high-flux applications.

II. Output Signal of SDD and Energy Resolution

An SDD is typically integrated with peripheral circuits such as a charge-sensitive preamplifier, thermoelectric cooler (TEC), temperature sensor, high-voltage distribution circuit, and reset control circuit into a single package, referred to in this paper as an SDD probe. For charge-sensitive preamplifiers, the reset-type architecture is typically employed to eliminate thermal noise from the resistor in RC feedback charge-sensitive preamplifiers. Driven by the inherent leakage current in the SDD itself and the pulsed current generated by incident particles, the output of the reset-type charge-sensitive preamplifier is a superposition of a ramp signal caused by leakage current and step pulses corresponding to incident particles. When the preamplifier output signal exceeds a certain threshold, the reset control circuit generates a reset signal to discharge the integration capacitor, allowing a new integration cycle to begin [27–29]. Figure 1 shows the measured waveform of the preamplifier output from a KETEK VIAMP series SDD probe measured with a ^{55}Fe source. With a typical gain of 5 mV/keV, the signal amplitude for the 5.89 keV X-ray from the ^{55}Fe source is only about 30 mV, while the swing of the preamplifier output signal is approximately 2 Vpp (with reset thresholds of about $±$0.975 V).

The energy resolution of an SDD system is determined by both the SDD itself and the readout electronics, which can be calculated by Eq. (1) [30], where σ_{Fano} represents the contribution from statistical fluctuations of the ionization process (Fano distribution), setting the fundamental resolution limit of the detector. σ_C represents the contribution from charge collection efficiency. σ_E refers to the contribution of electronic noise (including noise from the preamplifier, subsequent amplification circuits, and the ADC) after digital filtering.

$$FWHM = 2.355\sqrt{\sigma_{Fano}^2 + \sigma_C^2 + \sigma_E^2}$$

The energy resolution was evaluated by measuring the full width at half maximum (FWHM) at the 5.89 keV line of a ^{55}Fe radioactive source. Using an average ionization energy = 3.62 eV for silicon and the Fano factor of F = 0.117 [31], the Fano-limited energy resolution FWHM_{Fano} is approximately 118 eV, as calculated by Eq. (2) and Eq. (3) [32].

$$\sigma_{Fano} = \sqrt{F \cdot E \cdot \varepsilon} \approx 49.95 \text{ eV}$$

$$FWHM_{Fano} = 2.355 \cdot \sigma_{Fano} \approx 117.62 \text{ eV}$$

Achieving resolution close to the theoretical limit requires careful design of the entire signal chain, including the SDD, preamplifier, amplifier circuit, and ADC acquisition circuit. As previously mentioned, the amplitude of the preamplifier output signal corresponding to a 5.89 keV incident X-ray photon is only a few tens of millivolts. To reduce the impact of ADC quantization noise and utilize the full scale of the ADC, the step signals must be sufficiently amplified so they can be accurately digitized by the ADC. Each step in the preamplifier output is superimposed on a baseline that can be several volts in magnitude and varies over time. Therefore, it is necessary to eliminate the baseline and extract the step signals before amplification.

[Figure 1: see original paper] shows the schematic block diagram of the DMCA using a CR differentiator, while [Figure 2: see original paper] illustrates the signal distortion caused by the analog CR differentiator.

III. Signal Distortion Caused by the CR Differentiator

To extract and amplify the step pulse signals superimposed on the slowly varying ramp baseline, DMCAs for SDDs commonly adopt a CR differentiation circuit, as illustrated in [Figure 2: see original paper]. In practical measurements, it was observed that trapezoidal pulses shaped from the analog CR differentiator output exhibit a long tailing distortion, which is attributed to the non-ideal characteristics of the coupling capacitor, particularly the dielectric absorption effect.

Figure 3: see original paper shows the signal from the SDD preamplifier output as captured by an oscilloscope, and the resulting waveform after CR differentiation (C = 6.8 nF, R = 470 Ω). An inverse transform technique (CR-INV) was employed [33, 34] to reconstruct the step pulse from the CR-differentiated signal and compare it with the original step pulse output from the charge-sensitive preamplifier. The algorithm for the CR-INV transformation is given by Eq. (4) [33], where k_I = T_s/(RC), and T_s denotes the ADC sampling period.

$$x[n] = k_I \sum_{i=0}^{n} y[i] + y[n]$$

As shown in Figure 3: see original paper, compared to the original signal output from the preamplifier, the step waveform reconstructed via the CR-INV inverse transform exhibits a noticeable slope in the plateau region. This observation is consistent with phenomena reported in literature [34] and is attributed to prolonged tailing distortion present in the signal after CR differentiation. We also compared different coupling capacitors, including ceramic capacitors with different dielectrics (C0G, X7R) and polypropylene capacitors. The distortion effect was observed across all types, with the polypropylene capacitor exhibiting the minimal distortion. This non-ideal response results in baseline drift in the shaped trapezoidal signal. Figure 3: see original paper shows the waveforms resulting from trapezoidal shaping of two distinct signals: one is the output of the analog CR differentiator, and the other is the signal derived from the preamplifier output after ideal digital CR differentiation. The digital CR differentiation and trapezoidal shaping were both implemented in MATLAB. It can be clearly observed that the trapezoidal pulse shaped from the analog CR differentiator output also exhibits a long tail and fails to return to baseline. In contrast, the trapezoid shaped from the ideal digital CR differentiator output experiences no tailing or baseline drift issues.

IV. DMCA for SDD Using Subtractor-Based Active Pulse Extraction

To address the inherent limitations of the CR differentiator discussed above, this paper proposes an innovative DC-coupled DMCA architecture using subtractor-based active pulse extraction (referred to as DMCA-DAC). By utilizing a digital-to-analog converter (DAC) to dynamically track the output signal of the preamplifier, the incident particle pulse signal is extracted through subtraction of the DAC output signal from the preamplifier output. This approach fundamentally eliminates signal distortion caused by the non-ideal characteristics of the AC-coupling capacitor.

A. Hardware Design of the DMCA-DAC

The hardware architecture of the DMCA-DAC is shown in [Figure 4: see original paper]. Compared to the traditional architecture shown in [Figure 2: see original paper], the CR differentiator has been replaced by a subtractor circuit combined with a DAC. The preamplifier output signal is split into two paths. One path is fed to channel A of the ADC for real-time computation of the DAC tracking algorithm. The other path goes to a subtractor circuit, where the bias voltage generated by the DAC is subtracted, followed by subsequent amplification. The gain of the amplification stage is software-configurable, and the amplified signal is then acquired by channel B of the ADC for pulse height

spectrum measurement. To implement these functions, this design employs a dual-channel ADC (AD9251, 14-bit/80 Msps) combined with a high-speed DAC (AD9767, 14-bit). Both devices operate at 80 Msps under the control of an FPGA (AMD/XILINX, XC7A100T-2CSG324). A photograph of the assembled DMCA-DAC circuit board is presented in [Figure 5: see original paper]. Currently, the SDD probe interface is designed according to KETEK' s specifications, but it can be easily adapted to probes from other manufacturers.

For comparative testing, the DMCA-DAC can also be configured to operate in a mode that uses a CR differentiator (by bypassing the subtractor and modifying some components), referred to as DMCA-CR in the following text. The DMCA-DAC can also be configured for a no-amplification mode (by bypassing both the subtractor and amplification circuit), in which the ADC directly samples the preamplifier output without amplification. This configuration is referred to as DMCA-NA in subsequent sections.

As shown in [Figure 4: see original paper], in addition to the amplification circuit, fast ADC, and FPGA, the system includes supporting circuits such as a high-voltage power supply, low-voltage power supply, temperature measurement ADC, TEC power supply, and Ethernet interface circuit. The FPGA runs the SiTCP firmware [35] to communicate with the host PC over a 100-Mbps Ethernet link using standard TCP and UDP protocols. The high-voltage power supply module provides a low-noise bias voltage for the SDD with an output range of -200 V to 0 V, which can be set via host computer software. The low-voltage power supply provides the required $±$5 V power rails for the SDD probe. The output of the SDD probe' s built-in temperature sensor is sampled by an ADC (12-bit, 200 ksps). The TEC power supply is then adjusted via a DAC. Combined with a PID algorithm implemented in the FPGA, this achieves constant temperature control, allowing users to simply set the desired temperature.

B. Digital Pulse Processing Algorithm

The flowchart of the digital pulse processing algorithm is shown in [Figure 6: see original paper], which primarily includes a fast triangular filter (for trigger generation), a trapezoidal filter, a baseline calculator, a pile-up rejector, and a peak detector. Additionally, a baseline monitoring module is incorporated to collect statistics on the baseline of valid pulses, providing valuable information for parameter configuration and system debugging. During operation, key performance metrics including the input count rate (ICR), output count rate (OCR), and dead time are calculated in real-time. Furthermore, to facilitate debugging, a waveform sampling module is implemented, allowing waveforms from internal key nodes to be captured and transmitted back to the host computer for analysis and display. The current implementation supports acquisition of up to 4 analog signals and 8 digital signals.

The trapezoidal filter is implemented based on the unfolding-synthesis tech-

nique [36, 37], which enables flexible synthesis of pulse waveforms with arbitrary shapes. The recursive expressions for trapezoidal shaping are given by Eqs. (5)-(8) [36, 37], and the corresponding algorithm structure is shown in [Figure 7: see original paper]. In this algorithm, LE represents the rise time, PE the flat-top time, and TE the fall time of the trapezoid pulse. Specifically, when PE is set to zero, a triangular pulse can be formed.

$$y_1(n) = h_{N1}(n) - h_{N1}(n-1)$$

$$y_2(n) = M[h_{N2}(n) - h_{N2}(n-1)] + h_{N2}(n-1)$$

$$h_{N1}(n) = \frac{1}{1 - e^{-\Delta T/\tau}}[\delta(n) - \delta(n - LE)]$$

$$h_{N2}(n) = \frac{1}{1 - e^{-\Delta T/\tau}}[\delta(n - LE - PE - TE) - \delta(n - LE - PE)]$$

The trigger logic is based on a fast triangular filter. The output of this filter is differentiated to generate a bipolar pulse. When the amplitude of the fast triangular pulse exceeds a set trigger threshold, the system begins to detect the zero-crossing point of the bipolar pulse, which corresponds to the peak of the fast triangular pulse. Compared to a simple threshold-crossing trigger, using an armed zero-crossing trigger avoids timing uncertainties caused by variations in the threshold setting.

Accurate baseline calculation and pile-up pulse rejection are crucial for achieving high resolution, particularly under high counting rate conditions. A gated moving average filter was adopted for baseline calculation, where the number of averaging points can be configured via software. When a trigger signal is generated, the baseline calculation module is frozen, and the current calculated value is recorded. The baseline calculation module remains inactive until the pulse shaping process is completed. Additionally, a baseline monitoring module has been added which performs real-time statistics on the baselines of all valid events during energy spectrum acquisition. This allows users to set appropriate baseline limit parameters based on the baseline distribution to further discard events with abnormal baseline. The pile-up rejection logic utilizes an internal state machine. When a trigger signal is generated, the state machine is activated. If no new trigger signal arrives before the peak valid signal is asserted, the event is considered valid and recorded. Otherwise, it is identified as a pile-up event and discarded.

C. Dynamic Baseline Tracking Algorithm

As previously stated, channel A of the ADC samples the signal from the preamplifier output, while channel B samples the amplified difference between the preamplifier output and the tracking DAC output. Assume that at the initial moment, the preamplifier output and the DAC output are both zero, and consequently, the value sampled by ADC channel B is also zero. Subsequently, driven by the detector leakage current and the pulsed current introduced by incident particles, the output voltage of the preamplifier begins to rise over time. When the signal sampled by ADC channel B reaches a preset threshold (e.g., 4/5 of the ADC' s full scale), the tracking DAC output is updated with a new value corresponding to the current reading from channel A of the ADC, which represents the instantaneous voltage of the preamplifier output at that moment. After the tracking DAC updates, the difference between the preamplifier output and the DAC output returns to zero and starts to rise again over time. This cycle repeats until the preamplifier output itself reaches saturation, triggering a reset of both the preamplifier and the DAC output, as illustrated in [Figure 8: see original paper].

D. PID Temperature Control Algorithm

A stable operating temperature is a prerequisite for ensuring high energy resolution of the SDD. Temperature control is achieved by sampling the SDD probe' s temperature sensor output via an ADC and adjusting the TEC power supply with a DAC, managed by a PID algorithm embedded in the FPGA. The incremental PID (Proportional-Integral-Derivative) algorithm is used, which calculates the change or increment in the control output rather than the absolute output value itself [38]. The control output is determined by the difference between the current and previous control outputs, calculated using the formula:

$$\Delta u(k) = K_p[e(k) - e(k-1)] + K_i e(k) + K_d[e(k) - 2e(k-1) + e(k-2)]$$

Here, Δu(k) is the incremental change in the control output at the current time step. K_p, K_i, and K_d are the proportional, integral, and derivative gains, respectively. e(k), e(k-1), and e(k-2) are the error signals at the current (k), previous (k-1), and two-steps-previous (k-2) sample times, respectively. The control output at the current time step is updated based on the previous output and the calculated increment: u(k) = u(k-1) + ΔU(K).

E. Host Computer Software Development

A host computer software application was developed based on LabVIEW to communicate with the DMCA via TCP and UDP protocols, achieving functionalities such as parameter configuration, energy spectrum display, and waveform acquisition. [Figure 9: see original paper] shows the interface of the waveform

acquisition function, displaying the waveforms of some key internal signals (e.g., the shaped trapezoid, trigger signal, peak-valid signal, etc.) acquired by the aforementioned waveform sampling module in the firmware.

V. Experimental Results

The performance of the newly developed DMCA-DAC in this study was evaluated and compared with the CR-differentiator (DMCA-CR) and no-amplification (DMCA-NA) modes, using a KETEK SDD probe (model VIAMP-KC 3.0 H20) equipped with an SDD having an active area of 20 mm^2. The preamplifier output of the probe has a signal swing of 2 Vpp, which matches the input range of the AD9251, allowing for direct acquisition without amplification. All experiments were conducted using a uniform set of parameters. The SDD was operated at -45 °C with a bias voltage of -168 V. The trapezoidal shaping parameters were set to a 1 µs rise time, 0.3 µs flat-top time, and 1 µs fall time. For the DMCA-DAC and DMCA-CR, the amplification gain was adjusted to achieve a consistent dynamic range of 40 keV. The preamplifier reset interval (i.e., the time window after a reset during which data acquisition is prohibited) was uniformly set to 5 µs. A photograph of the experimental setup is shown in [Figure 10: see original paper].

An ^{55}Fe radioactive source was employed in the experiment. By varying the distance between the source and the detector, different input count rates (ICRs) were obtained to conduct performance tests of energy resolution and output count rate (OCR). ICR refers to the event rate of radiation interacting with the detector, while OCR refers to the event rate measured by the electronic system. They are calculated respectively as follows:

$$ICR = TrigCnt/LiveTime$$

$$OCR = EventCnt/RealTime$$

TrigCnt is the number of trigger pulses generated according to the trigger logic described in Section IV B, while LiveTime refers to the total duration for which the output of the fast triangular filter remains below the trigger threshold. EventCnt refers to the total number of valid events in the final output spectrum. RealTime represents the total data acquisition time, which is the total run time minus the dead time introduced by preamplifier resets and tracking DAC output updates. The energy resolution is defined as the full width at half maximum (FWHM) of the 5.89 keV Mn-Kα peak in the acquired energy spectrum, obtained by performing a Gaussian fit in MATLAB.

A. Temperature Control

[Figure 11: see original paper] shows the temperature curve of the SDD after the

target temperature was set and the PID algorithm was enabled. After approximately 70 seconds, the probe temperature decreased from room temperature to the target level, after which it remained constant, with fluctuations kept within $±$0.15 °C. Data acquisition was initiated only after the target temperature was reached.

B. Energy Resolution and OCR

[Figure 12: see original paper] shows the measured energy resolution versus ICR for the three configurations. As an example, [Figure 13: see original paper] presents a representative energy spectrum measured with the DMCA-DAC at an ICR of 300 kcps. For the DMCA-NA configuration with no amplification, the overall energy resolution is relatively poor, measuring only 134.66 ± 0.66 eV. This is primarily because ADC noise has a more significant impact when the signal amplitude is small, confirming that amplifying low-amplitude step signals prior to ADC digitization is essential for obtaining high energy resolution.

The DMCA-CR achieves a good resolution of 124.71 eV at low ICR. However, its performance degrades significantly with increasing ICR, deteriorating to 133.29 eV at 500 kcps. A similar phenomenon of energy resolution degradation with increasing ICR was also observed in Refs. [23, 39], which employed DMCAs based on CR differentiators. In contrast, the DMCA-DAC maintains a stable resolution of 126.75 ± 0.25 eV across the entire tested ICR range. At low ICR levels, the DMCA-DAC exhibits slightly inferior resolution compared to the DMCA-CR, primarily attributed to additional noise introduced by the DAC and subtractor circuit, which will be further optimized in future improvements.

[Figure 14: see original paper] shows the OCR as a function of ICR for the three configurations under the same pile-up rejection criterion. The three configurations exhibit nearly identical performance when the ICR is below 100 kcps. As the ICR continues to increase, the DMCA-DAC shows a slightly lower OCR performance than the DMCA-CR (approximately 10% lower at an ICR of 500 kcps), primarily due to the additional brief data acquisition inhibit time introduced during tracking DAC update adjustments.

C. Baseline Drift and Fluctuation

Baseline drift and fluctuation can be conveniently analyzed using the baseline monitoring module described in Section IV B. In an ideal case, the baseline distribution should be Gaussian-shaped and centered at zero. The statistical baseline distributions for valid events at different ICRs are presented in [Figure 15: see original paper], and the baseline centroids at different ICRs are shown in [Figure 16: see original paper]. For the DMCA-CR, a certain degree of baseline drift is observed. This drift increases with higher ICR, accompanied by significantly intensified fluctuations, which constitutes the primary cause for degradation of energy resolution with increasing ICR. In contrast, the DMCA-DAC maintains Gaussian distributions symmetric about zero across the tested

ICR range, with no noticeable change in distribution broadening. This clearly demonstrates the significant effectiveness of the novel design presented in this work in maintaining baseline stability.

VI. Conclusion

To address the issue of signal distortion caused by CR differentiators in traditional SDD DMCAs, which leads to deterioration of energy resolution at high count rates, this paper proposes and develops a novel DMCA for SDDs using subtractor-based active pulse extraction. By dynamically tracking the preamplifier output with a DAC and extracting incident particle pulse signals using a subtractor circuit, this approach eliminates the need for an AC coupling capacitor and the associated signal distortion.

In this study, the hardware of the proposed DMCA-DAC was developed, along with the corresponding digital pulse processing algorithms and host computer software, implementing functions such as trapezoidal filtering, pulse pile-up rejection, baseline monitoring, and waveform sampling. Comparative experiments demonstrate that the newly developed DMCA-DAC exhibits exceptional baseline stability, achieving a stable and excellent energy resolution of 126.7 $\pm$ 0.3 eV across a wide input count rate range of 10 to 500 kcps. In contrast, the CR differentiation scheme suffers from aggravated baseline drift and fluctuation as ICR increases, which directly leads to significant deterioration in energy resolution from 124.7 eV to 133.3 eV. A slight disadvantage of the DMCA-DAC is its marginally lower OCR compared to the CR scheme under high ICR conditions (approximately 10% lower at an ICR of 500 kcps), mainly attributed to the additional brief data acquisition inhibit time introduced during tracking DAC update adjustments.

At low count rates, the resolution of the DMCA-DAC is slightly inferior to that of the CR scheme due to additional noise introduced by the DAC and subtractor circuit, which will be further optimized in the next step to improve energy resolution toward its theoretical limit. Furthermore, the current design employs a dual-channel ADC, utilizing one independent channel to acquire the preamplifier output signal for baseline tracking. Theoretically, the amplitude of the preamplifier output can be calculated based on the amplified signal' s amplitude, the gain factor, and the DAC output. Therefore, subsequent work will focus on developing a single ADC implementation to simplify the system architecture and reduce cost.

References

[1] P. Lechner, C. Fiorini, R. Hartmann et al., Silicon drift detectors for high count rate X-ray spectroscopy at room temperature. Nucl. Instrum. Meth. A 458, 281-287 (2001). https://doi.org/10.1016/S0168-9002(00)00872-X

[2] G. Zampa, A.Rashevsky, A. Vacchi, The X-Ray Spectroscopic Performance

of a Very Large Area Silicon Drift Detector. IEEE Trans. Nucl. Sci. 56, 832-835 (2009). https://doi.org/10.1109/TNS.2008.2007955

[3] G. Bertuccio, M. Ahangarianabhari, C. Graziani et al., A Silicon Drift Detector-CMOS front-end system for high resolution X-ray spectroscopy up to room temperature. J. Instrum. 10, P01002 (2015). https://doi.org/10.1088/1748-0221/10/01/P01002

[4] G. Bertuccio, M. Ahangarianabhari, C. Graziani et al., X-ray silicon drift detector-CMOS front-end system with high energy resolution at room temperature. IEEE Trans. Nucl. Sci. 63, 400-406 (2016). https://doi.org/10.1109/TNS.2015.2513602

[5] B.G. Lowe, R.A. Sareen, Semiconductor X-Ray detectors, 1st edn. Taylor & Francis Group, Bosa Roca, 2017.

[6] E. Gatti, P. Rehak, Semiconductor drift chamber —An application of a novel charge transport scheme. Nucl. Instrum. Meth. 225, 608-614 (1984). https://doi.org/10.1016/0167-5087(84)90113-3

[7] E. Margui, R. van Grieken, X-Ray fluorescence spectrometry and related techniques: An introduction, Momentum Press, New York, 2013.

[8] I. Hafizh, M. Carminati, C. Fiorini, TERA: Throughput-Enhanced Readout ASIC for High-Rate Energy-Dispersive X-Ray Detection. IEEE Trans. Nucl. Sci. 67, 1746-1759 (2020). https://doi.org/10.1109/TNS.2020.3001459

[9] F. Wei, S.J. Wang, J.B. Liang et al., Next generation space environment monitor (SEM) for FY-2 satellite series. Chin. J. Geophys. 56, 1-11 (2013). https://doi.org/10.6038/cjg20130101

[10] F. Zhang, H.Y. Wang, W.X. Peng et al., High resolution solar soft X-ray spectrometer. Chin. Phys. C 36, 146-150 (2012). https://doi.org/10.1088/1674-1137/36/2/008

[11] X.H. Fu, C.L. Li, G.L. Zhang et al., Data processing for the active particle-induced X-ray spectrometer and initial scientific results from Chang' e-3 mission. Res. Astron. Astrophys. 14, 1595 (2014). https://doi.org/10.1088/1674-4527/14/12/008

[12] E.L. Chen, C.Q. Feng, S.B. Liu et al., Readout electronics for a high-resolution soft X-ray spectrometer based on silicon drift detector. Nucl. Sci. Tech. 28, 14 (2017). https://doi.org/10.1007/s41365-016-0160-02

[13] T. Ishiwatari, Siddharta Collaboration, Silicon drift detectors for the kaonic atom X-ray measurements in the SIDDHARTA experiment. Nucl. Instrum. Meth. A 581, 326-329 (2007). https://doi.org/10.1016/j.nima.2007.07.137

[14] V.T. Jordanov, G.F. Knoll, A.C. Huber et al., Digital techniques for real-time pulse shaping in radiation measurements. Nucl. Instrum. Meth. A 353, 261-264 (1994). https://doi.org/10.1016/0168-9002(94)91652-7

[15] V.T. Jordanov, G.F. Knoll, Digital synthesis of pulse shapes in real time for high resolution radiation spectroscopy. Nucl. Instrum. Meth. A 345, 337-345 (1994). https://doi.org/10.1016/0168-9002(94)91011-1

[16] C. Imperiale, A. Imperiale, On nuclear spectrometry pulses digital shaping and processing. Measurement 30, 49-73 (2001). https://doi.org/10.1016/S0263-2241(00)00057-9

[17] J.X. Li, H.L. Hou, Y.F. Huang et al., Pulse-shaping method for real-time neutron/gamma discrimination at low sampling rates. Nucl. Sci. Tech. 34, 165 (2023). https://doi.org/10.1007/s41365-023-01306-z

[18] E. Atkin, A. Gusev, A. Krivchenko et al., Low-noise analog readout channel for SDD in X-ray spectrometry. J. Instrum. 11, C01086 (2016). https://doi.org/10.1088/1748-0221/11/01/C01086

[19] Y. Li, K. Zhao, Z. Li et al., The Readout electronics onboard the First Pathfinder (CATCH-1) of the CATCH Constellation Space Mission. Nucl. Instrum. Meth. A 1082, 170977 (2026). https://doi.org/10.1016/j.nima.2025.170977

[20] KETEK. VIAMP Family Product Information, https://www.ketek.net/wp-content/uploads/2025/06/KETEK-VIAMP-Family___{Product}-Information.pdf; 2025 [Accessed 20 November 2025]

[21] Amptek. FAST SDD Ultra High Performance Silicon Drift Detector, https://www.amptek.com/products/x-ray-detectors/fastsdd-x-ray-detectors-for-xrf-eds/fastsdd-silicon-drift-detector; 2025 [Accessed 20 November 2025]

[22] G. Blaj, C.J. Kenney, A. Dragone et al., Optimal Pulse Processing, Pile-Up Decomposition, and Applications of Silicon Drift Detectors at LCLS. IEEE Trans. Nucl. Sci. 64, 2854-2868 (2017). https://doi.org/10.1109/TNS.2017.2762281

[23] S. Saxena, A.I. Hawari, Digital pulse deconvolution with adaptive shaping for real-time high-resolution high-throughput gamma spectroscopy. Nucl. Instrum. Meth. A 954, 161288 (2020). https://doi.org/10.1016/j.nima.2018.09.123

[24] L. Tang, X.K. Ma, K.B. Shi et al., A method for correcting drifted characteristic X-ray count peak. Nucl. Sci. Tech. 34, 175 (2023). https://doi.org/10.1007/s41365-023-01333-w

[25] L. Tang, S. Zhou, K.B. Shi et al., Application of a fusion neural network model with multimodal for fluorescence spectroscopy. Nucl. Sci. Tech. 35, 178 (2024). https://doi.org/10.1007/s41365-024-01528-9

[26] S.P. Wang, N. Pan, S.Q. Gu et al., Deep learning-based electronics architecture for pulse pile-up correction in synchrotron radiation spectroscopic detection. Nucl. Instrum. Meth. B 566, 165730 (2025). https://doi.org/10.1016/j.nimb.2025.165730

[27] L. Bombelli, C. Fiorini, T. Frizzi et al., "CUBE" , A low-noise CMOS preamplifier as alternative to JFET front-end for high-count rate spec-

troscopy. IEEE NSS Conference Record. Valencia, Spain, 1972-1975 (2011). https://doi.org/10.1109/nssmic.2011.6154396

[28] L.G. Toscano, G. Deda, G. Borghi et al., Read-out Electronics for SDD-based Compton detection in astronomical X-ray polarimetry. J. Instrum. 20, P06055 (2025). https://doi.org/10.1088/1748-0221/20/06/P06055

[29] J.W. Chen, Y.Q. Shi, F.C. Zuo et al., Low-noise read-out electronics design for a solar soft X-ray spectrometer onboard the MSS-1B satellite. Nucl. Sci. Tech. 36, 123 (2025). https://doi.org/10.1007/s41365-025-01699-z

[30] W.G. Song, L.J. Zhang, J. Zhang et al., Research on digital pulse processing techniques for silicon drift detector. Acta. Phys. Sin. 71, 012903 (2022). https://doi.org/10.7498/aps.71.20211062 (in Chinese)

[31] D.M. Schlosser, P. Lechner, G. Lutz et al., Expand detection efficiency silicon drift detectors. Nucl. Instrum. Meth. A 624, 270-276 (2010). https://doi.org/10.1016/j.nima.2010.04.038

[32] M.N. Mazziotta, Electron–hole creation energy and Fano factor temperature dependence in silicon. Nucl. Instrum. Meth. A 584, 436-439 (2008). https://doi.org/10.1016/j.nima.2007.10.043

[33] H.P. Wang, J.B. Zhou, X.P. Ouyang et al., Application of pole-zero cancellation circuit in nuclear signal filtering and shaping algorithm. Nucl. Sci. Tech. 32, 86 (2021). https://doi.org/10.1007/s41365-021-00916-9

[34] X.Y. Wang, J.B. Zhou, M. Wang et al., Signal modeling and impulse response shaping for semiconductor detectors. Nucl. Sci. Tech. 33, 46 (2022). https://doi.org/10.1007/s41365-022-01050-0

[35] Bee Beans Technologies Co., Ltd. SiTCP Manual, https://www.sitcp.net/doc/SiTCP_{eng}.pdf; 2025 [Accessed 20 November 2025]

[36] V.T. Jordanov, Unfolding-synthesis technique for digital pulse processing. Part 1: Unfolding. Nucl. Instrum. Meth. A 805, 63-71 (2016). https://doi.org/10.1016/j.nima.2015.07.040

[37] V.T. Jordanov, Unfolding-synthesis technique for digital pulse processing. Part 2: Synthesis. Nucl. Instrum. Meth. A 1044, 167421 (2022). https://doi.org/10.1016/j.nima.2022.167421

[38] Q. Wang, Z.K. Yao, Y. Zhang et al., High accuracy temperature control system of DBR laser based on ADN8834. Chinese Journal of Liquid Crystals and Displays 38, 609 (2023). https://doi.org/10.37188/CJLCD.2023-0068 (in Chinese)

[39] S. Saxena, A.I. Hawari, Investigation of FPGA-Based Real-Time Adaptive Digital Pulse Shaping for High-Count-Rate Applications. IEEE Trans. Nucl. Sci. 64, 1733-1738 (2017). https://doi.org/10.1109/TNS.2017.2692219

Note: Figure translations are in progress. See original paper for figures.