The Impact of Ion Strike Time Intervals on Single Event Effect in a 28 nm FPGA

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Abstract

Advanced nanoscale devices are core components in modern aerospace systems. The on-orbit reliability of the devices faces challenges from Single Event Effects (SEEs) induced by high-energy particles in space. The ground-based irradiation testing is a critical method for predicting on-orbit performance. However, the ground test is an accelerated testing method. The influence of ion strike time intervals (i.e., ion flux) on the SEE sensitivity of advanced nanoscale devices is not yet fully understood. This problem can lead to inaccurate reliability assessment. In this work, the impact of ion strike time intervals on the Single Event Upset (SEU) has been investigated systematically in a 28 nm Static Random Access Memory based (SRAM-based) Field Programmable Gate Array (FPGA). The ground-based irradiation experiments were conducted using various heavy ions under well controlled ion flux levels. The experimental results definitively demonstrate that the device's SEU cross section increases significantly as the ion strike time interval decreases. It shows when the flux exceeds 1000 ions/($\mathrm{cm}^2 \cdot$ s), the cross section exhibits changes, while it remains unchanged at the flux below 1000 ions/($\mathrm{cm}^2 \cdot$ s). Moreover, the flux of 1000 ions/($\mathrm{cm}^2 \cdot$ s) is significantly lower than the typical flux used in SEE testing. This phenomenon was more pronounced at lower core voltages and higher Linear Energy Transfer (LET) values. The analysis reveals that the voltage drop induced by transient pulse from heavy ions is the primary physical mechanism which responsible for the flux dependence. Furthermore, the physical mechanism of the experimental phenomena has been elucidated through Technology Computer-Aided Design (TCAD) and circuit-level simulations. Moreover, the mechanism is equally applicable to other advanced nanoscale devices. This finding provides an essential reference for accurate prediction of on-orbit failure rates of the advanced nanoscale devices.

Full Text

Preamble

The Impact of Ion Strike Time Intervals on Single Event Effects in a 28 nm FPGA

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Advanced nanoscale devices are core components in modern aerospace systems, yet their on-orbit reliability faces significant challenges from Single Event Effects (SEEs) induced by high-energy particles in space. Ground-based irradiation testing is a critical method for predicting on-orbit performance, but it represents an accelerated testing approach. The influence of ion strike time intervals (i.e., ion flux) on the SEE sensitivity of advanced nanoscale devices is not yet fully understood, which can lead to inaccurate reliability assessments. In this work, we systematically investigated the impact of ion strike time intervals on Single Event Upsets (SEUs) in a 28 nm Static Random Access Memory-based (SRAM-based) Field Programmable Gate Array (FPGA) through ground-based irradiation experiments using various heavy ions under precisely controlled flux levels. Our experimental results definitively demonstrate that the device' s SEU cross section increases significantly as the ion strike time interval decreases. Specifically, the cross section exhibits changes when the flux exceeds 1000 ions/($\text{cm}^2 \cdot$ s), while remaining unchanged at lower flux levels. Notably, this threshold flux is significantly lower than typical values used in SEE testing. This phenomenon becomes more pronounced at lower core voltages and higher Linear Energy Transfer (LET) values. Our analysis reveals that voltage drop induced by transient pulses from heavy ions is the primary physical mechanism responsible for this flux dependence. We further elucidated this mechanism through Technology Computer-Aided Design (TCAD) and circuit-level simulations, demonstrating its applicability to other advanced nanoscale devices. These findings provide an essential reference for accurately predicting on-orbit failure rates of advanced nanoscale devices.

Keywords: Single Event Effects, Heavy Ions, Nanoscale FPGAs, Ion Strike Time Intervals, Flux Effect

Introduction

Advanced nanoscale devices have become critical components in aerospace applications [1–3], but they are highly susceptible to Single Event Effects (SEEs) caused by energetic particles in the space environment [4,5], which seriously threatens satellite operational lifetime. Ground simulation testing using accelerator-generated ions is therefore essential to ensure radiation hardness reliability. However, significant differences exist between the space radiation environment and ground test conditions. Space particle flux is extremely low [6], resulting in long time intervals between particle strikes on a single device [7,8]. In contrast, ground tests are accelerated, typically employing high flux ions to accumulate statistically significant fluence within practical timeframes [9–13]. Specifically, ion fluxes around 10,000 ions/($\mathrm{cm}^2 \cdot \mathrm{s}$) are commonly used in accelerator simulation experiments, raising the fundamental question of whether SEEs from single ion irradiation can be directly extrapolated to real space conditions [14–17].

Nanoscale Field Programmable Gate Arrays (FPGAs) have been widely adopted in aerospace due to their low cost and high performance characteristics [18–22], attracting considerable attention to their SEE susceptibility. Previous studies have investigated various aspects, including how larger incident angles increase equivalent LET in active regions and lead to higher Multiple Bit Upset (MBU) cross sections [23], proposed methods for extracting Multiple Cell Upsets (MCUs) [24], and analyzed how charge sharing affects MCUs in 28 nm SRAM-based FPGAs [24]. Another study examined the influence of LET and stored data patterns on SEU cross sections in Flash-based FPGAs [25]. However, most ground irradiation tests in these studies were conducted at fluxes exceeding 10,000 ions/($\mathrm{cm}^2 \cdot \mathrm{s}$), which may yield imprecise SEU cross sections, potentially leading to costly over-design in radiation hardening or, conversely, underestimation of actual space operation risks.

Previous research has demonstrated that flux significantly influences device cross sections. A twofold variation in SEU cross section was observed in a 90 nm SRAM-based FPGA depending on ion flux [26], and the cross sections of three different SRAMs increased substantially when flux reached 10,000 ions/($\mathrm{cm}^2 \cdot \mathrm{s}$) [27,28]. Another study noted cross section increases with ion flux in a Xilinx FPGA [29]. These findings underscore the critical importance of conducting flux effect tests on advanced nanoscale devices.

II. Experimental Setups

A. Device Under Test

The Device Under Test (DUT) is the Xilinx XC7K325T FPGA, capable of delivering high-end connectivity, bandwidth, and signal processing capabilities [31]. Fabricated using a 28 nm bulk silicon process with high-K metal gate technology, all programmable routing in the device is controlled by Configuration Random Access Memory (CRAM). Through various configurations, the device can implement complex functions to meet diverse application requirements.

In Xilinx FPGAs, the CRAM is organized into multiple frames, with each frame consisting of a column of memory cells. For the DUT, the CRAM contains 22,546 frames (including 7 dummy frames), and each frame comprises 3,232 bits (101 words of 32 bits each), resulting in a total of 72,846,048 bits. All frame data can be read back, and error data along with logical information about error occurrences (detailed frame and logical locations) can be extracted by comparing it with the golden bitstream.

B. Test System

The test system consists of a motherboard and daughterboard connected via a high-speed interface, both requiring a 12 V DC power supply (ITECH IT6333A). This system enables testing of memory cells, Configurable Logic Blocks (CLBs), and Digital Signal Processing (DSP) modules. During experiments, the DUT on the daughterboard is exposed to ion beam irradiation while the main FPGA on the motherboard sends commands, reads data from the daughterboard, and compares it with the golden bitstream. Experimental upset errors and their logical addresses are saved in log files for further analysis.

C. Experiments

Before presenting the experimental methodology, we clarify the parameter of ion strike time intervals introduced in this study. The beam used in the experiments was pre-characterized by its provider, demonstrating excellent temporal and spatial uniformity. Therefore, ion strike time interval serves as a more intuitive parameter than flux, specifically referring to the time between two ion strikes on the device. This parameter is inversely proportional to flux, and we achieved variation in ion strike time intervals by precisely regulating flux across a range of 50–10,000 ions/($\mathrm{cm}^2 \cdot \mathrm{s}$) to establish different conditions.

Radiation experiments were conducted at two facilities: the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics (IMP), Chinese Academy of Sciences, and the Space Environment Simulation and Research Infrastructure (SESRI) at Harbin Institute of Technology (HIT). The DUT was irradiated using ^{181}Ta, ^{86}Kr, and ^{84}Kr ions. Since the device uses flip-chip packaging, the substrate was thinned to approximately 50 μm to ensure heavy ions could penetrate the device. Experiments were performed at room temperature (20°C) with core voltages of 0.85 V and 1.00 V. We employed a static testing method to prevent unexpected functional errors and reduce burst errors during DUT reconfiguration, thereby improving data acquisition efficiency.

For each ion species, multiple static tests were conducted with constant fluence but varying flux. The static testing process begins with configuring a bitstream onto the DUT, then turning on the ion beam for irradiation. After reaching the preset heavy ion fluence, the beam is turned off, and the post-irradiation bitstream is compared with the golden bitstream to identify SEUs. Multiple static tests are required, and the DUT is reconfigured between tests to restore functionality. By holding fluence constant while varying flux to modulate ion strike time intervals, multiple experimental results can be obtained. A picture of the irradiation test setup is shown in Fig. 2.

The heavy ions (^{181}Ta, ^{86}Kr, and ^{84}Kr) reached the device surface with energies of 2005.5 MeV, 1876.8 MeV, and 506.0 MeV, respectively. Additional detailed experimental parameters are summarized in Table 1.

[Figure 1: see original paper]. Schematic diagram of flip-chip FPGA memory cells irradiation. It illustrates the physical process where heavy ions generate substantial substrate current, leading to significant voltage drops in the PDN, thereby increasing the cross section of memory cells.

III. Experimental Results

The results demonstrate that SEU cross section increases with shorter ion strike time intervals. Unlike previous studies, this research employed a 28 nm device and observed distinct flux effects at 1000 ions/(cm$^2 \cdot$ s), with a maximum cross section increase of up to a factor of two. Factors such as LET and core voltage collectively modulate the degree to which ion strike time intervals affect cross section. These observations are presented in Fig. 3.

The coupling effects between voltage and ion strike time intervals were investigated through irradiation tests with ^{181}Ta ions (LET = 75.4 MeV/(mg/cm^2)) at core voltages of 0.85 V and 1.00 V. As shown in Fig. 3(a), cross section increases as ion strike time intervals decrease for both voltages. At 0.85 V core voltage, the cross section increases by approximately 42% when flux changes from 50 to 10,000 ions/(cm$^2 \cdot$ s), while at 1.00 V, it increases by only about 10% over the same range. These results indicate that device cross section is more significantly affected by ion strike time intervals at lower core voltage, with the flux effect becoming more pronounced. Three additional experimental groups at flux levels of 200, 400, and 700 ions/(cm$^2 \cdot$ s) with 1.00 V core voltage showed essentially unchanged cross section, a phenomenon analyzed in Section V.C.

The coupling effects between LET and ion strike time intervals were investigated using ^{86}Kr ions (LET = 20.5 MeV/(mg/cm^2)) at 0.85 V core voltage. As shown in Fig. 3(b), device cross section still increases as ion strike time intervals decrease. Under constant fluence, when flux changes from 50 to 10,000 ions/(cm$^2 \cdot$ s), cross section increases by approximately 22%. Compared with results at 75.4 MeV/(mg/cm^2) LET and 0.85 V core voltage, this increasing trend is less pronounced, indicating that device cross section is more significantly affected by ion strike time intervals at higher LET conditions, with the flux effect becoming more substantial under elevated LET.

Experiments conducted under shorter ion strike time intervals (higher flux) at 0.85 V core voltage using ^{84}Kr ions (LET = 36.9 MeV/(mg/cm^2)) reveal an even more pronounced effect. As shown in Fig. 3(c), when flux increased from 20,400 to 144,000 ions/(cm^2 · s), cross section approximately doubled—a more pronounced increase than observed with ^{181}Ta ions at 0.85 V core voltage. These findings demonstrate that device cross section becomes more significantly affected by ion strike time intervals within shorter time interval ranges, with the flux effect becoming more pronounced at higher flux ranges.

IV. Discussion

The experimental results from three ion species in Section III demonstrate that the flux effect is not a random phenomenon in 28 nm FPGA devices. In experiments with ^{181}Ta and ^{86}Kr ions, flux effects were observed even at 1000 ions/(cm^2 · s). At such flux levels, ion strike temporal intervals are comparatively long, and multiple ions do not directly interact with each other. Therefore, in smaller technology nodes, a different physical mechanism must be responsible for the flux effect—one that exhibits dependence on LET, core voltage, and the variation range of ion strike time intervals. We conclude that the IR drop effect is the primary cause of cross section variation.

With advancing deep submicron technology focused on reducing power consumption and increasing operating frequency, voltage reduction significantly diminishes transistor noise margins, while increased transistor density leads to critical power density issues. Power distribution across the chip is achieved through metal rails and stripes forming a Power Delivery Network (PDN) [32,33], whose equivalent circuit is shown in Fig. 4. Each metal layer in the PDN has finite resistivity, causing a portion of the applied voltage to drop across the network according to Ohm' s law. This phenomenon, known as IR drop, is widely acknowledged as an inevitable issue that can only be mitigated, not entirely eliminated [34-37]. IR drop includes static IR drop (when no input switching occurs) and dynamic IR drop (when continuous input switching causes PDN voltage fluctuations) [38,39].

In our static tests without input switching during irradiation, the chip generated static current during normal operation without heavy ion strikes. When heavy ion strikes caused bit upsets, the resulting transient current became dynamic current. In such cases, static and dynamic currents together produced transient current surges. IR drop can cause power supply noise and VDD decreases, particularly when sudden current increases from extensive switching activity cause voltage drops. This global phenomenon means current surges generated in one block can influence the entire chip, effectively explaining why higher core voltage reduces the impact of IR drop on cross section, while lower core voltage makes devices more susceptible to upsets and thus more sensitive to IR drop effects. For heavy ions with higher LET, single ions generate stronger transient pulses, making the IR drop phenomenon more pronounced. Similarly, shorter ion strike temporal intervals produce larger transient pulses in the same timeframe, making IR drop more noticeable and its impact on cross section more pronounced.

In practical applications, static current can occur even when gate inputs remain unchanged. In previous-generation larger process node devices, such static current was minimal and typically negligible. However, technology node advancement, accompanied by reductions in operating voltage and gate oxide thickness, leads to increased static current. Furthermore, with higher transistor density in Integrated Circuits (ICs), numerous gates may connect to the same PDN node, causing cumulative static current pulses to reach magnitudes comparable to dynamic current [33]. Therefore, when using advanced small-node devices, the IR drop effect induced by both static and dynamic currents must be considered.

In ground-based irradiation experiments, heavy ion strikes generate electron-hole pairs, causing multiple transistor upsets that induce transient voltage drops in the core voltage through IR drop. Although simulation studies show that static and dynamic current pulses dissipate within 100 ps, the resulting voltage drop can persist until the chip' s voltage regulation module restores the supply voltage to nominal levels. Numerous studies have demonstrated that decreasing core voltage reduces the critical charge of transistors [40], causing device upset cross section to increase under identical ion species and irradiation parameters. Therefore, severe IR drop effects can ultimately lead to flux effects that increase SEU cross section as ion strike time intervals decrease.

Raphael Viera et al. [41] studied IR drop influence on cross section through laser-based fault injection simulations on a 28 nm ARM7 FPGA at 1.00 V core voltage. They noted that traditional fault models focus on localized photocurrent while neglecting IR drop effects from simultaneous laser irradiation of multiple gates. Three simulation scenarios—considering only photocurrent, only IR drop, and their combined interaction—showed that IR drop alone could induce up to 50 mV voltage drop, while combined effects reached 791 mV. Fault statistics revealed that IR drop nonlinearly amplified fault severity, expanding both spatial and temporal susceptibility and increasing fault-prone regions by 30–50%. This was the first study to demonstrate IR drop as a critical factor in fault injection processes, emphasizing that laser-induced IR drop must be considered to avoid underestimating circuit susceptibility.

However, prior research has not explored simulations or experimental studies on IR drop effects induced by heavy ion irradiation, nor has it examined flux influence on IR drop effects. Therefore, our ground-based heavy ion irradiation experiments and simulations validating the proposed flux effect mechanism are crucial for ensuring the safety of advanced nanoscale devices in aerospace applications.

V. Experimental and Simulation Verification

To further demonstrate the impact of IR drop effects, we conducted TCAD and Cadence simulations. TCAD simulations provide transient current pulses from heavy ion strikes, which are incorporated as current sources in Cadence simulations to obtain voltage drops across the PDN.

A. Experimental Verification

To verify the specific mechanism by which ion strike time intervals affect cross section, we conducted supplementary verification experiments at HIRFL in IMP. Using ^{78}Kr ions, these experiments investigated the dependence of the DUT’ s upset cross section on core voltage variations. The DUT’s core voltage was varied across multiple tests while all other parameters remained constant, following the procedure outlined in Section II.B. Detailed experimental parameters are summarized in Table 2.

Although many studies have shown that voltage reduction increases SEU cross section, we conducted ground irradiation experiments on the DUT using ^{78}Kr ions (LET = 16.6 MeV/(mg/cm^2)) at various core voltage levels to ensure analytical rigor. The cross section variation trend with core voltage (0.85 V to 1.00 V) is shown in Fig. 5, confirming that the upset cross section exhibits a clear increasing trend as core voltage decreases.

B. Simulation Verification

To physically quantify the complete current pulse induced by heavy ion strikes, we used the Sentaurus TCAD tool to simulate device transient response. A full-structure Complementary Metal-Oxide-Semiconductor (CMOS) inverter model was constructed, including both PMOS and NMOS transistors along with independent N-well and P-substrate contacts to ensure all electrical interactions between devices, wells, and substrate were considered. Fig. 6 illustrates the simulation structure located at the N-well/P-substrate junction. A heavy ion with LET of 75 MeV/(mg/cm^2) was simulated with normal incidence at the device center, with sufficient range to penetrate the entire structure.

Fig. 7 compares current collection at different terminals after ion strike, revealing that substrate current collected at the N-well contact is significantly larger than transient current at individual MOS transistor drains. This is attributed to the large collection volume provided by the expansive N-well/P-substrate PN junction, further amplified by funneling effects and parasitic bipolar amplification [42]. Consequently, peak well current reached nearly ten times the drain current, indicating that substrate current (component I_{sub} in Fig. 7(c)) is the dominant factor in transient disturbance on the PDN.

For circuit-level verification, substrate current waveforms from TCAD simulation were imported as Piece-Wise Linear (PWL) current sources into Cadence. A 28 nm SRAM array was constructed for circuit-level IR drop simulations with initial voltage set to 0.85 V. The IR drop curve in Fig. 8 reveals a maximum voltage drop approaching 200 mV and minimum drop near 50 mV, clearly showing that substrate current induced by heavy ions significantly affects circuit voltage drop, which can substantially impact SEU cross section of memory cells.

Voltage drop statistics from each node were compiled to generate a 2D spatial voltage drop distribution heat map (Fig. 9). The spatial distribution shows that voltage degradation spreads to surrounding memory cells, causing voltage degradation across entire blocks. This non-local character of IR drop is critical for understanding flux effects, implying that consecutive ion strikes only need to have overlapping influence regions in space, rather than hitting the exact same transistor or memory cell.

C. Mechanism of Ion Strike Time Intervals Affecting Device Cross Section

The experiments in Section V.A confirm the dependence of device cross section on core voltage, while simulations in Section V.B demonstrate that heavy ion strikes induce significant voltage degradation. Both results support our proposed mechanism for ion strike time interval influence on cross section, which correctly explains why cross section changes become more significant under conditions of higher LET ions, shorter ion strike time intervals, and lower core voltage. Higher LET ions generate larger transient currents, producing larger voltage drops. Shorter ion strike time intervals cause sufficient voltage drops before voltage regulation takes effect, triggering cross section changes. Lower core voltage makes circuits more sensitive, causing cross section to exhibit stronger dependence on ion strike time intervals.

To identify the onset threshold of the flux effect, additional irradiation tests using ^{181}Ta ions at 1.00 V core voltage were conducted with three flux levels within the 50-1000 ions/(cm^2 · s) range. Results in Fig. 3(a) show that device cross section remained essentially consistent below 1000 ions/(cm^2 · s) but began increasing at approximately this threshold, implying that when ion strike time intervals decrease to 1 ms, some cells running below target voltage may be affected by subsequent heavy ion irradiation.

In simulations, voltage drops recover at the nanosecond scale—much faster than the 1 ms observed in experiments. This difference is explained by analyzing the chip' s multi-stage power delivery network. Transient current from a single heavy ion has nanosecond-scale pulse width, and such high-speed surges are primarily compensated locally by bypass capacitors within the chip and packaging. Our TCAD-Cadence co-simulation in Fig. 8 accurately captures this rapid recovery process, which gradually recovers on a nanosecond timescale. However, bypass capacitors have limited charge capacity and require replenishment from the slower Voltage Regulation Module (VRM). The VRM' s response time typically ranges from hundreds of microseconds to milliseconds [43-45]. Under low flux conditions, the VRM has sufficient time to fully recharge bypass capacitors between consecutive heavy ion strikes, keeping events independent. Under high flux conditions, ion strike frequency exceeds the VRM' s recharge capability, resulting in net cumulative charge deficit in bypass capacitors that manifests as core voltage drop, significantly reducing device noise margin. Consequently, later ion strikes generate transient voltage drops on this already degraded voltage baseline, increasing SEU cross section.

In addition to temporal characteristics, spatial characteristics of IR drop play an equally critical role. Fig. 9 presents simulation results of spatial voltage drop distribution, revealing significant spatial spreading. Voltage degradation is not confined to cells near the ion strike location but spreads to surrounding cells within the PDN. This non-local nature means a single ion strike' s influence extends to multiple memory cells, indicating that cumulative effects occur when the spheres of influence of consecutive ion strikes overlap in both space and time. At high flux, this spatiotemporal superposition of multiple IR drop events leads to more severe degradation of average core voltage across the chip, inducing the observed increase in SEU cross section.

This mechanism clearly illustrates how nanosecond-scale transient IR drop processes, constrained by millisecond-level power regulation response limits, ultimately manifest as flux dependence in experiments. The effect threshold of 1 ms observed in our experiments aligns with typical VRM response times, providing strong support for this cumulative effect model. Therefore, IR drop effect is the direct physical cause of flux effect, while competition between ion strike time intervals and VRM response time is the key factor determining effect strength.

VI. Conclusion

This study demonstrates that SEU cross section increases with shorter ion strike time intervals in nanoscale FPGAs, with this phenomenon persisting even at flux levels of 1000 ions/($\mathrm{cm}^2 \cdot \mathrm{s}$). This indicates that flux effects must be considered during ground-based irradiation experiments on advanced nanoscale devices. The flux effect becomes more pronounced under conditions of higher LET and lower core voltage. High current generated at shorter ion strike time intervals causes voltage drops that reduce chip core voltage, leading to increased device SEU cross section.

TCAD simulations were used to obtain current sources, which were then injected into Cadence to simulate SRAM arrays, revealing voltage drops on the PDN sufficient to influence device cross section. A voltage distribution map demonstrates the global impact characteristics of IR drop effects. Analysis of the competition mechanism between ion strike time intervals and chip VRM response time confirms the timescale over which IR drop influences device upset cross section. These results provide a comprehensive explanation for the mechanism of ion strike time interval influence on cross section, which is equally applicable to other advanced nanoscale devices. This study provides an essential reference for accurately predicting on-orbit failure rates.

Future work will include additional simulations for quantitative analysis of the physical mechanism underlying cross section variations induced by ion strike time intervals, as well as irradiation experiments on other advanced nanoscale digital circuits to demonstrate the validity and general applicability of this physical mechanism.

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Note: Figure translations are in progress. See original paper for figures.