A Novel Pixel-Chip-Based Region-of-Interest Readout Circuit Design

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Abstract

This paper presents a novel pixel chip readout scheme: the Region-of-Interest Readout Circuit (ROIRC), which is designed for large area, large array pixel chips and Gas Pixel Detector (GPD). This design employs a sentinel pixel detection strategy, enabling rapid identification and prioritized readout of the pixel regions containing signal events. During the scanning readout of these signal events, ROIRC employs a Block-based readout approach, effectively minimizing the readout of non-signal pixels. The functionality of ROIRC has been successfully implemented on both the ASIC and FPGA platforms. In the tests of the ROIRC, the detector is capable of detecting low-energy X-rays in the range of 2-10 keV and support multiple event readouts, and the pixel chip can read out photoelectron signal events with the count rate up to 15 k ·(cm-2 ·s-1) .

Full Text

Preamble

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This paper presents a novel pixel chip readout scheme: the Region-of-Interest Readout Circuit (ROIRC), designed for large-area, large-array pixel chips and Gas Pixel Detectors (GPD). This design employs a sentinel pixel detection strategy, enabling rapid identification and prioritized readout of pixel regions containing signal events. During the scanning readout of these signal events, ROIRC utilizes a Block-based readout approach, effectively minimizing the readout of non-signal pixels. The functionality of ROIRC has been successfully implemented on both ASIC and FPGA platforms. In tests of the ROIRC, the pixel chip embedded in the GPD is capable of detecting low-energy X-rays in the range of 2–10 keV and supports multiple event readouts, with the pixel chip able to read out photoelectron signal events at count rates up to 15 k cm ^{2}s ^{1}.

Keywords: ROIRC, Topmetal-L, LPD, pixel chip, X-ray

INTRODUCTION

POLAR-2 is the next-generation space station mission for the Chinese POLAR experiment, based on the same Compton scattering measurement principle as POLAR but with an extended energy range and an order-of-magnitude increase in total effective area for polarized events [1]. The Low Energy X-ray Polarization Detector (LPD) is one of three payloads in the POLAR-2 experiment [4]. LPD is specifically designed to observe the polarization of Gamma-Ray Burst (GRB) prompt emission in the 2–10 keV energy range and to measure the polarization degree and direction of GRBs as well as their very early X-ray afterglow [5, 6]. This observation is achieved using an array of X-ray photoelectric polarimeters based on GPD [7–12].

Pixel chips exhibit excellent characteristics in photoelectron track imaging, fast time response, and high spatial resolution. Given their wide application in space exploration, the anode pixel readout chip represents one of the core devices [14–17]. Pixel chips typically consist of two parts: the pixel array and the readout circuit. The readout circuit significantly impacts pixel chip performance, making its design the focus of numerous studies. Typical pixel chip readout designs, such as the ALPIDE chip used in the ALICE ITS experiment at the Large Hadron Collider at CERN, employ a hit-driven fashion that reads out only pixels hit by particles. The in-pixel multiple-event data is read out asynchronously by a priority encoder circuit in each double column. This design is not only fast in response but also power-efficient, as the expected occupancy is low and only hit pixels are read out [18–20]. The Imaging X-ray Polarimetry Explorer (IXPE) and the Enhanced X-ray Timing and Polarimetry (eXTP) mission utilize self-triggering XPOL pixel chips. Within these chips, every 2×2 pixel array forms a trigger mini-cluster. When a mini-cluster is triggered by a signal event, the core logic identifies all such clusters and defines the surrounding Region of Trigger (ROT). It then defines the region of interest (ROI) for event capture and readout

by adding predefined padding on the four borders [21–23]. In XPOL-III, the ROI definition approach has been upgraded, delivering enhanced flexibility that not only reduces the number of pixels within the ROI but also effectively shortens the readout time for signal events [24].

The electronics system for the cosmic X-ray polarization detector (CXPD), which functions as a prototype detector for LPD, employs the Topmetal-II− chip for its anode readout and has successfully demonstrated on-orbit capture of photoelectron signals [25, 26]. In CXPD, the gas microchannel plate (GMCP) and Topmetal chip constitute the complete detection system. The GMCP is responsible for electron multiplication, offering high-precision time and energy resolution, while the Topmetal chip implements signal event acquisition, position resolution, and photoelectron track imaging. The successful operation of CXPD has determined that the Topmetal series of chips will be used as the anode readout for GPD in LPD. The readout modules of these chips employ the rolling shutter scheme, which sequentially reads out every pixel regardless of whether it has been hit by a signal event. Consequently, the frame refresh time increases with chip array size. For large-array Topmetal-M1 and M2 chips, the array is divided into 16 channels for parallel readout to enhance the readout rate, with each readout channel requiring high-power analog buffers to drive signals, thereby leading to significant increases in overall chip power consumption [27–32]. Compared to CXPD, the pixel chips in LPD require key characteristics such as high effective area, high count rate, and low power consumption. Therefore, large-array pixel chips using Rolling Shutter readout mode struggle to meet LPD application requirements [2, 3, 13]. Consequently, a novel readout scheme must be developed based on previous generations of Topmetal chips.

This paper presents a novel readout scheme, the Region-of-Interest Readout Circuit (ROIRC), which comprises the scanning module and the co-processing module. The scanning module serves as the readout circuit for the pixel chip Topmetal-L, integrated into the LPD design. The co-processing module is implemented in the front-end FPGA. ROIRC is designed to rapidly identify pixels hit by signal events and designate them as high-priority readout areas, thereby reducing event readout waiting time. The ROIRC method for determining priority readout areas is implemented through the FPGA in the electronics, without requiring comparators to perform threshold comparisons, thereby simplifying the analog circuit architecture of the pixel unit. Furthermore, it enables the entire readout logic to function with only a single readout channel. This approach meets LPD requirements for low-power design in pixel chips. The proposed ROIRC scheme has been implemented and successfully validated through tests.

II. TOPMETAL-L READOUT MODULE DESIGN

Topmetal-L is a large-area CMOS pixel sensor chip designed for LPD. It is based on the Topmetal-II− and Topmetal-M chips and fabricated using the GSMC 130 nm CMOS process. As shown in [FIGURE:1] and

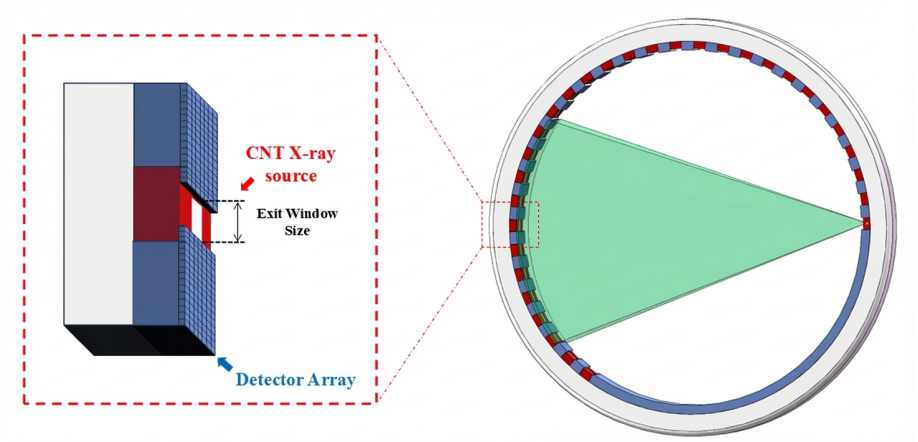

Figure 1: Figure 2

, the total size of the Topmetal-L chip is 17 mm × 24 mm, including a pixel matrix of 356 (rows) × 512 (columns) with periphery circuits. The readout circuits are placed at the left and bottom of the pixel matrix. All IO pads are located at the left, right, and bottom of the chip to facilitate assembly in multi-chip applications. Each pixel sensor is 45 × 45 m^2, and the exposed non-insulated area is 26 × 26 m^2. Each Topmetal is surrounded by a guard ring of the same metal layer, covered by an insulating layer. The coupling capacitance between the guard ring and the top metal can be used for pixel performance calibration. The guard ring of each pixel can be biased with an external voltage signal to emulate electrons generated by particle hits.

As shown in

, each pixel unit consists of a Topmetal sensor, a charge-sensitive amplifier (CSA), a two-stage source follower circuit, and row readout selection switches. The Topmetal working principle is based on a patch of the topmost metal layer acting as a charge collection electrode placed in each pixel cell, with the Topmetal sensor connected directly to the CSA. The Topmetal sensor of the pixel unit is responsible for collecting charge signals and converting them into voltage signals through the CSA for amplification.

The CSA consists of a folded cascode operational amplifier, a feedback capacitor (Cf), and a discharge transistor (Mf). The folded cascode architecture provides high gain and superior linearity, as shown in

. The feedback capacitor Cf (1 fF) is formed by parasitic capacitance between two metal layers. The charge-to-voltage conversion gain of the CSA is $\Delta Vout/Qin = -1/Cf$, where Qin is the input charge and ΔVout is the output voltage. The decay time constant of the CSA output signal is given by $= Rf \cdot Cf$, where Rf represents the equivalent resistance of Mf. By adjusting the gate

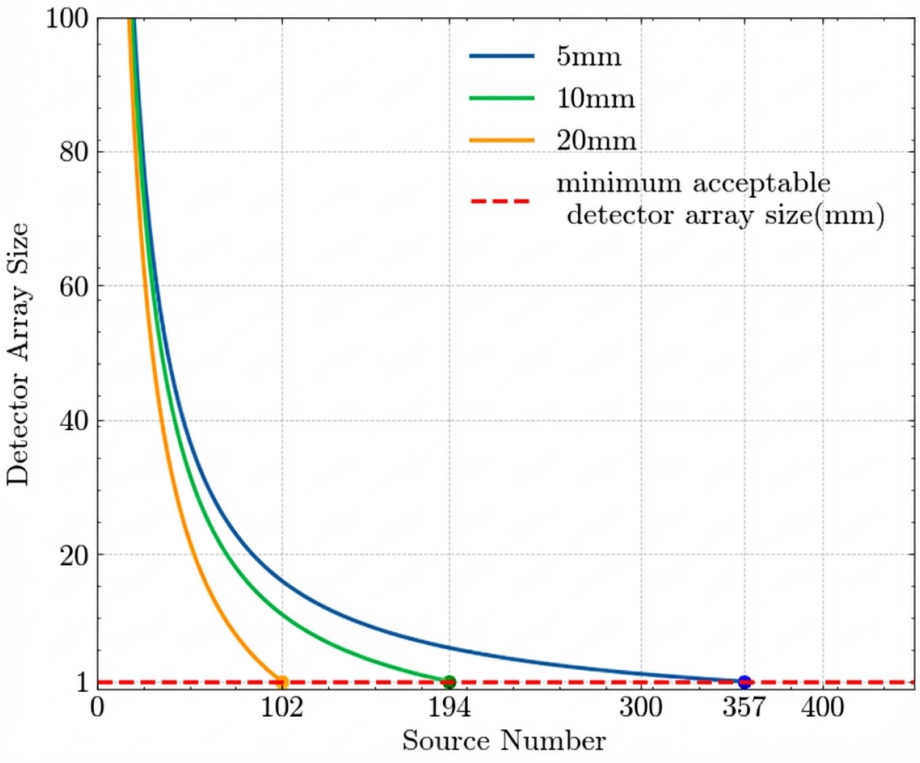

Figure 2: Figure 3

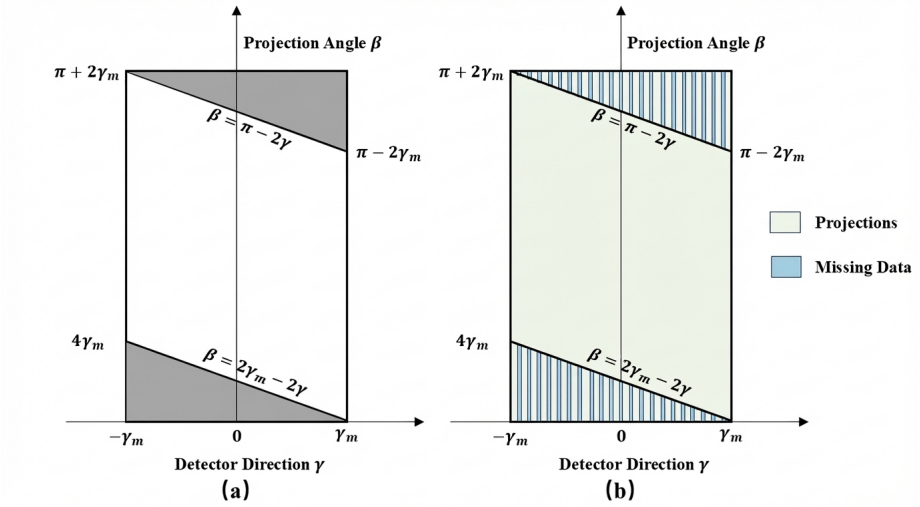

Figure 3: Figure 4

voltage of Mf, the value of Rf can be modified, thereby controlling the output signal decay time. Thus, the Topmetal-L chip employs a decay-based mechanism for pixel circuit reset. This design ensures that charge collection within each pixel remains continuous and independent of row and column selection switch operation. However, this architecture requires that the row and column selection switches can rapidly and precisely locate the pixel region hit by signal events.

As shown in [FIGURE:5], the single-pixel response to a particle signal is depicted. Upon charge deposition, the sensor output exhibits a rapid step increase followed by exponential decay. The X-axis shows relative decay time, while the Y-axis indicates output signal amplitude. Time 1 5 represent signal readouts at different instances. The CSA output is processed through the two-stage source follower, with the signal read out via row and column switches. In each column, all row-selection-switch outputs are connected to the column-selection-switch. Analog outputs from the pixel signal are transmitted out by the analog buffer.

The relevant parameters of the Topmetal-L chip are summarized in . As detailed in [2], these parameters were both theoretically derived and systematically verified through measurement. The following discussion will focus on the chip' s readout circuit design.

The readout circuit of the Topmetal-L chip serves as the critical component of ROIRC—the scanning module—and is implemented using a standardized digital ASIC process. This L-shaped scanning module, embedded in the lower left corner of the pixel chip, manages data readout. Compared to Rolling Shutter readout circuits, this design' s advantage lies in its ability to adjust its working method through multiple parameter configuration sets, thereby offering flexibility and diversity in scanning schemes. The scanning module employs serial input of multi-bit data for each parameter configuration. The scanning logic and parameter configuration logic operate on independent clocks, allowing customized design of different logic blocks to meet specific timing requirements. The row readout selection switch of the pixel unit, the chip-level column readout selection switch, and the control of the column start switch are all connected to the scanning module. It achieves timing convergence under a 50 MHz clock constraint for both scanning logic and data configuration logic. However, the scanning logic clock frequency is also limited by the analog circuit—that is, whether the analog signals of pixels before switching can be read out within the constrained scanning logic clock period. This limitation arises from routing constraints in large-array pixel chips and will be investigated in subsequent chip iterations. In ROIRC testing, a 10 MHz scanning clock was utilized for pixel chip testing.

The function of each parameter is shown in . The pixel switching time Tscan is 100 ns, the data configuration time Tshif t is 20 ns per bit. Each parameter configuration consists of 10-bit serial data and two enable load bits. The time required to complete one data configuration Tdata is 220 ns. Input signals for the scanning module are supplied by the co-processing module, whose circuit functions are implemented in an FPGA. This FPGA-based design provides ROIRC

with greater flexibility and adaptability, enhancing compatibility with various low-energy X-ray detector electronic systems. The co-processing module design can also be ported to a digital ASIC implementation. The operational principles of the scanning module and co-processing module, their working relationship, and the implementation scheme are illustrated in [FIGURE:6].

As summarized in , compared to similar pixel arrays in Topmetal-M chips, Topmetal-L requires only a single readout channel to implement ROIRC readout logic, reducing the number of analog buffers to one-fifteenth that of Topmetal-M. Simulation results show that the operating current of the analog buffer in a single readout channel is 10 mA, which effectively reduces chip power consumption. Furthermore, this design enables each chip to utilize only one analog-to-digital converter, facilitating low-power integration of the detector system [2, 29]. This section primarily focuses on circuit design from the ASIC perspective. The following section presents a comprehensive overview of ROIRC design, integrating the FPGA within the electronics system.

III. REGION OF INTEREST READOUT

ROIRC consists of two core components: the scanning module integrated into the Topmetal-L chip and the co-processing module implemented in the FPGA. The scanning module receives parameters from the co-processing module, updates scanning configurations, and reads out scanned pixels. The co-processing module determines the scanning strategy and sends control parameters to the scanning module. The scanning area is determined by setting pixel start addresses, pixel end addresses, and the number of row and column steps in the pixel array.

The ROIRC workflow consists of three sequential phases: (1) In the initial phase, the co-processing module instructs the scanning module to perform readout at uniform row and column intervals. This process is defined as "sentinel monitoring scanning," where the pixels scanned are defined as "sentinel pixels." Those sentinel pixels hit by signal events are defined as "trigger pixels." (2) The scanning module calculates the target area to be scanned based on the positions of these trigger pixels. (3) To ensure complete readout of signal events, ROIRC expands the perimeter of the area that needs to be read out; this process is defined as "region inflation." This paper elaborates on three core components of the ROIRC algorithm. As illustrated in

, the schematic diagram shows the random selection of rows 123–138 and columns 53–74 from the chip matrix. The scanning module divides parameters received from the co-processing module into six distinct groups that collectively define the scanning module' s operating mode.

demonstrates how ROIRC captures and records complete particle trajectories.

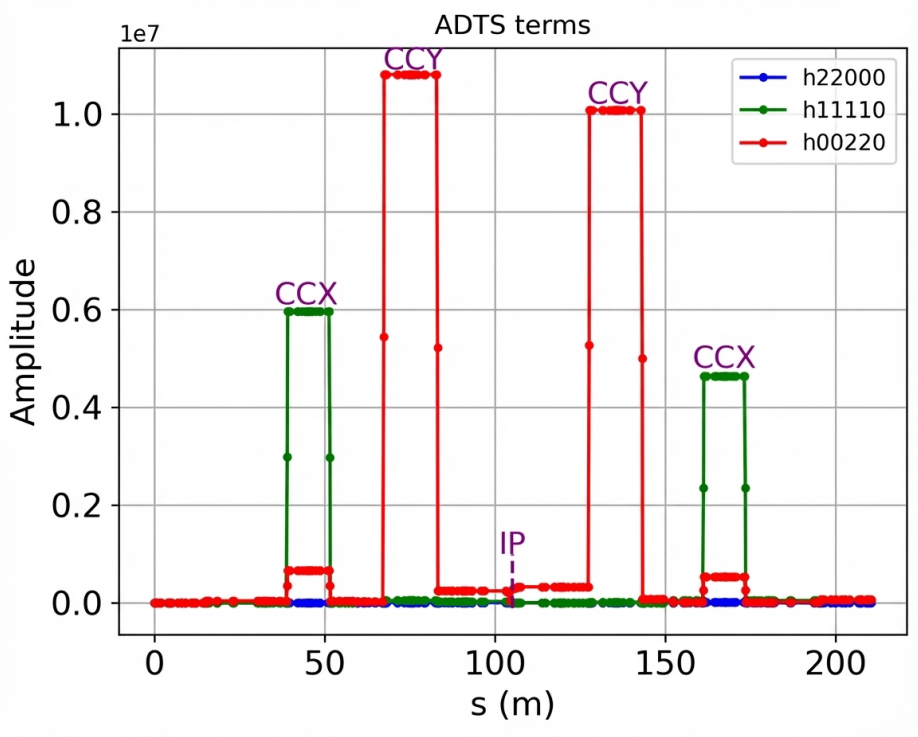

Figure 4: Figure 7

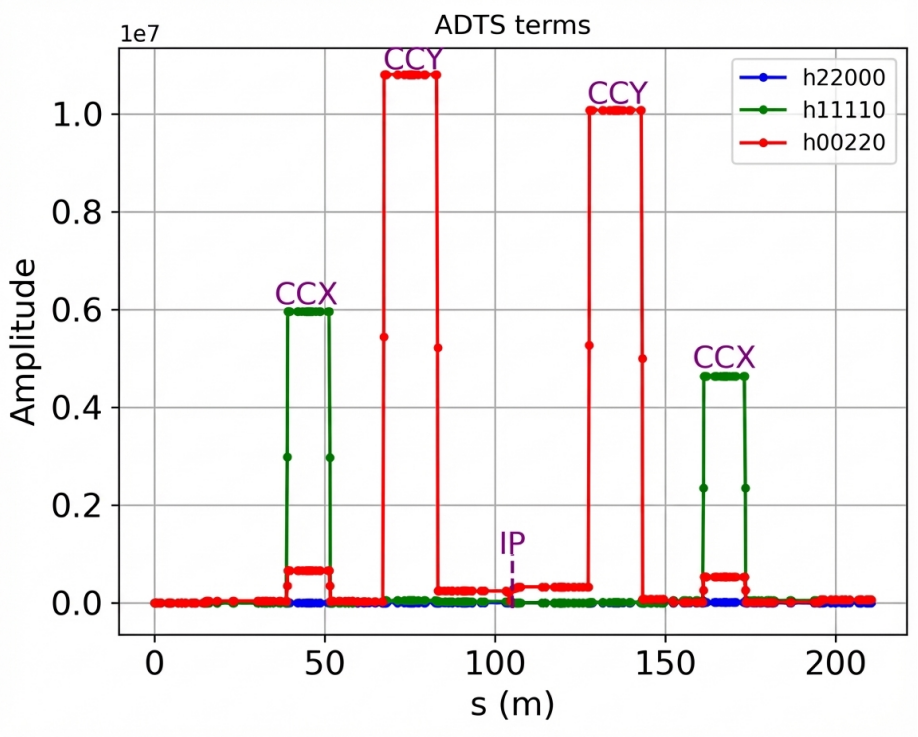

Figure 5: Figure 7

A. Sentinel Monitoring Scanning and Threshold Comparison

The sentinel monitoring scanning process is illustrated in [FIGURE:8]. Its purpose is to rapidly determine particle event arrival by increasing frame rate. Sentinel pixels are uniformly distributed across rows and columns of the pixel array, with their distribution defined by row and column step parameters. Only these pixels are read out during this phase. The co-processing module stores data from each sentinel scan frame. If no signal event is detected, the scanning module repetitively executes this process.

To identify signal events, the co-processing module compares the current frame' s sentinel pixel data with that of the previous frame. If the difference exceeds the set threshold, it determines that an effective signal event has occurred around that sentinel pixel, and the pixel is identified as a trigger pixel. The co-processing module records address information for all trigger pixels in the current frame. The time Tsen required for sentinel monitoring scanning per frame can be calculated using Equation (1), where Npixel is the total number of pixels in the array, Nr−step is the number of row steps, and Nc−step is the number of column steps during scanning. Tscan and Tdata are known (see Section II for details).

$$T_{sen} = \frac{N_{pixel}}{N_{r-step} \times N_{c-step}} \times T_{scan} + T_{data} \tag{1}$$

B. Region Scanning

The region scanning scheme executes upon detection of a trigger sentinel pixel. This scheme employs a Block-based scanning method, where each triggered sentinel corresponds to a predefined Block region, with the Block' s position determined by the trigger sentinel location. For all trigger sentinels within a cluster event, ROIRC defines Block regions based on their relative positions: adjacent sentinels are assigned Blocks with boundaries strictly defined by preset row and column intervals, while sentinels identified on the event periphery can have their Block dimensions dynamically adjusted by the co-processing module. This strategy integrates adjacent Blocks into a continuous readout region, thereby avoiding redundant pixel scanning while ensuring complete event coverage.

During region scanning, ROIRC reads out pixel information from each Block sequentially in row-column order. As shown in [FIGURE:9], due to the large size of the chip' s pixel array, multiple signal events may hit and be detected within the duration of a single sentinel scan frame. When multiple signal events are detected within the same sentinel scanning frame and are determined to be spatially distant from one another (such as Block1 and Block2), the system assigns each event its own dedicated Block scanning region. They are not combined into a single rectangular area. As shown in

and

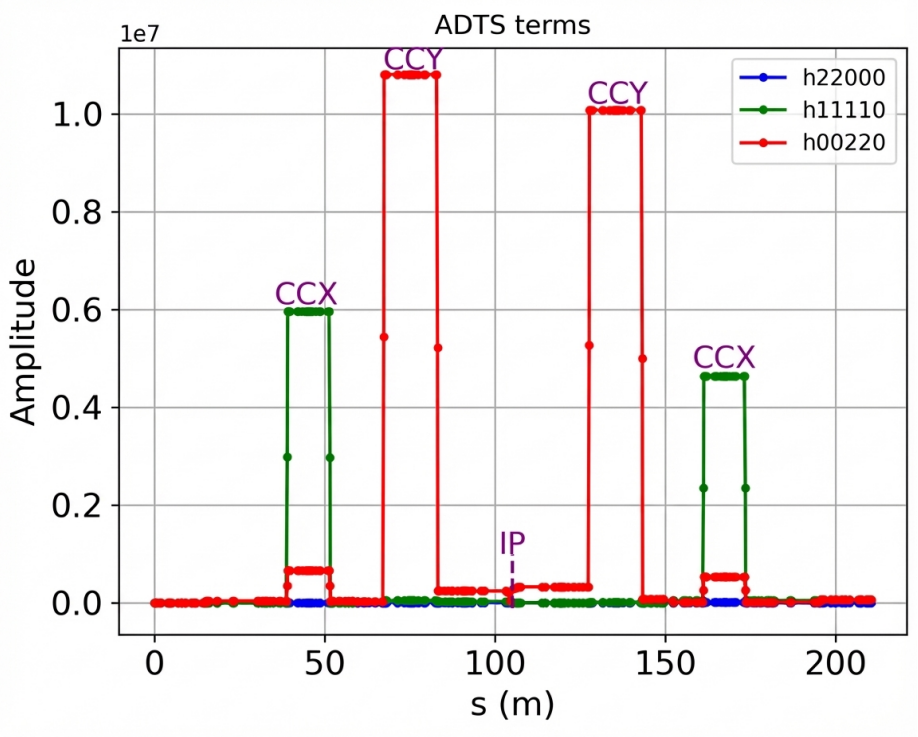

Figure 6: Figure 7

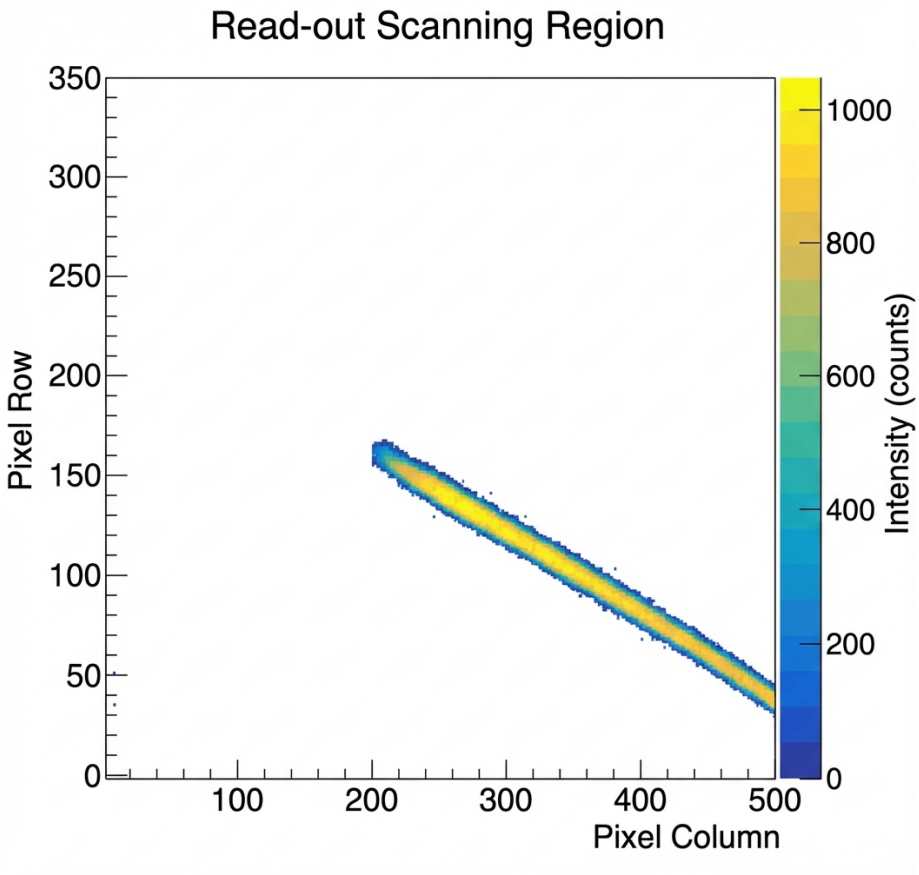

Figure 7: Figure 21

(d), compared to the method of calculating the minimum bounding rectangle (i.e., determining coordinates of Xmax, Xmin, Ymax, Ymin for the area), the Block-based approach reduces both the number of pixels to be read out and the associated readout time, particularly for irregular or elongated tracks, as well as for tracks triggered distantly within the same frame.

The spacing between sentinel pixels can be flexibly configured according to application requirements to achieve an optimal balance between frame rate and signal event capture probability. Once region scanning is completed, ROIRC returns to sentinel monitoring scan mode to await subsequent signal events. Since the scanning module requires parameter reconfiguration before each Block scan, the single-Block scanning time Tblock is calculated using Equation (2), where Nblock is the number of pixels in a single Block.

$$T_{block} = T_{shift} + T_{scan} \times N_{block} \tag{2}$$

C. Dilation Process

As shown in

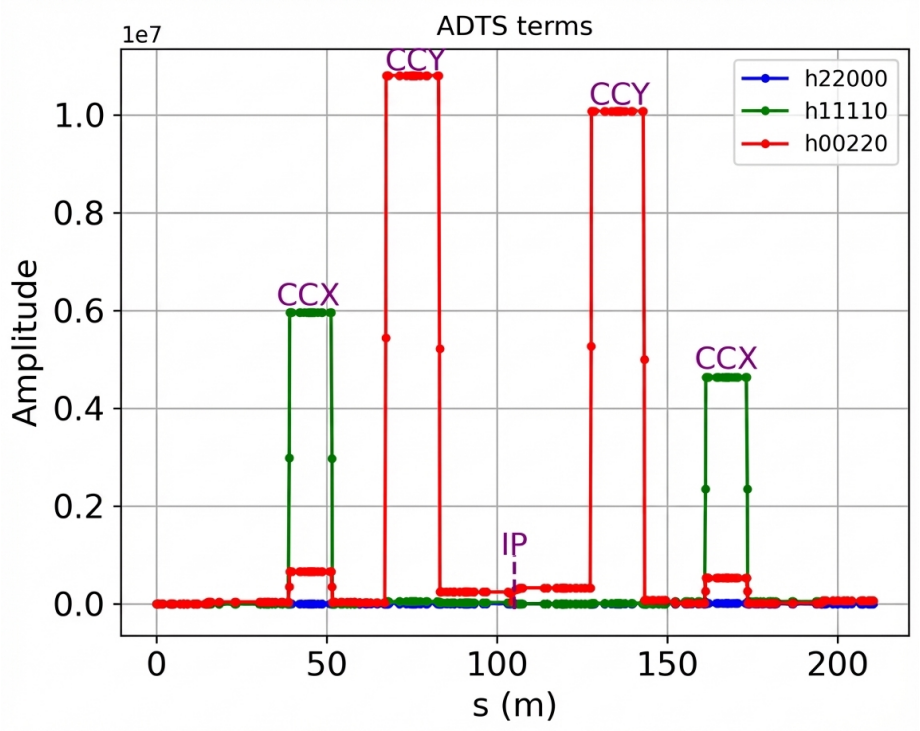

Figure 8: Figure 7

, particle signal events typically deposit energy in irregular, spatially stochastic patterns across the pixel array. When edge signals exhibit insufficient amplitude, the difference between sentinel frames before and after the event may not change significantly, preventing the sentinel from being triggered as a trigger pixel. Consequently, reading out only Blocks containing trigger pixels may result in incomplete signal event readout.

To resolve incomplete signal readout, the dilation process has been introduced into the region scanning procedure. The core concept is to read out not only the Block where the triggered pixel is located but also surrounding Blocks containing sentinel pixels adjacent to those triggered pixels. The size of these Blocks can be controlled by the collaborative processing module. [FIGURE:10] illustrates the dilation algorithm implementation process. Tregion denotes the readout time for a single signal event, Ndp is the number of dilated Blocks, and Tdilation is the time required to read out a single dilated Block.

$$T_{region} = N_{trigger} \times T_{block} + N_{dp} \times T_{dilation} \tag{3}$$

IV. TEST RESULTS

This section presents test results for the Topmetal-L chip integrated into the GPD and operated under ROIRC readout logic. The readout architecture of the pixel chip in the LPD detector must be capable of reading out complete photoelectron track images, handling high count rates, and rapidly accessing pixel regions hit by signal events. Consequently, test evaluation focuses on the readout mechanism, signal event integrity, and support for multiple event readouts.

It should be emphasized that the Topmetal-L chip and ROIRC readout scheme represent only one component of the overall detection system. Detector performance is influenced by multiple factors, including internal GPD components, gas mixture properties, and the electronic system. Therefore, all tests described hereafter were conducted under operating conditions for both chip and detector as defined in [2, 3, 8]. This ensures that ROIRC logic not only achieves rapid readout but also maintains reliability and validity of data acquired and read out by the detector. Section IV.A details the testing platform setup.

A. Test Setup

The experimental test platform comprises the GPD, an electronic system, and experimental test instruments. As shown in [FIGURE:11], the GPD is divided into three functional regions: the electron drift region, electron multiplication region, and charge collection region. The GMCP serves as the electron multiplier in the electron multiplication region, with a diameter of 25 mm, thickness of 300 m, pore diameter of 50 m, pore pitch of 60 m arranged in a triangular pattern, and bulk resistance of 2 GΩ. The drift gap between the cathode and GMCP is 10 mm, and the induction gap between the GMCP and anode is 3 mm. The

detector was operated with cathode voltage (V-drift) at −3600 V, GMCP top surface (V-top) at −1650 V, and GMCP bottom surface (V-bottom) at −500 V, while the anode was grounded. The working gas within the chamber consists of helium and dimethyl ether (DME) in a 4:6 ratio. The energy resolution reached 18% at 6.4 keV, as defined in [3, 8]. X-rays are emitted by the Fe source or X-ray generator, passing through the beryllium window on the gas chamber to enter the chamber. The mixed gas inside enhances interaction between X-rays and gas molecules in the electron drift region, effectively inducing photoelectric effect and converting X-rays into photoelectrons. Under the electric field influence, these electrons drift toward the GMCP upper surface and enter channels through small orifices. Within these channels, cascade multiplication of initial electrons occurs, generating significant numbers of secondary electrons that eventually exit the GMCP and are collected by the Topmetal.

The test electronics comprise the bonding board, readout board, and FPGA core control board, with interconnections shown in

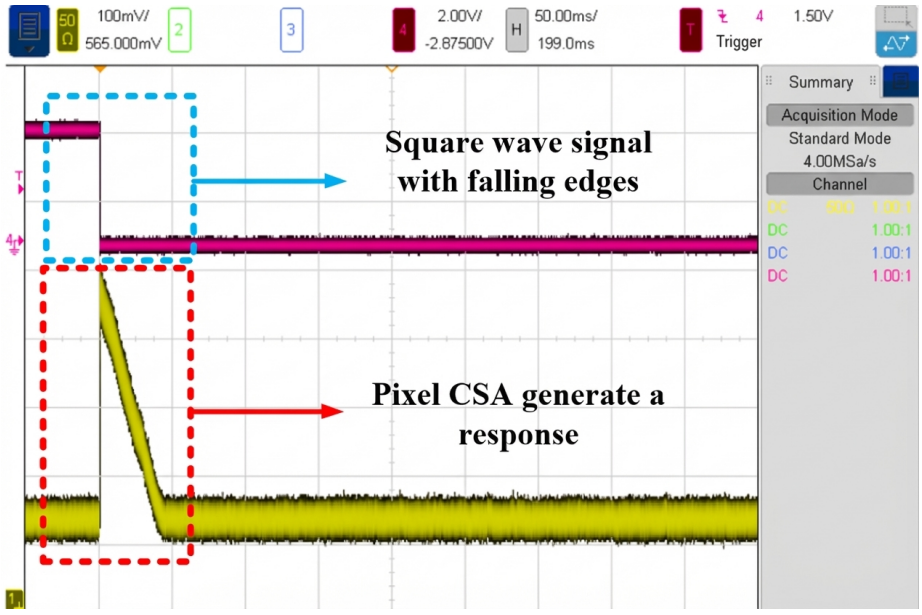

Figure 9: Figure 12

. The readout board serves two primary functions. First, it utilizes an on-board 8-channel DAC (DAC8568) chip to supply adjustable bias voltages to the Topmetal-L chip. By configuring different DAC channels, key performance parameters such as decay time constant can be precisely tuned to ensure stable chip operation. Second, the board transmits pixel readout signals to the ADC (ADS52J90) located on the FPGA core control board. This ADC features an input dynamic range of 2 V, sampling rate of 40 MSPS, and sampling resolution

of 12 bits, resulting in an LSB of approximately 0.49 mV.

The FPGA core control board implements the co-processing module and handles data transmission and processing tasks. Exchange of control commands and data transmission between the electronic system and PC are accomplished via PCIe bus interface. Furthermore, the readout board can be connected to an external oscilloscope for real-time monitoring of pixel output signals. Test operators can inject square-wave signals into the guard ring structure of the Topmetal-L chip to simulate negative charge injection into the top-metal layer.

B. Noise Testing and Pixel Masking

As described in Section III.A, "trigger pixel" detection depends on the trigger threshold set in the co-processing module. However, inherent to CMOS technology, some pixels exhibit higher noise levels than others, as shown in

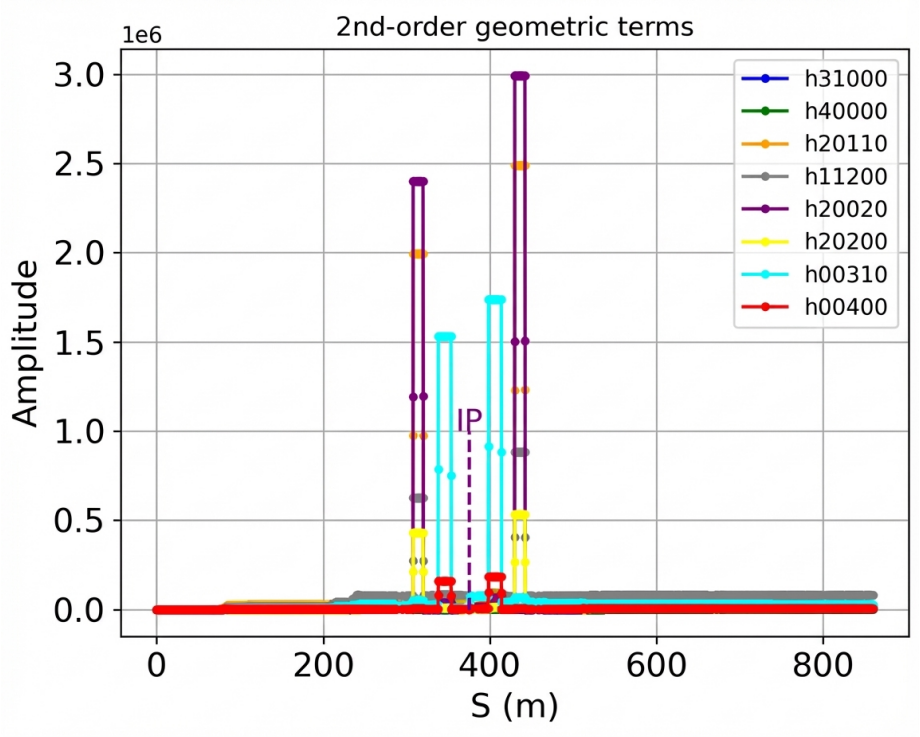

Figure 10: Figure 14

. If these high-noise pixels are selected as sentinel pixels, noise fluctuations can exceed the set threshold, causing erroneous triggering by the co-processing module and initiating unnecessary region scanning.

In this test, we compared output signal baselines of all pixels in the Topmetal-L

chip across consecutive frames and visualized in binary the pixels with differences exceeding the threshold, as shown in FIGURE:15. As threshold increases, the number of white points (pixels with differences exceeding the threshold) decreases. While higher thresholds can suppress false triggers from noisy pixels, setting them too high risks missing valid low-amplitude signal events. To address this issue, this paper proposes implementing a bad-pixel masking algorithm. ROIRC records and masks addresses of these defective pixels. Consequently, even if a masked pixel is designated as a sentinel, it is excluded from trigger logic. In this experiment, conducted with no external signal injected into the chip, pixels exhibiting inter-frame differences greater than 100 mV were masked. FIGURE:15 shows the image after masking, demonstrating that the bad-pixel masking strategy effectively suppresses false triggering.

C. Validation of Readout Scheme Feasibility

ROIRC detects signal events through sentinel pixels. The spacing between these sentinels is a critical parameter directly impacting system trigger efficiency and frame rate. To optimize this, we performed trigger rate experiments based on Monte Carlo simulations in the low-energy spectral region (3 keV, the lowest-energy X-ray attainable from our team' s X-ray generator). As shown in [FIGURE:17], results revealed that with row and column spacing of 5 pixels and the trigger threshold (established in Section IV.B for bad-pixel filtering), the chip achieves collection efficiency exceeding 90% for 3 keV photoelectron signals. Based on this result, the following parameters were adopted: row and column start addresses of 0, end addresses at 355 and 511, step sizes for both rows and columns of 5 pixels; each Block corresponding to a sentinel pixel contained 25 pixels; dilation range set to 7 pixels; minimum scanning region (triggered by single sentinel) of 361 pixels; and trigger threshold set to 200 ADC counts.

In practical testing, ROIRC scheme performance was validated using the Fe radioactive source, which emits monoenergetic 5.9 keV X-rays. This experiment assessed the detector' s capability to record photoelectron tracks under the ROIRC scheme. The test platform is shown in [FIGURE:18].

illustrates ROIRC capturing signal events.

(a)( ) shows the sentinel scanning process, where evenly spaced blue dots represent readout values during sentinel monitoring, with all other pixel values set to ADC value 0, and the red wireframe encloses triggered sentinel pixels.

(a)( ) shows event signals from regional readout, while

(a)( ) provides a magnified view of these event signals.

(b) shows sentinel pixels at the local position of the pixel chip. Each readout sentinel pixel is evenly spaced and uniformly distributed. The scanning region in

(b) corresponds to the position of the triggered sentinel pixel in

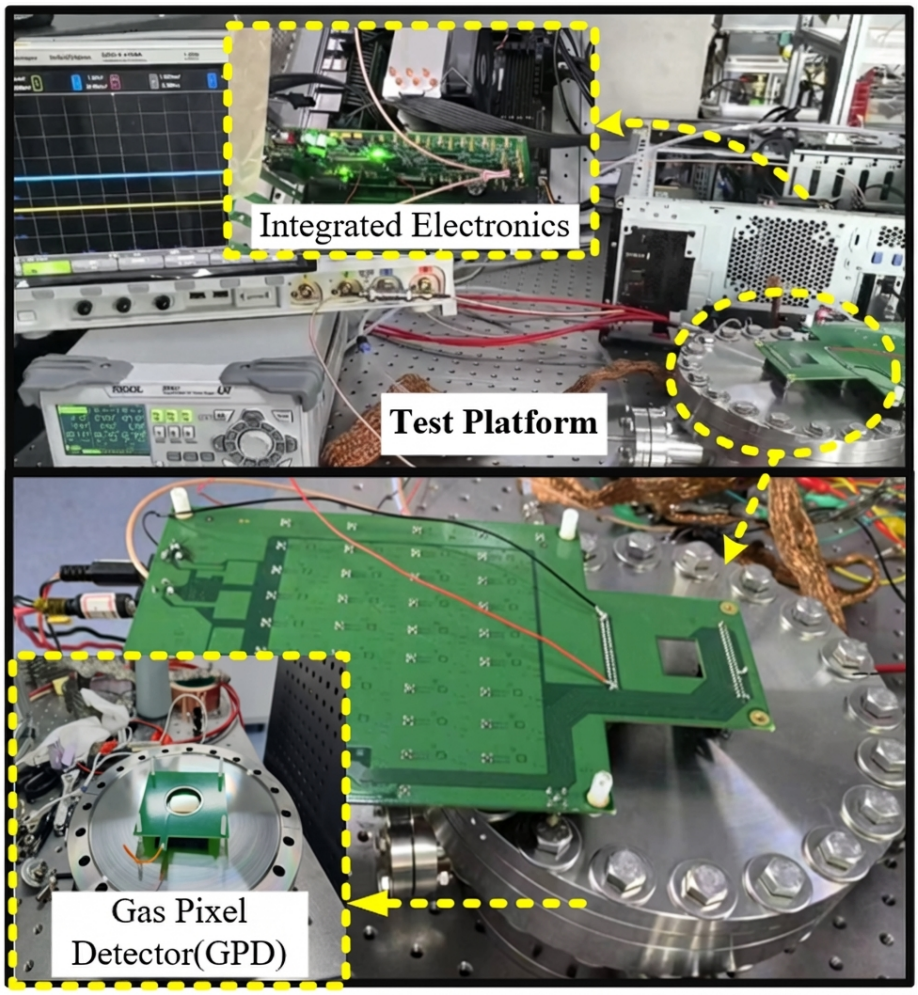

Figure 11: Figure 16

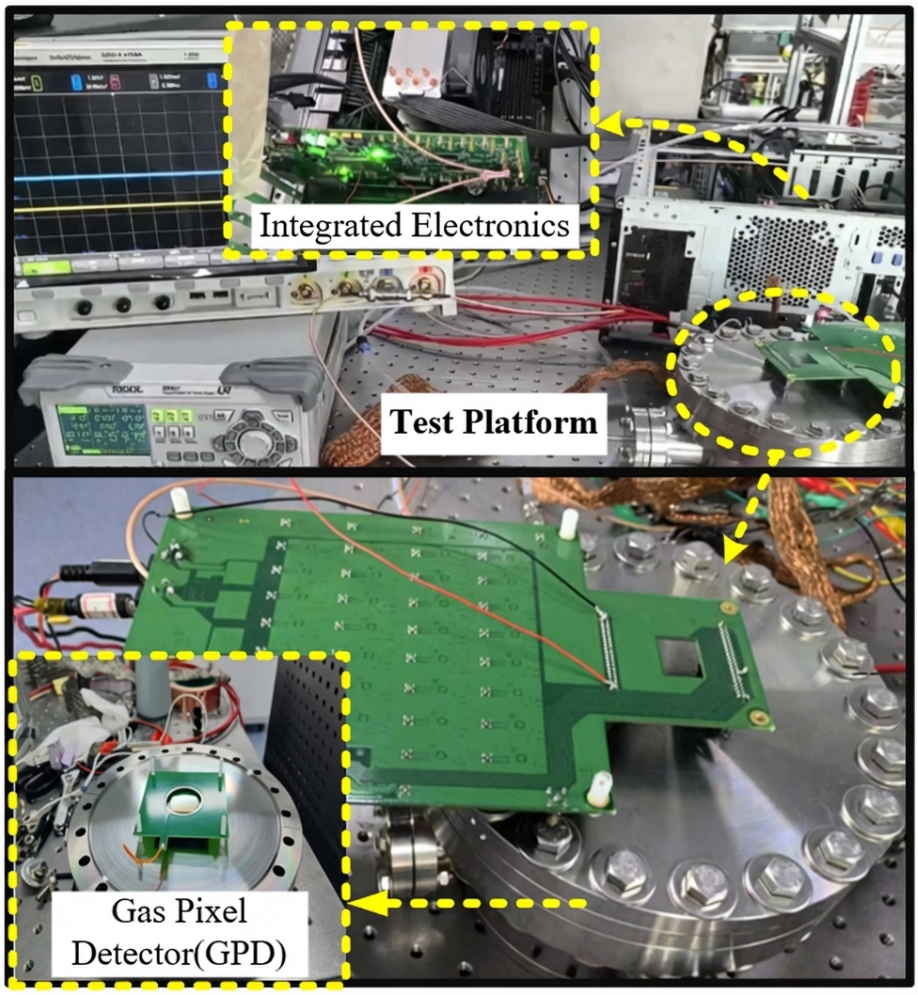

Figure 12: Figure 16

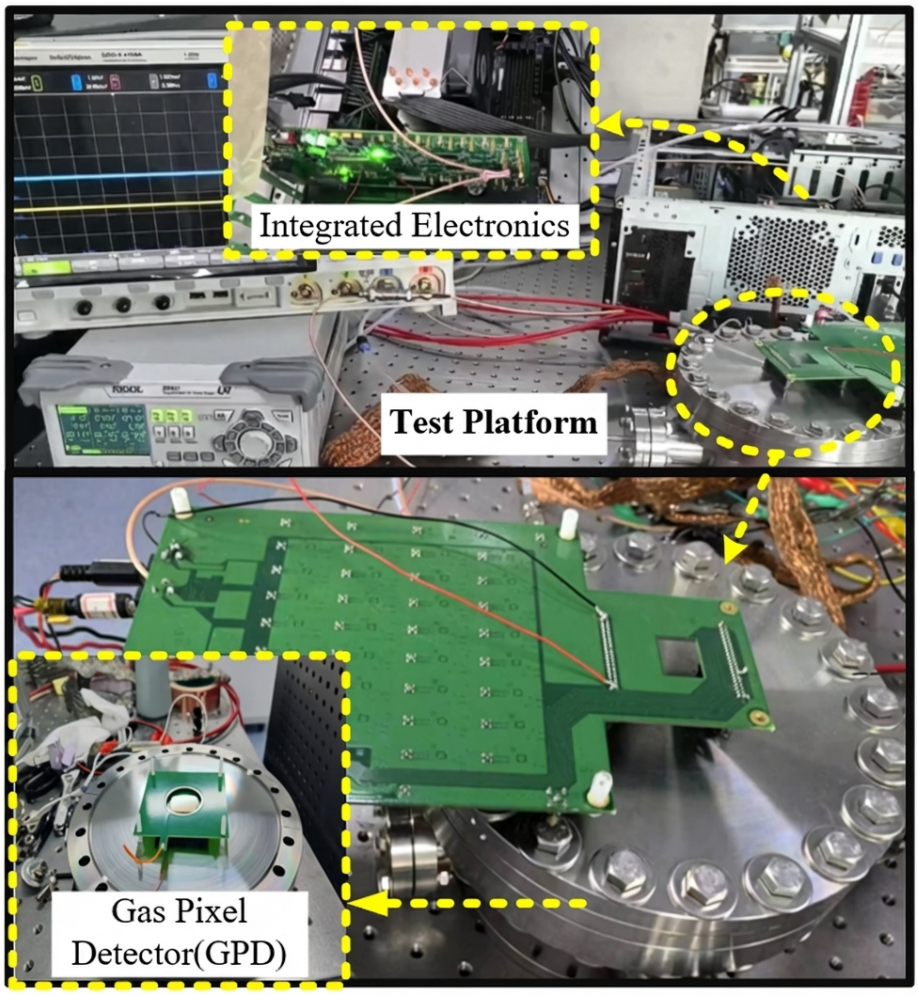

Figure 13: Figure 16

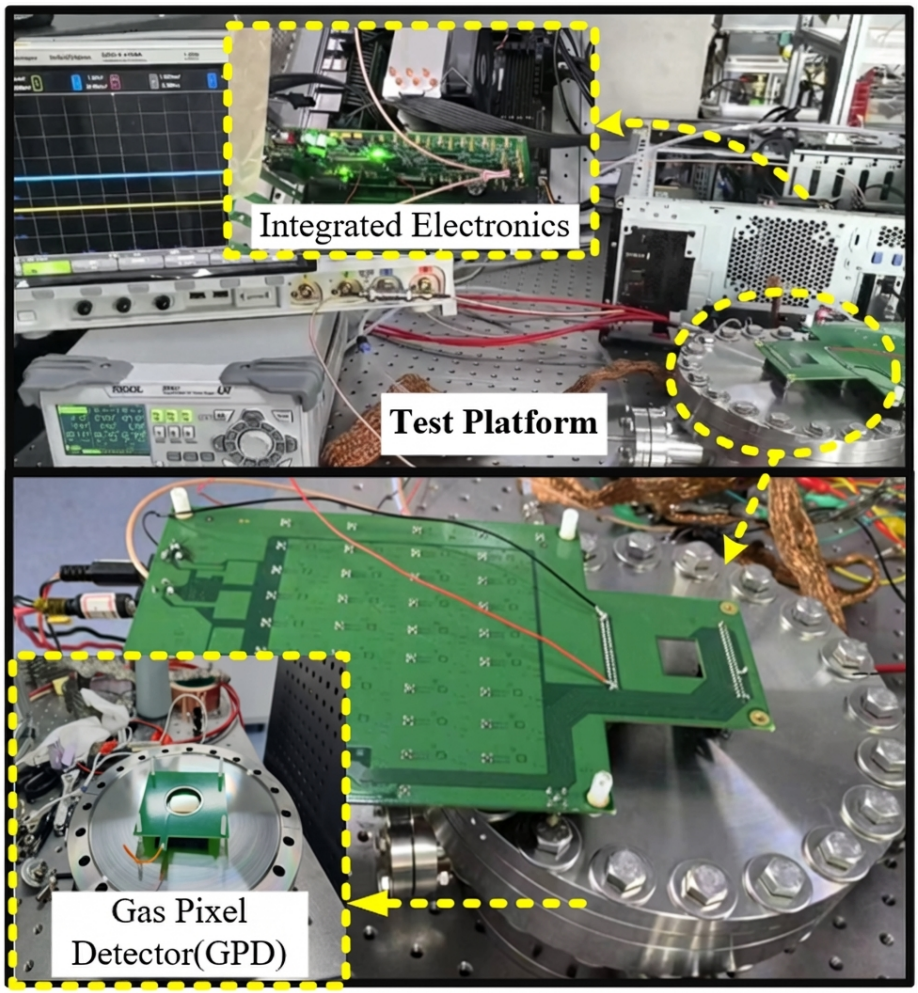

Figure 14: Figure 16

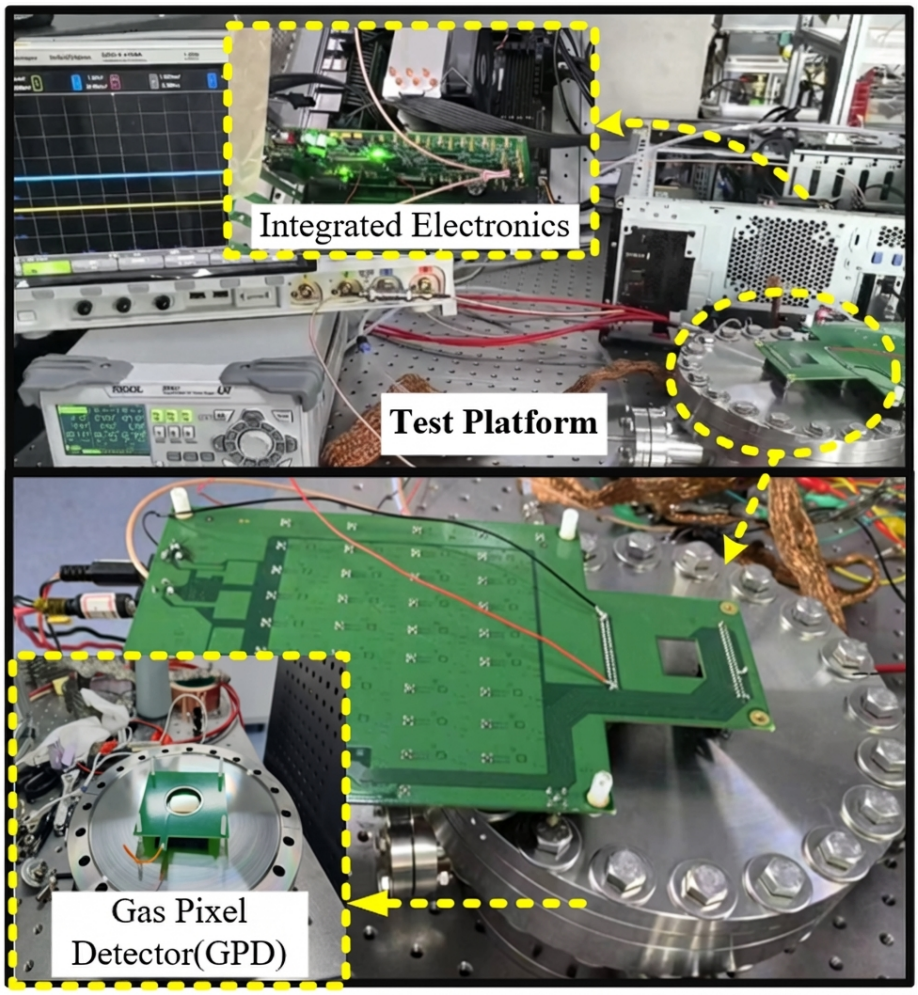

Figure 15: Figure 16

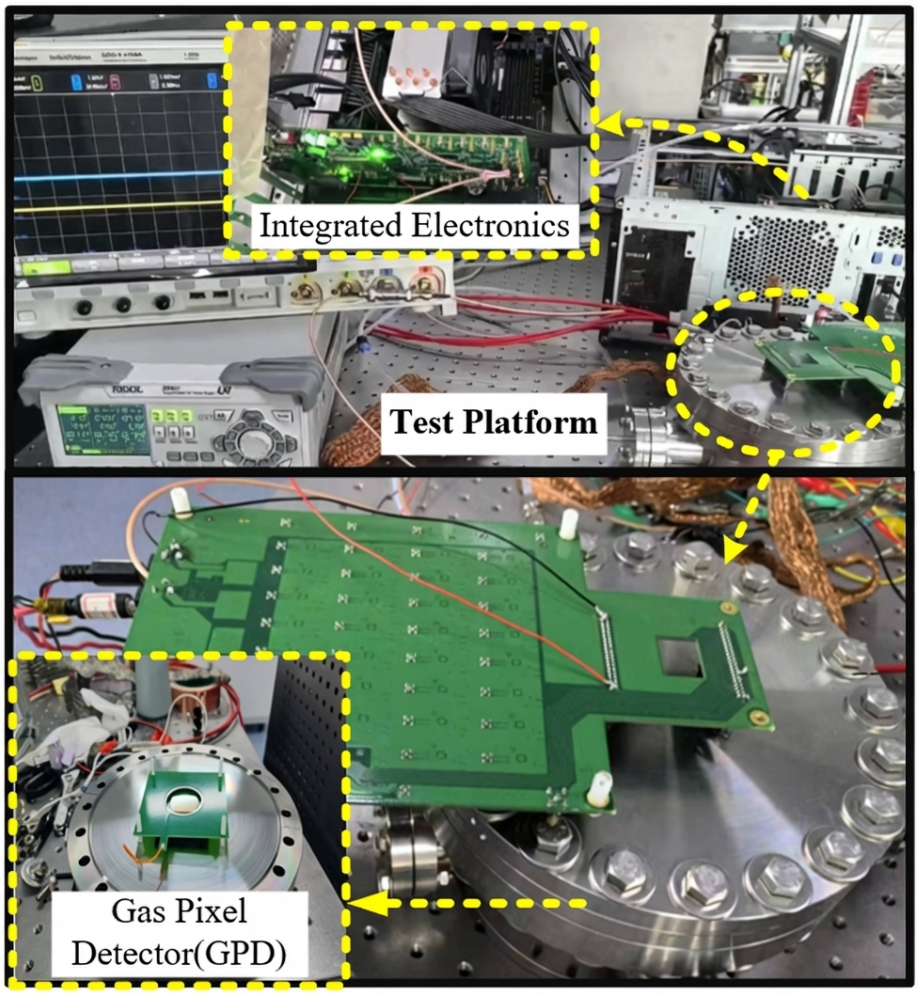

Figure 16: Figure 16

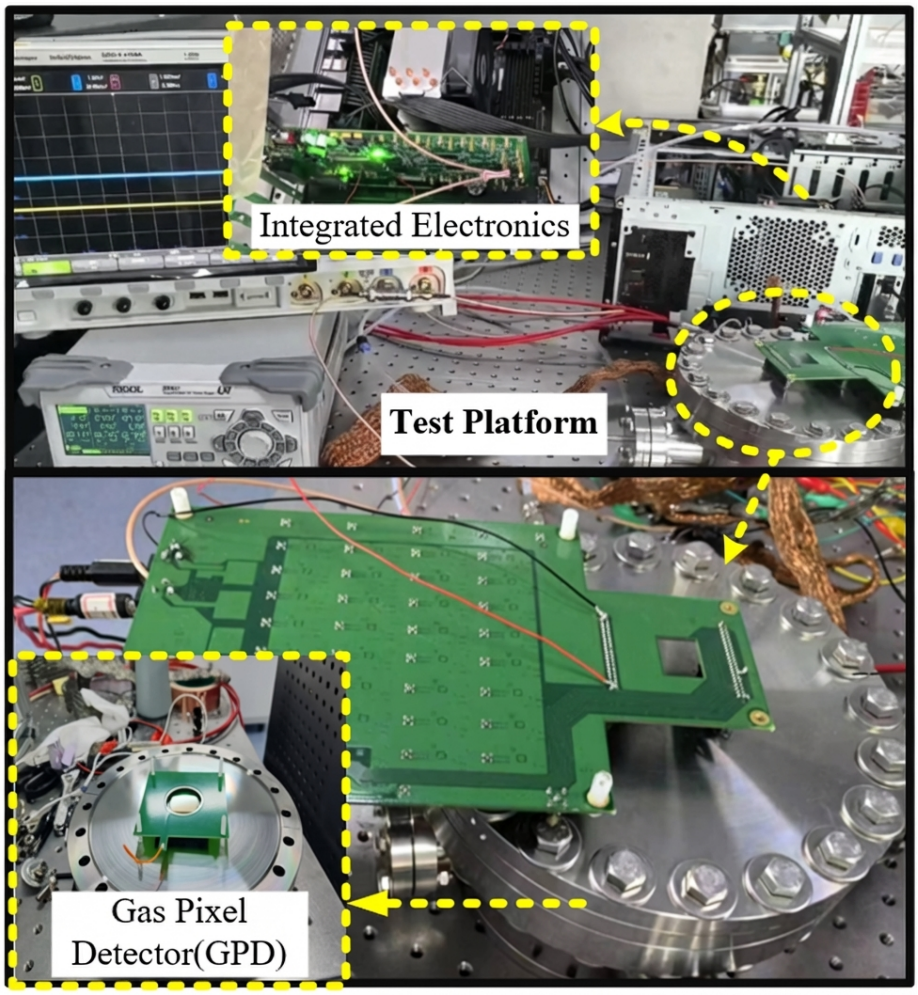

Figure 17: Figure 16

(b) .

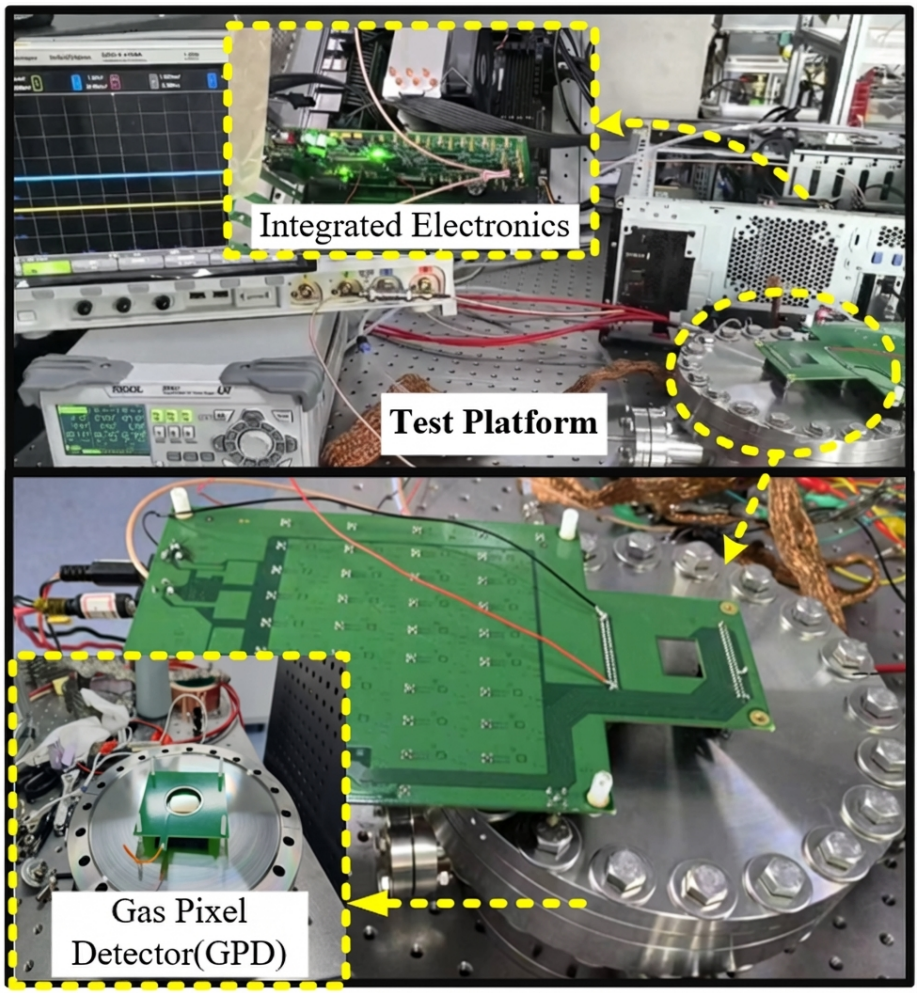

Figure 18: Figure 16

(c) demonstrates that in a single frame of sentinel monitoring scanning, ROIRC can support triggering of multiple sentinels and perform multi-region readout operations based on trigger pixel position sequence. [FIGURE:19] shows the distribution of the number of pixels hit per single photoelectron event from the Fe source in the Topmetal-L sensor.

According to Equation (1), Equation (2), and Equation (3), under a scanning step of 5 pixels in both row and column directions, the maximum dead time required for reading effective event signals is 709.24 s. In contrast, under Rolling

Shutter readout mode, the maximum dead time reaches 18227.2 s. During region scanning, the extent of the pixel region read out is defined by the count of triggered sentinel pixels. Statistical results reveal that most signal events triggered only one sentinel pixel, with a maximum of two. Therefore, the corresponding number of pixels in region scanning ranges from 361 to 456. Based on this, the required readout time for a single Fe event during the region scanning stage ranges from 36.1 s to 45.6 s.

D. Readout Signal Imaging and Track Completeness

The pixel chip is required to image captured photoelectron tracks in LPD. Thus, we must ensure the chip reads out each signal event in its entirety. To verify this, we performed track integrity analysis on collected signal events. In [FIGURE:20], pixels marked in red indicate triggered sentinel pixels. Their address information enables the backend data processor to define the scanning region. In the readout logic, all sentinel pixels are positioned at the center of their respective Block regions.

By locating sentinel pixels, data processing can determine whether the entire trajectory of the signal event is within the scanning region, thereby confirming whether the signal event has been fully read out. We conducted comprehensive analysis of track integrity for both X-ray signals and high-energy alpha particle signals. These alpha particles are produced by natural decay of trace amounts of radon (Rn) in the GPD gas mixture. Their high energy results in more spatially expansive tracks, providing a more stringent test of readout completeness during region scanning. As described above, signal tracks collected in Section IV.C were analyzed, and it was verified that trajectories of all signal events were completely read out.

ROIRC uses Block-based readout to capture signal events of various track shapes and pixel coverage. Even if multiple event signals are triggered in a single sentinel scanning frame, the readout logic ensures all signal events are read out during subsequent regional scanning.

(a) shows particle tracks from Fe signals, and

(b) shows tracks from alpha particle signals.

(c) illustrates simultaneous generation and reading of both signals during the same sentinel scanning period. As indicated in

(d), the black wireframe indicates the pixel area (composed of all sentinel pixels' Blocks) during region scanning.

E. Readout Rate

One primary goal of ROIRC design is to enable the low-energy polarization detector (LPD) equipped with large-array pixel chips to meet astrophysical observation requirements. For instance, the peak photon count rate of GRB

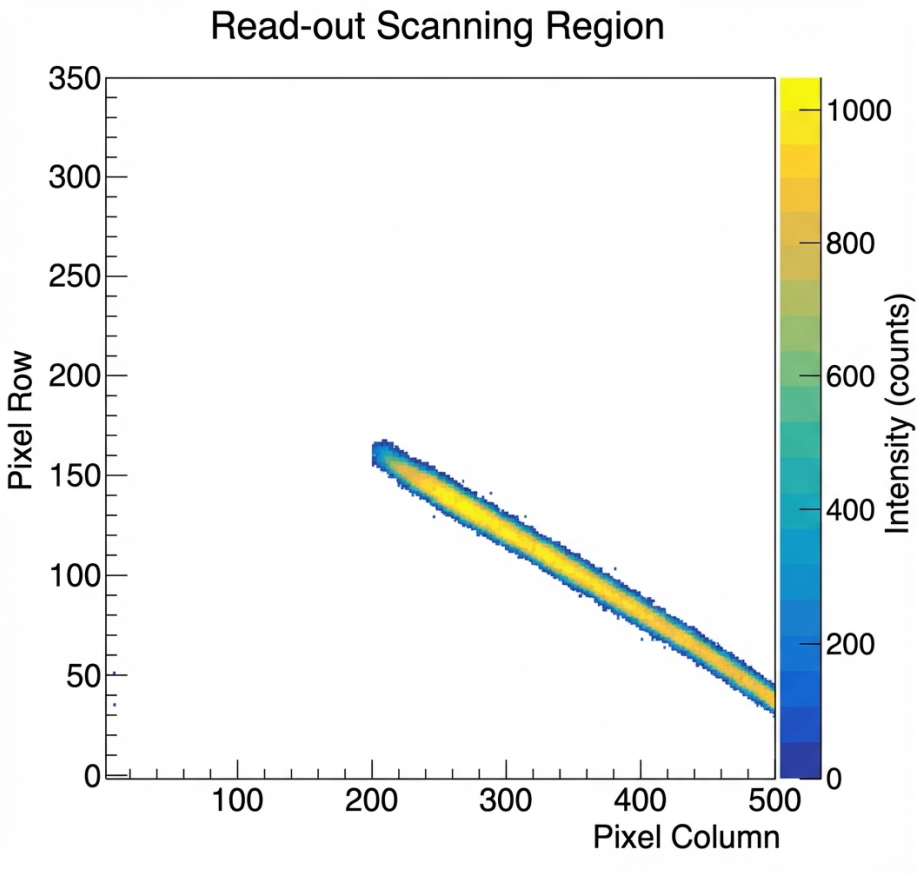

Figure 19: Figure 21

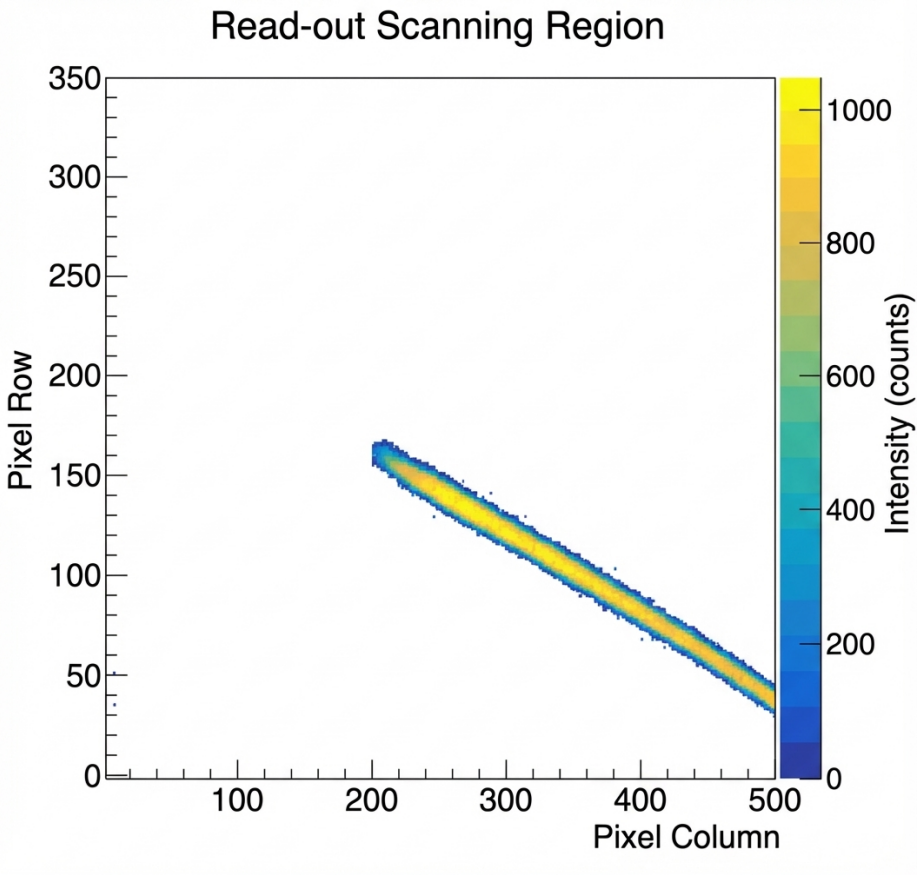

Figure 20: Figure 21

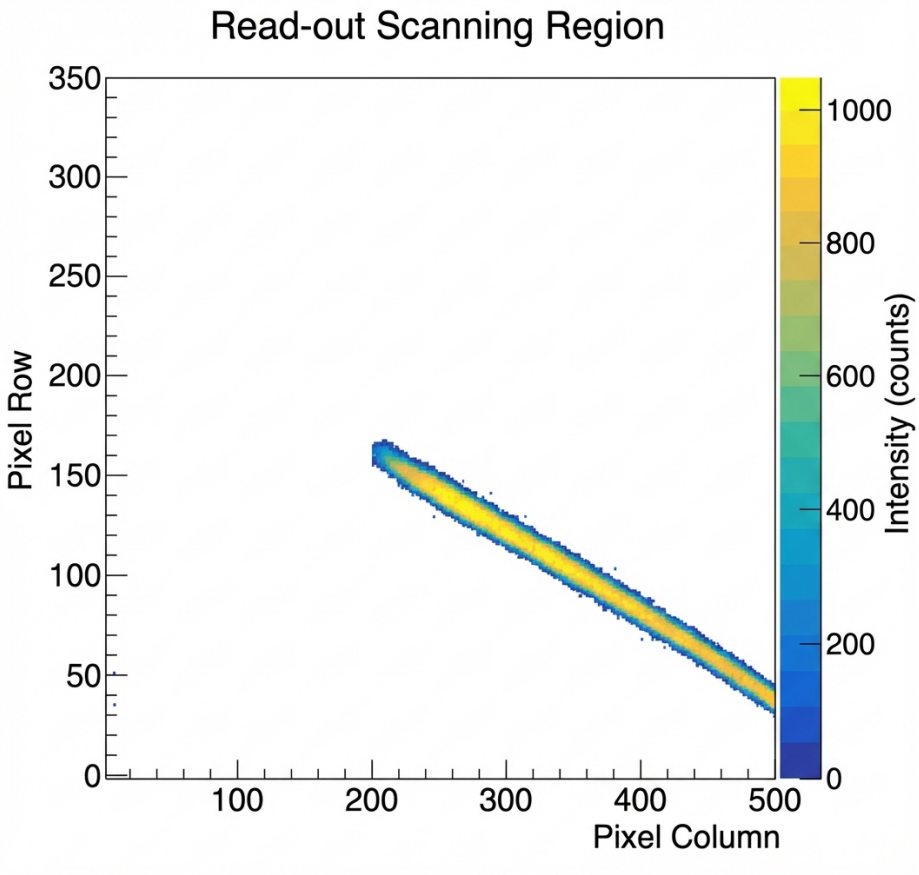

Figure 21: Figure 21

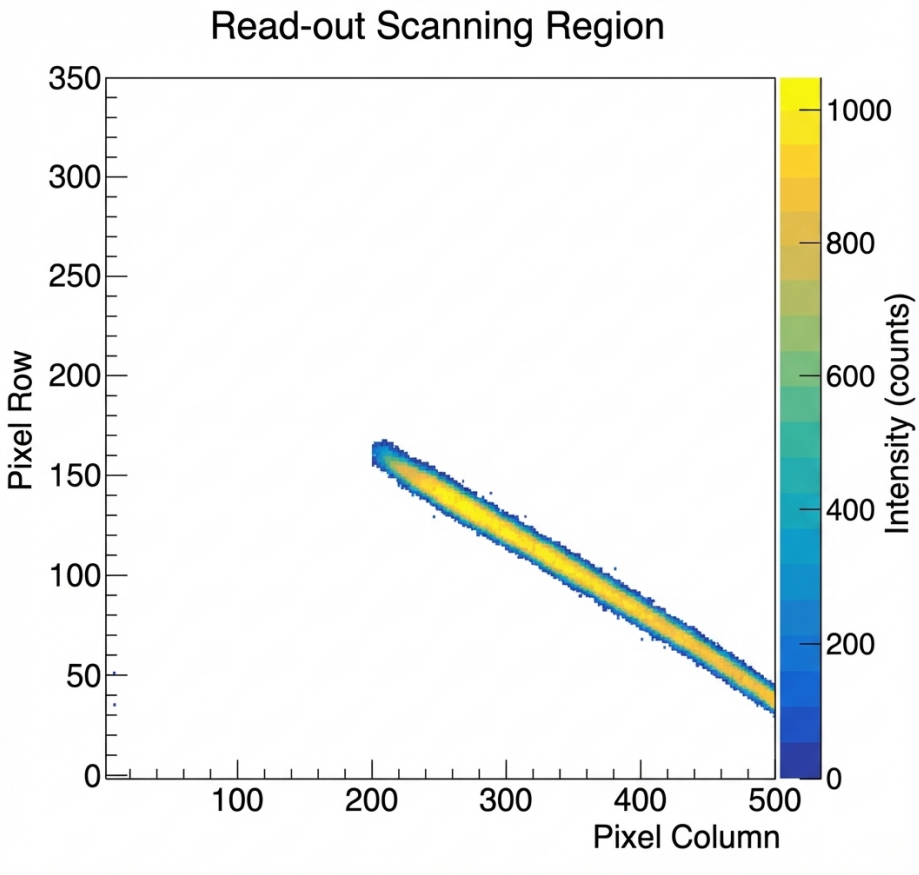

Figure 22: Figure 21

221009A, the brightest GRB observed to date, reached about 4500 ph × cm ^{2}s ^{1} in the 2–10 keV band within a one-second interval. Considering the GPD detection efficiency is approximately 0.1, the signal event rate to be processed by the corresponding front-end electronics system is no less than 450 counts × cm ^{2}s ^{1} [3].

As described in Section II, the signal amplitude acquired by the Topmetal-L pixel chip decays over time; failure to read out the signal within this decay window results in signal loss. Therefore, under the parameter configuration established in Section IV.C, the signal event count rate of the detector in ROIRC readout logic must be evaluated. This rate defines the number of events the chip can process per unit time. In this counting experiment, bias voltage settings for the Topmetal-L chip were consistent with those in [2]. Based on combined simulation and experimental results, the typical discharge rate of the CSA for charge signals under this system configuration is approximately 37.28 mV/ms.

As shown in [FIGURE:22], which depicts the test platform, the chip is placed within the GPD. By adjusting X-ray generator intensity, we can alter the quantity of signal events. [FIGURE:23] shows the distribution of all signal events, where areas with higher brightness indicate a greater number of signal events passing through those regions. All events were successfully read out by the Topmetal-L chip. The measured counting rate of the pixel chip as a function of X-ray tube input current for 5.40 keV X-rays in a 40% He + 60% DME gas mixture at 1 atm is shown in [FIGURE:24]. The Y-axis represents the number of signal events collected and read out by the Topmetal-L chip embedded in the GPD, while the X-axis represents the relative intensity setting of the X-ray generator.

Under ROIRC readout mode, when signal event count rate is less than 15 k cm ^{2}s ^{1}, the chip count rate scales linearly with increasing photon output from the X-ray generator, meaning there is no signal event overlap. However, when signal event count rate exceeds 15 k cm ^{2}s ^{1}, the count rate no longer increases linearly, and some events overlap. These results confirm that the ROIRC-operated detector achieves a maximum usable readout rate of 15 k cm ^{2}s ^{1}, exceeding the 450 counts × cm ^{2}s ^{1} requirement set by the brightest known GRB scenarios.

V. CONCLUSION

This paper has presented the design and testing of a novel readout scheme, the Region-of-Interest Readout Circuit (ROIRC), for the Topmetal-L pixel chip. ROIRC is implemented by digital ASIC (the scanning module) and FPGA (the co-processing module) in the electronics. We have detailed its design structure, logical working principle, and functional behavior. Additionally, we have introduced test results, including X-ray tests based on the radioactive element Fe and the X-ray generator.

The scanning module is integrated into the Topmetal-L chip. It receives parameters from the co-processing module, which it uses to update scanning config-

uration and read out scanned pixels. The co-processing module, implemented in the FPGA, determines scanning strategy and sends corresponding control parameters. Together, they enable rapid and complete readout of signal events through a two-stage process: sentinel monitoring followed by region scanning.

Under ROIRC operating mode, the GPD can detect low-energy X-rays in the 2–10 keV range. The Block-based readout mode enables multiple events detected within a single frame of sentinel scanning to be read out in different regions, effectively reducing scanning of invalid pixels. When signal event count rate is less than 15 k cm ^{2}s ^{1}, ROIRC readout rate for signal events increases linearly, meeting LPD application requirements. Due to ROIRC flexibility, its operating modes are diverse, making it particularly suitable for scenarios where pixel chips require large-scale assembly, low power consumption, and large detection areas.

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