Design and verification of a high-precision LLRF system for SXFEL

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Abstract

A high-performance low-level radio frequency (LLRF) control system based on a Zynq MPSoC platform has been developed for the digital and intelligent upgrade of the Shanghai Soft X-ray Free-Electron Laser (SXFEL). The system integrates eight 16-bit, 310-MSPS analog-to-digital conversion channels and two 16-bit, 500-MSPS digital-to-analog conversion channels, supporting both continuous-wave and pulsed operation modes. An FMC-LPC interface enables direct interoperability with the White Rabbit (WR) timing and control network, allowing real-time feedback on electron beam orbit, focusing, and energy variations. Experimental results on the SXFEL facility show that the proposed LLRF system achieves amplitude stability better than 0.03% (RMS) and phase stability better than 0.02° (RMS) at the output of the pulse compressor, demonstrating its capability to meet stringent stability requirements in modern FEL facilities.

Full Text

Preamble

Design and Verification of a High-Precision LLRF System for SXFEL

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Abstract

A high-performance low-level radio frequency (LLRF) control system based on a Zynq MPSoC platform has been developed for the digital and intelligent upgrade of the Shanghai Soft X-ray Free-Electron Laser (SXFEL). The system integrates eight 16-bit, 310-MSPS analog-to-digital conversion channels and two 16-bit, 500-MSPS digital-to-analog conversion channels, supporting both continuous-wave and pulsed operation modes. An FMC-LPC interface enables direct interoperability with the White Rabbit (WR) timing and control network, allowing real-time feedback on electron beam orbit, focusing, and energy variations. Experimental results on the SXFEL facility show that the proposed LLRF system achieves amplitude stability better than 0.03% (RMS) and phase stability better than 0.02° (RMS) at the output of the pulse compressor, demonstrating its capability to meet stringent stability requirements in modern FEL facilities.

Introduction

The Shanghai Soft X-ray Free-Electron Laser (SXFEL) is an advanced X-ray free-electron laser facility driven by a radio-frequency linear accelerator [**?**]. It is designed to operate across the soft X-ray spectral range, providing high temporal and spatial coherence, high peak brightness, ultrashort pulse durations, and continuously tunable wavelengths, making it a powerful platform for frontier research in X-ray science and related applications [**?**]. In 2021, SXFEL achieved free-electron laser amplification at wavelengths of 5.6 nm, 3.5 nm, 2.4 nm, and 2.0 nm, fully covering the "water window" spectral region. In particular, saturation was obtained at 3.5 nm with a peak power exceeding 500 MW [**?**], and the coherent radiation was reliably delivered to the experimental endstations, marking a significant advancement in the facility' s performance and operational maturity [**?**].

The SXFEL linear accelerator consists of five X-band, eleven C-band, and two X-band accelerating units [**?**], as illustrated in Fig. 1 [Figure 1: see original paper]. Beam stability measurements show that the injector delivered a relative energy stability of 0.01%, while the stability at the linac exit reached 0.03%. As part of the ongoing modernization and intelligent upgrade program, stringent performance targets have been defined, including inter-bunch timing consistency of the digitized timing system within 10 ms and a temporal resolution better than 2 fs in the digitized holographic diagnostic system. To fulfill these requirements, the low-level RF (LLRF) control system must incorporate a White Rabbit (WR) timing interface to ensure phase-locked synchronization and tight coordination with the global timing network.

Beyond precise timing synchronization, the digitalization of FEL facilities requires robust real-time and offline data analysis frameworks. These capabilities

enable continuous diagnostics, online optimization of radiation characteristics, and responsive feedback control, enhancing experimental efficiency and stability. However, these advancements impose demanding requirements on the computational performance and data throughput of the LLRF control hardware and necessitate advanced algorithmic optimization to achieve real-time, deterministic control under high-bandwidth operating conditions.

System Design

The intermediate frequency (IF) signal generated by the digital board can be output through two distinct approaches: vector modulation (VM) or frequency up-conversion [**?**]. In the up-conversion method, the I and Q components are used to modulate the IF signal [**?**]. The modulated IF signal is then mixed with the LO signal to up-convert it to the RF range. The process is expressed as: ωcos(ωsin( )ωcos(ωsin(ωcos( )ωsin(Where ωRF=ωc+ωIF.

The frequency upconversion method offers superior LO isolation and enhanced flexibility for achieving higher frequency outputs. However, this approach necessitates additional hardware, such as mixers and filters, to perform the upconversion process. Furthermore, it may introduce undesirable effects, including increased noise, phase distortion, and spurious signal generation, which can impact overall system performance [**?**].

In VM, the RF signal is directly generated by combining I and Q components with the LO signal. The VM process is mathematically represented as: ωcos(ωsin(Where I(t) and Q(t) are the modulating signals, ωc carrier signal. is the angular frequency of the Direct VM facilitates precise control over both amplitude and phase, making it particularly suitable for applications demanding high stability and accuracy. Additionally, the absence of an upconversion stage simplifies the system architecture, reducing both complexity and the risk of signal distortion. Therefore, VM output is selected in this case for RF signal modulation to ensure optimal performance and reliability.

Shown in fig.2, the newly developed low-level RF control system is composed of front-end frequency conversion electronics, Clock and Local Oscillator (LO) generator and digital processing boards, designed to achieve precise and reliable control of microwave signals. The front-end frequency conversion electronics are responsible for down-converting various collected microwave signals, such as the forward and reflected signals from solid-state amplifiers and klystrons, as well as the forward and reflected signals at the input and output of the accelerating structure, to an intermediate frequency (IF). These IF signals are then digitized by high-resolution, high-sampling-rate ADCs on the digital boards [**?**].

Within the digital boards, the digitized data undergoes a series of computational processes, including calibration, proportional-integral (PI) control, and phase and amplitude extraction through the CORDIC algorithm, among other operations [**?**]. These computations produce an I (in-phase) signal and a Q (quadrature) signal, which are fed back to the front-end frequency conversion

electronics. The IQ signals are then combined with a reference signal and undergo vector modulation (VM) to generate the final low-level RF output signal. This design ensures high precision and stability, meeting the stringent requirements of advanced accelerator systems.

The clock and local oscillator (LO) generator is designed to process the reference signal input through a series of operations, including frequency division, multiplication, mixing, filtering, amplification, and attenuation, to produce the required LO and clock signals. In the SXFEL system, the low-level RF control adheres to a four-times IQ sampling scheme, ensuring precise synchronization and signal fidelity [**?**]. This configuration is critical for achieving the stringent phase and amplitude stability demands in advanced accelerator applications [**?**].

2.1 Component Selection

The SXFEL operates in a pulsed acceleration mode, where achieving high beam stability critically depends on maintaining the flatness of the microwave field. However, during operation, the output signal from the low-level RF control system undergoes amplification through solid-state amplifiers and klystrons. This process introduces external perturbations, such as parasitic capacitance, that adversely affect the flatness of the pulsed microwave signal. Furthermore, inherent relative jitter in the pulse triggering mechanism exacerbates the impact of waveform non-uniformities, further compromising beam stability [**?**]. To mitigate these effects, precise modulation of the low-level RF control system' s output waveform is essential to ensure the pulse top flatness at the input of the accelerating structure. Therefore, we employ Intra-Pulse Amplitude Modulation (IPAM) to modulate the VM output waveform.

Mathematically, the modulated signal can be represented in as: ωcos(where S(t) is the modulated signal, A(t) is the time-varying amplitude function, Ψ is the angular frequency of the carrier signal, and ω is the phase. Feedback-based modulation can be expressed as: where Aref(t) is the desired amplitude profile, ΔA(t) is the deviation from the desired amplitude, and K is the gain factor of the control algorithm. The principle of Intra-pulse Amplitude Modulation is shown in figure 3 [Figure 3: see original paper].

High-resolution digital-to-analog conversion plays a pivotal role in this modulation process, enabling the fine adjustments required to achieve the desired flatness. Based on the system requirements, a DAC with a resolution of 16 bits and a sampling rate exceeding 250 MSPS has been selected. This specification ensures the capability to perform high-precision modulation, thereby safeguarding the stability of the pulsed microwave signals and ultimately enhancing overall beam performance.

For the selection of the ADCs, considering that the SXFEL system imposes an overall beam stability requirement of less than 0.03%, higher resolution is generally preferred. This is because the effective number of bits (ENOB) of the ADC is typically lower than the nominal resolution after accounting for

non-idealities. However, balancing performance, cost, and practical implementation considerations, a resolution of 16 bits was chosen. Similar to the DAC selection, a high sampling rate is critical to ensure the effective operation of the flatness modulation feedback loop. Given the use of IQ modulation, an ADC with a sampling rate exceeding 250 MSPS is preferred to meet these stringent performance requirements.

2.2 Digital Board Schematic Design

The whole schematic of the digital board is shown in fig.4. In the Xilinx Zynq series architecture, two modules are integrated: the Processing Logic (PL) and the Processing System (PS), connected via a high-speed AXI bus. The PL module functions as a traditional FPGA, handling data acquisition and transmission, while the PS module serves as the processor core, responsible for data processing and controlling the output signals.

In the design of the low-level RF digital board, the PL module is equipped with four dual-channel 310 MSPS 16-bit ADCs, enabling eight-channel data acquisition. Additionally, two dual-channel 500 MSPS 16-bit DACs are integrated, where one DAC outputs I and Q signals for pulsed operation after differential amplification, and the other DAC directly generates continuous-wave I and Q signals. The PL module also connects to various interfaces, including SD card, SFP, HDMI, RJ45, and DC ADC ports.

On the PS module, 8 GB of DDR4 memory is deployed, along with an M.2 SSD interface, USB UART interface, USB 3.0 ports, and an RJ45 network interface. During operation, microwave signals are first down-converted to intermediate frequency (IF) by the front-end frequency conversion electronics and then digitized by the ADCs connected to the PL module. The PL module demodulates the digitized signals and transfers the processed data to the PS module via the AXI bus. The PS module utilizes the demodulated signals—typically microwave samples from the input of accelerating structure—to perform vector modulation (VM), proportional-integral (PI) control, and other signal processing tasks for the RF output.

2.3 Front-End Frequency Converter and Local Oscillator/Clock Generator

The signals such as the output of the LLRF system itself, the output of the solid-state amplifier, the output and reflection of the klystron, the output and reflection of the pulse compressor, and the output and reflection of the accelerating structure, are collected via directional couplers and subsequently subjected to down-conversion processing of their pulse signals [**?**].

The schematic of Front-end frequency converter and Local Oscillator/Clock generator is shown in fig.5. Synchronization clock reference for the soft system is derived from 2856/108, meaning all clock signals, local oscillator signals, and

other related frequencies must align with this reference. To ensure compatibility with the existing SXFEL equipment and to maximize the performance of the 310 MSPS ADC, we have selected 2856/54 = 52.889 MHz as the intermediate frequency (IF). Given the use of four-fold IQ sampling, the clock frequency is therefore set to 211.556 MHz. During the operation of the Local Oscillator/Clock generator, the 2856 MHz master oscillator (MO) signal is first passed through a 1-to-4 power divider. Two of the divided outputs serve as direct reference signals. One of the remaining signals undergoes a ninth frequency division to generate a 317.333 MHz signal, which is subsequently filtered, amplified, and split into two signals. Another divided output is processed through a two-third frequency division, followed by filtering, amplification, and power division, to produce two 211.556 MHz clock signals. Meanwhile, an additional signal undergoes a two-stage frequency division to generate a 52.889 MHz intermediate frequency (IF) signal. This IF signal is then mixed and down-converted with a separated portion of the original 2856 MHz MO signal. After further filtering and amplification, the system outputs a local oscillator signal at 2803.111 MHz.

2.4 Vector Modulation

After the IF signal is generated by the digital board, the RF signal is produced through vector modulation (VM) techniques. Vector modulation involves generating a baseband signal through digital signal processing, followed by conversion to the desired frequency band using digital-to-analog converters (DACs) [**?**]. The general mathematical representation for a vector-modulated output is shown in equation 5. sin)(where: I(t) and Q(t) are the in-phase and quadrature components, respectively, fc is the carrier frequency. Compared to direct up-conversion, VM offers superior precision, greater flexibility, lower distortion, and a broader bandwidth, making it a highly advantageous technique for high-performance applications.

2.5 Bunch ID Retrieval

To integrate Bunch-ID into detectors, each spectrum acquisition signal must be tagged with the corresponding pulse number. The defined target devices requiring Bunch-ID include diagnostic equipment and various detectors. The synchronization port is an Ethernet interface connected to a timing switch to synchronize timing signals. The timing Bunch-ID is encoded and transmitted through the FMC interface using a custom protocol. The timing system supplies decoding code for the Bunch-ID at the target device end, which must be integrated on the target device to annotate its data.

Additionally, the Bunch-ID can be used to provide the delay time between each free-electron laser pulse experiment and the laser pump pulse. This enables precise synchronization and alignment for advanced experiments and diagnostics. In the design process, we reserved two HP banks in the Zynq chip to interface with the FMC-LPC connector, supporting data rates of up to 1.8 Gbps. This

configuration ensures high-speed acquisition of Bunch ID and precise synchronization with the external White Rabbit timing system.

2.6 Timing Distribution

In high-precision mixed digital and RF systems, the clock signal determines not only the reference timing for data acquisition (ADC) and signal generation (DAC), but also directly influences the overall noise level in the conversion process [**?**]. For a DAC, its output noise can be viewed as the superposition of two components: the intrinsic noise (e.g., quantization noise and thermal noise) and the noise introduced by clock jitter. Specifically, when the clock exhibits random jitter (RJ) or periodic jitter (PJ), there is a slight timing offset Δt between the ideal sampling instant and the actual sampling instant, resulting in an amplitude error in the DAC output. Under small-signal approximation, the RMS amplitude error due to random jitter can be expressed as:

Where fsig is the fundamental frequency of the DAC output and Vpeak is the peak amplitude. σt is the RMS value of the clock jitter.

The total output noise power can then be approximated by: where Nin represents the DAC' s inherent noise. Clock phase noise thus manifests as timing jitter, which directly translates into amplitude and phase errors in the output, ultimately degrading signal fidelity and signal-to-noise ratio. In practical implementations, in addition to selecting high-quality clock sources with low phase noise, careful attention must be paid to the power integrity and isolation of the clock distribution network. Ferrite beads and decoupling capacitors are added to both the clock distribution chips and DAC power rails to suppress high-frequency ripples and electromagnetic interference, thereby reducing noise coupling into the clock lines. Differential routing and solid ground planes are employed to mitigate parasitic coupling and crosstalk. Together with proper reference voltage design and board-level shielding, these measures minimize the impact of clock input noise on DAC output quality, ensuring excellent linearity and stability in high-speed, high-accuracy applications.

In our overall system design of this digital board for low-level control applications, four clock distribution chips are employed to ensure high clock quality and consistency across all functional modules. The first distribution chip supplies phase-synchronous clock signals to the four ADCs, while the second one drives both DACs and the FMC interface, thus ensuring synchronized data conversion and transmission. The third chip is dedicated to capturing and distributing the external trigger input, enabling fast and stable trigger synchronization. Finally, the fourth chip provides an additional frequency offset through fine-tuning of the output clock, thereby offering flexibility for subsequent control and compensation tasks.

3. Hardware Design

The stability requirements for the SXFEL beam impose stringent performance targets on the LLRF system, as summarized in Table 1 .

Characteristics	S-Band	C-Band
Working frequency (GHz)		
Repetition rate (Hz)		
Amplitude stability (%) (RMS)	<0.03	<0.03
Phase stability (deg.) (RMS)	<0.03	<0.06
VM output level (dBm)	-10-10 dBm	-10-10 dBm

3.1 DSP Board

In the design and fabrication of this digital board, the XCZU19EG was chosen as the core processing device primarily because of its comprehensive advantages in resource capacity, flexible I/O structures, and support for high-speed interfaces. The XCZU19EG belongs to the Xilinx Zynq UltraScale MPSoC family, featuring a quad-core ARM Cortex-A53 and a dual-core ARM Cortex-R5 processing subsystem, along with abundant programmable logic resources. This single-chip solution seamlessly integrates high-speed data processing, real-time control, and embedded software execution. Compared with other devices in the same family, the XCZU19EG provides a larger number of LUTs, registers, and DSP slices, as well as higher-bandwidth transceivers, making it well-suited for multi-channel, high-speed data acquisition and transmission.

In our design, four ADCs (16-bit, 310 MSPS) and two DACs were incorporated to achieve high-precision, high-speed data conversion. Because both the acquisition and transmission ports involve high data width and rate, meeting logic resources and real-time processing requirements necessitates sufficient high-bandwidth I/O within the FPGA. Taking the ADC as an example, throughput per channel can be estimated by equation below:

N×R×fs=Dth

where fs is the sampling rate, R is the resolution, and N is the number of channels. For AD9652, fs=310 MSPS, R=16 bits and each ADC contains two channels. Therefore, one ADC can deliver up to 310$×10^{6}$$×16×$2=9.92 Gbps. Given such a large data flow, the High Performance I/O (HPIO) of the XCZU19EG plays a pivotal role in supporting high-throughput, low-latency data transfer. In this design, the four ADCs and two DACs are all connected to the programmable logic of the XCZU19EG via HPIO, enabling efficient data reception and real-time signal processing.

Moreover, the XCZU19EG provides multiple high-speed interface options, including SFP ports for remote data communication and an FMC connector for system expansion. The SFP ports enable long-distance, high-speed, low-latency

data transmission, while the FMC interface offers flexibility for adapting various custom or off-the-shelf function modules, facilitating future system upgrades and expanded capabilities. Consequently, the XCZU19EG—by virtue of its high integration, robust performance, and flexible I/O features—enables a compact, extensible, and reliable digital board design, effectively meeting the multi-channel, high-speed acquisition and signal processing requirements of this project.

As illustrated in Figure 6 [Figure 6: see original paper], the overall design layout and the final fabricated board are presented. The ADC inputs, clock signal and external trigger interfaces, as well as the DAC outputs, are all routed through SMA connectors.

3.2 RF Front-End Frequency Mixer and VM Module

Shown in Fig.7, the RF front-end adopts a separated layout for the down-conversion and vector modulation (VM) modules to reduce mutual interference and maintain signal integrity between channels. Each functional block is enclosed in individual metal shielding housings, and the measured inter-channel isolation remains above 70 dB, effectively suppressing local-oscillator leakage and unintended coupling. Multi-stage low-pass filtering is introduced in the IF and baseband paths to remove harmonic and spurious products arising from the mixing process, which improves spectral cleanliness and preserves the linearity of amplitude and phase control. The high-frequency transmission sections employ low-loss Rogers dielectric substrates, reducing dispersive effects and temperature-induced phase drift, and ensuring stable characteristics over extended operating conditions. A dedicated stabilized power distribution scheme is used, with separate regulation for the analog modulation path and digital control circuits, limiting ripple and switching noise propagation toward sensitive analog nodes. This hardware configuration provides the required precision in vector modulation and frequency conversion for LLRF systems operating in high-stability accelerator environments.

The frontend module comprises eight RF down-conversion channels and a vector modulator driven by DAC-generated I/Q baseband signals referenced to a common low-noise master source. The reference and LO signals are distributed through a passive matched network with controlled impedance and length-matched routing, so that the relative phase between channels is determined by layout rather than active conditioning elements. Gain and phase trims are applied during calibration to correct residual I/Q imbalance and DC offsets. Channel responses are adjusted to maintain uniform group delay and amplitude characteristics, which allows coherent field reconstruction across channels. In this configuration, the measured short-term amplitude stability is better than 0.015%, and the integrated phase jitter is below 25 fs (rms) over the 10 Hz–10 MHz offset range. These values were obtained under stabilized power and thermal conditions using standard amplitude Allan-deviation evaluation and phase-noise integration procedures, and remained consistent across repeated measurements. The resulting performance meets the requirements for high-

stability LLRF operation in accelerator environments.

3.3 Assembled LLRF Controller

The assembled LLRF controller is shown in fig.8. To ensure reliable thermal management during continuous operation, a machined aluminum heat-spreading plate is mounted directly above the DSP board, providing an efficient conduction path for dissipating heat from the ZYNQ processing device, Ethernet transceiver, and on-board power regulation components. The DSP board is interfaced with the FMC carrier card via a high-density FMC ribbon connector, ensuring stable high-speed digital communication and consistent signal timing. RF interconnection between the DSP board, the front-end frequency-conversion stage, and the vector modulation (VM) module is implemented using short, phase-matched SMA coaxial links to minimize insertion loss and preserve channel isolation. At the VM module output, a cavity-type narrowband filter with a $±$5 MHz passband is incorporated to suppress residual LO feedthrough and spurious mixing components, thereby improving spectral purity and reducing interference between the reference and RF drive signals.

Firmware Design

The actual firmware implementation is illustrated in Figure 9 Figure 9: see original paper. In this architecture, the digitized baseband or intermediate-frequency (IF) data first pass through a finite impulse response (FIR) filter [**?**], which serves to attenuate out-of-band noise and spurious components while preserving the desired signal bandwidth. Mathematically, a standard M-tap FIR filter with impulse response h[k] implements the convolution knxkh where x[n] denotes the input signal samples, and y[n] is the filtered output. By carefully designing h[k] based on the passband and stopband specifications, this FIR stage ensures both spectral shaping and pre-conditioning of the signals for subsequent IQ-based amplitude and phase extraction [**?**]. Once filtered, the in-phase (I) and quadrature (Q) components proceed to the calibration module for offset or gain mismatch compensation before reaching the CORDIC (Coordinate Rotation Digital Computer) engine.

The digital signal processing architecture is developed using Xilinx System Generator, where functional blocks are implemented at the schematic level and subsequently translated into synthesizable Verilog code through the System Generator workflow. Shown in fig.9(b), the entire processing chain operates at a clock frequency of 105.667 MHz, identical to the sampling rates of both the ADCs and DACs, ensuring synchronous data movement across the system. Packaged functional modules are used to encapsulate arithmetic and control logic, allowing the design effort to focus on computational behavior and timing closure rather than low-level data type handling. Building on this framework, a four-stage pipelined IQ demodulator is being integrated, providing continuous quadrature baseband extraction at the full 105.667 MHz rate. This pipelined structure improves throughput and timing margins, enabling stable I/Q component output

while preserving phase accuracy under high-speed operating conditions.

As shown in Fig. 9(c), the system supports multiple operating modes that can be selected through a dedicated control register. The mode selection register can be accessed and modified online via the embedded Linux environment, allowing configuration changes to be performed without interrupting system operation. This mechanism provides enhanced operational flexibility and broadens the applicability of the controller across different machine conditions, tuning procedures, and diagnostic workflows.

The down-conversion and baseband extraction stage employs a 16-bit ADC/DAC interface, which necessitates a 16-stage real-time pipelined CORDIC architecture for vector magnitude and phase computation, shown in fig.9(d). The CORDIC module operates at the system clock of 105.667 MHz, producing amplitude and phase outputs at the full sampling rate. After quantization optimization, the amplitude component is represented with 15-bit resolution and the phase component with 17-bit resolution, providing sufficient dynamic range for downstream feedback and feedforward control loops. The computed I/Q-derived amplitude and phase signals are delivered directly to higher-level control algorithms without additional decimation or rate conversion, preserving timing determinism and minimizing processing latency in the closed-loop system.

CORDIC provides a computationally efficient means of performing polar-to-Cartesian or Cartesian-to-polar transformations via iterative shift-and-add operations rather than explicit multiplications. In its rotation mode, for example, given initial variables (x0, y0, z0) and a predefined set of rotation angles αk, CORDIC iterates according to where σk {+1,-1} determines the rotation direction at step k. For amplitude and phase estimation, one can initialize z0=0 and iterate until yk 0, at which point xk converges to the signal magnitude while zk represents the accumulated rotation angle (i.e., the instantaneous phase). This computationally lightweight algorithm seamlessly integrates into real-time systems, facilitating high-throughput amplitude-phase determination or rotation in applications such as LLRF control and advanced digital beam-forming.

To support shot-to-shot beam tuning and rapid recovery during FEL commissioning, an absolute time stamp is appended to each acquired amplitude and phase data frame within the EPICS data stream. The time stamp is synchronized to the White Rabbit (WR) timing network and is associated with the pulse trigger, bunch identifier, and global timing markers distributed by the accelerator control system (shown in fig 9(e)). This pulse-resolved timing tag is inserted by replacing the corresponding column in the process variables (PVs), thereby ensuring that each recorded RF diagnostic sample can be unambiguously mapped to a specific electron bunch. As a result, beam commissioning personnel can perform pulse-by-pulse correlation analysis between RF field evolution and beam performance metrics, enabling faster identification of perturbations and reducing the time required to re-establish optimal lasing conditions.

Test Result

The first low-level RF controller deployed in our system is designed for operation in the C-band at 5712 MHz, corresponding to the accelerating structures used in the initial commissioning stage of the facility. Figure 10 Figure 10: see original paper illustrates the eight-channel PYDM monitoring interface, which provides real-time visualization of key RF diagnostics. The displayed channels include the cavity input signal at the accelerator section, the klystron output and reflected signals, as well as the output signal from the solid-state power amplifier. This interface enables operators to observe amplitude and phase variations across multiple stages of the RF chain simultaneously, thereby supporting efficient beam tuning and system stability assessment.

Figure 10(c) presents the stability test results of the VM output. As shown, the measured performance indicates that the VM maintains an amplitude stability better than 0.015% (RMS) and a phase stability better than 0.015° (RMS) at 5712 MHz. These results confirm that the vector modulation stage provides sufficiently low noise and drift characteristics to support high-precision field regulation in C-band accelerating structures.

Figure 10(d) shows the stability performance of the pulse compressor output signal. The measured results indicate an amplitude stability better than 0.03% (RMS) and a phase stability better than 0.02° (RMS), which can meet the requirement from SXFEL commissioning. The low-level RF controller described above has been deployed on the SXFEL supporting subsequent user facility and operated under beam conditions, experiments. The system has maintained continuous and stable operation for more than three months.

6. Conclusion and Outlook

A high-performance LLRF digital control system has been developed for the SXFEL upgrade. The system is based on the Xilinx Zynq XCZU19EG MPSoC and integrates eight 16-bit, 310-MSPS ADC channels and two 16-bit, 500-MSPS DAC channels. Experimental evaluation in SXFEL demonstrates high stability, achieving amplitude and phase stabilities of 0.015% (RMS) and 0.015° (RMS) at the vector modulator output, and 0.03% (RMS) and 0.02° (RMS) at the pulse compressor output under C band. These results satisfy the stringent stability requirements of the upgraded SXFEL. The system has been in continuous stable operation for more than three months, confirming its long-term robustness and suitability for accelerator operation.

References

[1] Z.T. Zhao, D. Wang, L.X. Yin et al., Shanghai soft X-ray free-electron laser facility. Chin. J. Lasers 46(1), 0100004 (2019). https://doi.org/10.3788/CJL201946.0100004 (in Chinese)

[2] C. Feng, H.X. Deng, Review of fully coherent free-electron lasers. Nucl. Sci. Tech. 29, 160 (2018). https://doi.org/10.1007/s41365-018-0490-1

[3] Liu, B.; Feng, C.; Gu, D.; Gao, F.; Deng, H.; Zhang, M.; Sun, S.; Chen, S.; Zhang, W.; Fang, W.; et al. The SXFEL Upgrade: From Test Facility to User Facility. Appl. Sci. 2022, 12, 176. https://doi.org/10.3390/app12010176

[4] Z.T. Zhao, C. Feng, K. Zhang, Two-stage EEHG for coherent hard X-ray generation based on a superconducting linac. Nucl. Tech. 28, 117 (2017). https://doi.org/10.1007/s41365-017-0258-z

[5] Yu, Cheng, et al. "Status of Various Types of Undulators at SXFEL." IEEE Transactions on Applied Superconductivity 34.5 (2024): 1-4.

[6] Z.Q. Geng, Beam-based optimization of SwissFEL low-level RF system. Nucl. Sci. Tech. 29, 128 (2018). https://doi.org/10.1007/s41365-018-0460-7

[7] Junqiang Zhang, et al., A precision LLRF control system for UED, Nucl. Instrum. Meth. A, Volume 1021, 2021, 165587

[8] Yiming Xu, et al., Design and verification of adaptive control to generate flat-top radio frequency power output of pulse compressor for SXFEL, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors Associated Equipment, Volume 1031, 2022, 166596. https://doi.org/10.1016/j.nima.2022.166596.

[9] Cheng-Cheng Xiao, et al., Design and preliminary test of the LLRF in C band high-gradient facility SXFEL, NUCL TECH 31, (2020), https://doi.org/10.1007/s41365-020-00806-6.

[10] Han, J. W., et al. "An Intra-pulse feedforward algorithm for improving pulsed microwave stability." arXiv preprint arXiv:2310.15968 (2023).

[11] XIAO Chengcheng, et al., Design and test of a C band local oscillator and clock device in LLRF, NUCLEAR TECHNIQUES, January 2021, Vol.44, No.1.

[12] Zhang Junqiang, et al., A beam energy feedback for ultrafast electron diffraction facility, HIGH POWER LASER AND PARTICLE BEAMS, Jun. 2020, Vol. 32, No. 6.

[13] Fu, K Fong, Z Yin, et al., A digital phase-locked loop based LLRF system[J]. Nuclear Instruments & Methods in Physics Research, 2020, 962(May11):163688.1-163688.7.

[14] Xie, Zhexin, et al. "Preliminary Design of CSNS-II LINAC SRF LLRF based on C-ADS Injector I." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 1072 (2025):

[15] Li, Z., Du, B., Wu, K., Pang, J., Qin, J., & Zhao, L. (2024). An MTCA-based LLRF prototype system of LINAC in Hefei Advanced light facility. Nu-

clear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 1069, 169901.

[16] Tamura, Fumihiko, et al. "Commissioning of the next-generation LLRF control system for the Rapid Cycling Synchrotron of the Japan Proton Accelerator Research Complex." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 999 (2021): 165211.

[17] Tu, Xiude, et al. "The analysis of beam stability and improvement of RF system at HUST THz-FEL by digital LLRF." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 1011 (2021): 165588.

[18] Yiming XU, Chengcheng XIAO, Wencheng FANG. Design and test of multi-variable estimation-based calibration for vector modulator (J/OL). Nuclear Techniques, 2024, (11): 2025-01-09.2025-11-11. https://www.sciengine.com/doi/10.11889/j.0253-3219.2024.hjs.47.110202.

Note: Figure translations are in progress. See original paper for figures.