

## Performance study of a prototype readout electronics for the time-of-flight detectors of HIAF-HFRS facility

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**Date:** 2025-10-11T21:34:31+00:00

### Abstract

In the High Energy FRagment Separator (HFRS) at the High Intensity heavy-ion Accelerator Facility, plastic scintillation detectors are used for high-precision time-of-flight (ToF) measurements to identify the secondary ions from the reaction between the primary beam and the target. During the day-one experiments, the readout electronics for the ToF detectors is required to achieve a time resolution of 94 ps (full width at half maximum, FWHM) with a counting rate up to  $10^6$  counts per second (cps) and per channel. This study presents a prototype readout electronics for plastic scintillation ToF detectors. The system comprises a constant-fraction discriminator, a level conversion board, and a time digitization board. We developed an octal logic signal adapter to convert nuclear-instrument-module signals into low-voltage-differential-signaling standard. For time digitization, a field programmable gate array is utilized through the internal tapped delay line. The system's time resolution and counting rate performance were evaluated using a high-precision pulse generator and a picosecond pulsed laser. The test results indicate that the single-channel time resolution is around 24 ps FWHM, with a maximum counting rate of  $1.6 \times 10^6$  cps. The overall average ToF resolution achieves 42 ps FWHM during the laser test at a repetition rate of 1 MHz. These results validate that the developed system meets the requirements of the HFRS beamline for ToF resolution and counting rate.

### Full Text

### Preamble

**Performance Study of a Prototype Readout Electronics for the Time-of-Flight Detectors of the HIAF-HFRS Facility**

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In the High Energy Fragment Separator (HFRS) at the High Intensity Heavy-Ion Accelerator Facility, plastic scintillation detectors are employed for high-precision time-of-flight (ToF) measurements to identify secondary ions from reactions between the primary beam and target. For the day-one experiments, the readout electronics for the ToF detectors must achieve a time resolution of 94 ps (full width at half maximum, FWHM) with a counting rate up to  $10^6$  counts per second (cps) per channel. This study presents a prototype readout electronics system for plastic scintillation ToF detectors, comprising a constant-fraction discriminator, a level conversion board, and a time digitization board. We developed an octal logic signal adapter to convert nuclear instrument module (NIM) signals into low-voltage differential signaling (LVDS) standard. For time digitization, a field-programmable gate array (FPGA) is utilized through an internal tapped delay line. The system's time resolution and counting rate performance were evaluated using a high-precision pulse generator and a picosecond pulsed laser.

The test results indicate that the single-channel time resolution is approximately 24 ps FWHM, with a maximum counting rate of  $1.6 \times 10^6$  cps. The overall average ToF resolution achieves 42 ps FWHM during the laser test at a repetition rate of 1 MHz. These results validate that the developed system meets the HFRS beamline requirements for both ToF resolution and counting rate.

**Keywords:** HIAF-HFRS, plastic scintillation detectors, time-of-flight (ToF), time-to-digital converter (TDC), high counting rate, trigger-less, readout electronics

## INTRODUCTION

Radioactive ion beam facilities have played a crucial role in the physics of exotic nuclei for over three decades [1–3]. In-flight separation stands out as one of the primary techniques for producing and investigating exotic nuclei [4]. Currently, several prominent laboratories worldwide operate in-flight separators, including BigRIPS at RIKEN-RIBF in Japan [5], ARIS at FRIB in the USA [6], FRS at GSI in Germany [7], and RIBLL at HIRFL in China [8, 9]. Furthermore, upcoming years will see the operation of new state-of-the-art separators such as Super-FRS at FAIR in Europe [10] and the High Energy Fragment Separator (HFRS) at the High Intensity Heavy-Ion Accelerator Facility (HIAF) in China [11, 12].

At HIAF-HFRS, a significant number of exotic nuclei far from the line of stability

can be produced. Accurate identification of each ion is essential for subsequent experiments. Typically, the  $\Delta E$ -ToF-B technique is employed to accomplish particle identification, which entails simultaneously measuring the energy loss ( $\Delta E$ ), time-of-flight (ToF), and magnetic rigidity ( $B$ ) to determine the proton number ( $Z$ ) and mass-to-charge ratio ( $A/Q$ ) of the ions [13, 14]. Simulations for the HFIRS beamline suggest that to achieve reliable particle identification, a ToF resolution of 94 ps (all time resolution values reported in this work correspond to the full width at half maximum, FWHM) is required [12]. Furthermore, these simulations predict a maximum secondary beam intensity of approximately one million particles per second. Consequently, it is imperative to employ a time-of-flight detector with superior timing performance and high-intensity beam capability to accurately measure the ToF.

Plastic scintillation detectors are among the most mature and widely used ToF detectors, offering high time resolution at relatively low cost. These features have led to their extensive application in various radioactive beam lines worldwide, including BigRIPS at RIKEN-RIBF [14], ARIS at FRIB [6], Super-FRS at FAIR [15], and RIBLL1 and RIBLL2 at HIRFL [16, 17]. Given the established performance and reliability of plastic scintillators in similar contexts, it would be prudent for the HFIRS facility to prioritize plastic scintillation detectors for its own ToF detection system. A prototype of the plastic scintillation ToF detectors for HFIRS has been built, and its timing performance was evaluated using conventional electronics consisting of Mesytec MCFD16 and MTDC32 modules [18]. The best ToF resolution achieved was approximately 24 ps. However, due to inherent conversion and readout times, this commercial electronics system is limited in terms of counting rate, with a maximum single-channel capacity of 700 kilo-counts per second (kcps). In addition, the MTDC32 module requires an external trigger signal to operate.

In modern time measurement readout electronics, time-to-digital converters (TDCs) implemented using both application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs) are widely used across various applications [19–22]. Given the advantages of lower cost and higher flexibility, FPGA-based TDCs have been extensively employed in time-of-flight measurements for nuclear physics experiments [19, 23–25]. According to the latest review [19], the tapped delay line (TDL) architecture stands out among mainstream TDC structures. Ultra-high time resolutions have been achieved using TDL-based TDCs on Xilinx Kintex-7 FPGA [26–28] and Xilinx Zynq Ultrascale+ FPGA [29, 30]. The time resolution measured using FPGA-based TDCs is shown in Table 1. In the Cooling Storage Ring External-target Experiment (CEE) at the Heavy Ion Research Facility in Lanzhou (HIRFL), the readout electronics prototype for the ToF detectors has achieved an electronic time resolution better than 24 ps [24, 31]. The ToF system of the CBM experiment at FAIR has achieved an electronic time resolution better than 47 ps using FPGA TDC technology [32]. The high-granular neutron ToF detector (HGND) for the BM@N experiment has developed a 344 ps TDC based on a Kintex-7 FPGA [33]. In the HL-2A tokamak device, a real-time double-ring neutron ToF spec-

trometer system achieved a time resolution of 122 ps based on FPGA TDC technology [34].

Considering the successful applications of FPGA-based TDCs in nuclear physics experiments, we aim to design a readout electronics system based on FPGA for plastic scintillation ToF detectors capable of achieving an electronic time resolution better than 47 ps under a counting rate up to 1 MHz for a single channel. The readout electronics comprises a constant-fraction discriminator, a level conversion board, and a time digitization board.

## II. Structure of the Readout Electronics

The block diagram of the readout electronics system for the plastic scintillation ToF detector is shown in Fig. 1 [Figure 1: see original paper]. It mainly consists of three parts: a constant-fraction discriminator (CFD), a logic level converter, and a time-to-digital converter (TDC). The analog negative signals from the photomultiplier tubes (PMTs) of the detectors are sent to the CFD for timing, which generates logic signals with fast negative NIM standard. To meet the requirements of the high-precision and ultra-fast TDC, these logic signals are converted into low-voltage differential signaling (LVDS) standard by a NIM-to-LVDS level converter. The LVDS signals are subsequently transmitted to the TDC board for digitization, where they are interfaced with the following data acquisition (DAQ) system via either a USB 3.0 cable or an optical fiber.

For the timing method, constant-fraction discrimination was chosen to meet the stringent requirements for ToF resolution and counting rate of the HFRS beamline. Currently, a constant-fraction discriminator addressing this demand is under development. In the present work, we selected a commercial CFD—ORTEC Model-935 [35]—to serve as a provisional substitute for the developing unit. The Model-935 is capable of performing constant-fraction timing on fast signals as narrow as 1 ns, making it suitable for applications involving very fast detectors such as the plastic scintillators utilized at HFRS. The maximum input rate for this module can reach 200 MHz, which meets the counting-rate requirement of exceeding 1 MHz at HFRS. In addition, its input range from 0 to -10 V accommodates the relatively large signals from PMTs, ensuring compatibility with the ToF detectors.

The fast negative NIM output signals from the Model-935 are processed by the logic level converter and the time-to-digital converter, which have been meticulously designed and manufactured. We have developed a prototype consisting of two custom boards, whose specifications and functionalities are described in the following sections.

## III. Design of the Logic Level Converter

The photograph of the NIM-to-LVDS logic level conversion board is shown in Fig. 2 [Figure 2: see original paper]. The converter primarily comprises two

key components: the conversion of NIM signals to TTL signals, followed by the conversion of TTL signals to LVDS differential signals with strong immunity to noise interference and low power consumption [36]. The NIM signal output from the constant-fraction timing discriminator is passed to a differential amplifier to generate an MECL signal, which is subsequently converted into a TTL signal. Then the TTL signals are converted into LVDS signals.

In the present design, we have implemented an 8-channel logic level converter board. The specific parameters of this board are detailed in Table 2. It supports a maximum input rate of 20 MHz. The driver is compatible with NIM input standards and adheres to the LVDS output standard.

## IV. Design of the Time-to-Digital Converter

The photograph of the TDC board we developed is presented in Fig. 3 [Figure 3: see original paper]. This board integrates a time-digitization module for precise time measurement and a data-transfer module for fast data transmission. To adapt to the high-speed LVDS signals, we have selected the DS25BR150 chip manufactured by Texas Instruments, which features an integrated  $100\text{-}\Omega$  termination resistor [37]. This configuration typically introduces a random jitter of approximately 1 ps, contributing minimally to the overall system time jitter. The LVDS signal, after being driven by a high-speed buffer, is sent into the High Range (HR) BANK of a Kintex-7 FPGA xc7k325T from AMD Xilinx, which is specifically designated for receiving and processing time-digitized signals.

### A. High-Precision Time-Digitization Module

Dead time significantly impacts the performance of the readout electronics system at high counting rates. To measure adjacent hit signals effectively for TDCs, it is crucial to minimize the conversion time interval between successive hits, ideally approaching zero. In the high-precision time digitization board we designed, all functional modules operate in a pipeline architecture with virtually zero dead time during data transfer. All measured data will be recorded by the TDCs without any external trigger for the DAQ system, which is called triggerless mode. Fig. 4 [Figure 4: see original paper] shows the overall architecture design of the TDC. The high-precision time digitization module is implemented by an FPGA-based TDC module, which is constructed using a time interpolation method [38]. In this design, a 500-MHz counter generates “coarse-time stamps” while intra-cycle subdivision produces “fine-time stamps” through delay line analysis. By combining coarse-time stamps and fine-time stamps, high time measurement precision can be achieved. The designed high-precision time digitization system mainly consists of four components: the coarse time counter module, the delay line module (latch arrays), the fine time encoding module, and the data storage FIFO arrays. The area occupancy of the TDC in this design is 3269 LUTs (203800 in total), 6678 Registers (407600 in total), and 2579 Slices (50950 in total).

When the high-precision time measurement board is powered on, a 40 MHz clock on the board is used to generate multiple clocks through a phase-locked loop (PLL): a 500 MHz TDC clock, a 300 MHz clock for reading and packaging TDC data from first-in-first-out (FIFO) memories, and a 100 MHz system clock for data transfer from the backend USB 3.0 module. In this design, the working clock of the TDC module is a high-frequency 500 MHz clock, while the working clock of the backend data processing and transmission module is 100 MHz. The addition of the FIFO array serves another purpose: to isolate clock domains and prevent timing issues.

In this design, the used TDC for each channel consists of a coarse counter, a 188-tap delay line, a D-type flip-flop (DFF) bank, a fine time encoder, and a data storage FIFO. Once activated, the 44-bit coarse time counter array begins continuously sampling at the 500 MHz frequency. Meanwhile, the LVDS input signal is first sent to the trigger unit to generate the hit signal. This hit signal propagates through the delay line and is sampled by the D flip-flop array at the rising edge of the next clock cycle. After sampling, the delay line data is encoded by the encoding module, resulting in an 8-bit fine time. Finally, the combination of coarse time and fine time together represents the timing information of the measured signal.

The block diagram of the single-chain TDL FPGA TDC is shown in Fig. 5 [Figure 5: see original paper], which illustrates the use of multi-CARRY4 cascade to construct a single-chain TDL for fine time measurements. In our design, the high-resolution TDC is constructed by cascading dedicated carry logic units on the Kintex-7 FPGA, which feature dedicated routing and minimal internal propagation delay. Multiple CARRY4 logic blocks are used to build the delay line, with the carry outputs (CI, CO[3]) of the CARRY4 units interconnected. The carry output of the CARRY4 is used as the tap output. The TDL performs fine time measurement within intervals shorter than the coarse time (2 ns). The TDL is constructed from a cascade of 47 CARRY4 logic units to ensure that the delay time of the TDL exceeds one TDC clock cycle, thereby meeting the total delay time requirement. When there is no hit signal in the delay line, the output of the delay line is all “0”, meaning that the raw position encoding sampled at the rising edge of the TDC clock is also all “0”. When the hit signal propagates through the delay line, the areas that the hit signal has not passed through will output “0”, while the areas that the hit signal has passed through will output “1”. Moreover, the corresponding CARRY4 logic unit’s CO will transition from “0” to “1”. At this point, the delay line is sampled by the D flip-flop array, which will output a pattern like “...000011111...”, where the position of the 0-to-1 transition corresponds to the fine time of arrival of the signal in one clock cycle [39].

The function of the encoder module is to convert the thermometer code sampled by the D-type flip-flop array into binary code. This is achieved by step-by-step calculation, where the logical “1” values from the entire carry chain output are summed and finally encoded into 8-bit data. Currently, we are using the Wallace

encoder, which reduces encoding errors caused by bubble errors. Fig. 6 [Figure 6: see original paper] shows the process of encoding the TDC fine-time stamp in one clock cycle. The raw position encoding is first grouped into sets of 6 bits. We use the 6-input LUT (LUT6) from the underlying logic resources of the Kintex-7 FPGA to convert the number of logical “1”s in each group into a 3-bit count output [40]. Then, we use a 2-input adder to convert the 3-bit count of each group into a 4-bit encoding. This process is repeated multiple times using adders, ultimately resulting in an 8-bit fine time data corresponding to the delay chain position output encoding.

## B. Ultra-Fast Data-Transfer Module

Our high-precision time measurement electronics system is designed to operate in a trigger-less mode, meaning the system does not rely on a trigger signal to initiate operation. Upon detecting an input LVDS signal (NIM-TTL-LVDS), the entire TDC module performs time information measurement. Given that the readout electronics system for the plastic scintillation ToF detectors is expected to operate at a high count rate of 1 MHz, it is crucial for the electronics system to complete data transmission as quickly as possible to prevent TDC data loss caused by slow transmission speed.

Fig. 7 [Figure 7: see original paper] illustrates the transmission process of the TDC data to the DAQ via a USB 3.0 port. After passing through the level conversion board, the LVDS differential signals are sequentially sent to the TDC module for time information measurement. The TDC data from all channels is first individually framed and then stored in a first-in-first-out (FIFO) array. The data readout control module plays a key role in managing the TDC data in the FIFO array and handling clock domain crossing. This module first checks for the presence of TDC data in each FIFO of the array and then reads the TDC time data from different FIFOs.

The function of the data storage FIFO array is, first, to frame and package the coarse-time stamp, fine-time stamp, trigger count, and other related TDC data into the FIFO array. The TDC data is then read out from different channels according to the corresponding control instructions from the backend data transmission module. To minimize time overhead during intermediate data transmission, a data splitting module is incorporated into the design. This module serves two main purposes: aggregating the data and splitting it into 32-bit chunks for continuous transmission to the backend, while simultaneously generating a data valid signal; and avoiding direct data transfers from the high-frequency TDC clock domain to the system’s low-frequency clock domain.

In the data packaging module, the split data from the frontend is aggregated and packaged. This module also performs high-low bits reversal. Finally, the processed TDC data is uploaded to the DAQ server via the USB 3.0 module.

## V. Test Results

We have evaluated the performance of the readout electronics using a pulse generator and plastic scintillation detectors, with the primary assessment metric being the time resolution of each channel.

### A. Calibration of the Delay Line

According to the design of the TDC, the arrival time of the signal to one channel is given by  $t = N_C \cdot T_{clk} - T_F$ , where  $N_C$  represents the number of clock periods  $T_{clk}$  (2 ns in this work), and  $T_F$  is the fine-delay time within one  $T_{clk}$ . From this equation, it is evident that the resolution of the TDC module for sub-nanosecond timing is mainly determined by the precision of the fine-delay time.  $T_F$  is determined by the delay time of each fired delay unit within the FPGA's underlying logic resource, CARRY4. Typically, as the FPGA manufacturing process advances, the delay per unit decreases, thereby enhancing the resolution of the TDC. However, variations in signal propagation times through the carry chain and clock jitter at the edges of the clock distribution network can cause fluctuations in the delay-tap widths [41]. To assess this nonlinearity of the delay chain, we performed code density tests to calibrate the delay time using the bin-by-bin approach [42]. We first obtained the distribution of the firing density ( $d_j$ ) of each delay unit illustrated with the blue line in Fig. 8 [Figure 8: see original paper]. The measured average least significant bit (LSB) is  $2 \text{ ns}/175 = 11.43 \text{ ps}$ , where 175 is the number of TDC's valid bins. The differential nonlinearity (DNL) and integral nonlinearity (INL) of each TDC channel were analyzed. The maximum DNL (ranging from 1.77 LSB to 3.89 LSB) and INL (ranging from 4.93 LSB to 7.67 LSB) of all eight TDC channels are shown in Figs. 9 and 10, respectively. Then the fine-delay time until the  $i$ th unit is calculated by  $T_{F,i} = T_{clk} \cdot \sum$ , as depicted by the red line in Fig. 8. By combining the equations, we can obtain the signal arrival time.

### B. Cross-Talk Evaluation

There are 8 channels in the TDC. To assess the impact of cross-talk (XT) on time resolution, we measured the time resolutions of two channels at various time intervals and different locations.

To assess the impact of XT from various time intervals on time resolution, and given the 100 ns pulse width of the NIM signal post-CFD, we step around the 100 ns interval in 2 ns increments to observe changes in time resolution of channel-1 and channel-2. Note that the rising edge of the stop signal may be influenced by XT from the trailing edge of the NIM signal (an uncorrelated XT effect [43]). The test results, represented by the square markers and black line in Fig. 11 [Figure 11: see original paper], show a time resolution jitter within 10 ps. Specifically, near the most likely XT interval of 100 ns, the jitter is less than 3 ps, indicating minimal impact from XT. To assess the impact of XT on time resolution due to interference from adjacent channels, we injected an interfering

signal generated by a pulse generator into an adjacent channel. Fig. 11 shows that the presence of interference signals in the adjacent channel does not affect the start and stop signals, indicating that multi-channel time resolution remains unaffected by XT.

To assess the impact of XT at different locations on time resolution, we calculated time resolution by positioning TDCs at various locations within the FPGA; the results are presented in Fig. 13 [Figure 13: see original paper]. The 8-channel TDCs are laid out and routed within the FPGA as shown in Fig. 12 [Figure 12: see original paper], with each channel's TDC placed on a different BANK. TDCs located in different positions exhibit a 6-7 ps variation in time resolution. Fig. 12 shows that channel-1 and channel-2 are laid out adjacently, as are channel-7 and channel-8. Fig. 13 indicates that the time resolution for channel-1 and channel-2 is 27.5 ps, while for channel-7 and channel-8 it is 26.4 ps. The time resolution for channel-1 and channel-8 is 32.7 ps, with these variations primarily due to the routing and layout differences of the TDC channels within the FPGA. The impact of XT at different locations on time resolution is negligible.

### C. Test with Pulse Generator

To evaluate the time resolution performance of the ToF detector readout electronics system we designed and to verify whether this system meets the time resolution requirements for the plastic scintillation ToF detectors on the HFRS beamline, we conducted a series of tests. In order to accurately replicate the real signals from plastic scintillation detectors, we utilized Tektronix's ArbExpress software [44] to import the detector signals, which were originally captured by a Tektronix MSO54 oscilloscope. The waveforms were subsequently exported to a Tektronix AFG3252C pulse generator to produce simulated signals with the same shape as the original detector signals, while allowing for adjustable amplitude and frequency. The generated signals were then sent into the CFDs followed by the level converter and TDC board, from which one can obtain the time difference between every two channels. Fig. 14 [Figure 14: see original paper] presents the distribution of the time differences between channel-6 and channel-2. The coincidence time resolution for this channel pair, represented by the FWHM value from the fitted Gaussian function, is measured to be 29.6 ps. The fitting procedure was performed using CERN-ROOT software [45] to obtain the FWHM and its uncertainty (including statistical and fitting errors). Similarly, we obtained the coincidence time resolutions for the other seven pairs of channels as listed in the following equation array:

$$\text{FWHM}_{ch1+ch2}^2 = 27.9^2$$

$$\text{FWHM}_{ch1+ch3}^2 = 28.1^2$$

$$\text{FWHM}_{ch1+ch4}^2 = 30.4^2$$

$$\text{FWHM}_{ch1+ch5}^2 = 29.2^2$$

$$\text{FWHM}_{ch1+ch6}^2 = 29.5^2$$

$$\text{FWHM}_{ch1+ch7}^2 = 32.1^2$$

$$\text{FWHM}_{ch1+ch8}^2 = 32.4^2$$

$$\text{FWHM}_{ch2+ch6}^2 = 29.6^2$$

Subsequently, the time resolution for each individual channel was calculated and is illustrated in Fig. 15 [Figure 15: see original paper], with the average value around 24 ps.

Given that the ToF detectors at the HFRS beamline are expected to operate at a high beam rate of  $10^6$  counts per second (cps), we evaluated the saturation characteristics of the entire readout electronics for the detectors. During the test, the output signal from the pulse generator was split into eight using a power splitter. Eight channels of the readout electronics processed the signals simultaneously, allowing us to assess the performance of the system under high-rate conditions. The pulse generator was configured to provide a fixed number of input signals ( $10^6$  events) with different rates. Then we monitored and recorded the total count of output, with the test results shown in Fig. 16 [Figure 16: see original paper]. It demonstrates that for input frequencies up to  $1.6 \times 10^6$  cps, the readout electronics correctly captured all the events without loss. This validation confirms that the system meets the counting-rate requirements of the HFRS beamline. However, beyond this rate, the system exhibited a progressive inability to record all the input events, indicating the onset of saturation. These results confirm that the readout electronics are capable of meeting the required count rate of the plastic scintillation ToF detectors at the HFRS beamline.

#### D. Test with Plastic Scintillation Detectors

To further evaluate the performance of the readout electronics for the plastic scintillation ToF detectors, we conducted a joint test, as shown in Fig. 17 [Figure 17: see original paper]. It is a joint test setup and detector diagram and shows the connection correspondence between the large and small plastic scintillator PMTs and the electronics readout channel. A PiL1-037-40 picosecond pulsed diode laser from NKT Photonics [46] served as the beam source, which can emit laser pulses at a wavelength of 375 nm with a repetition rate of up to 40 MHz. Each scintillation detector is composed of one thin plastic scintillator coupled to four photomultiplier tubes (PMTs). One scintillator is EJ-228 from Eljen Technology with a smaller size of  $70 \text{ mm} \times 70 \text{ mm} \times 0.5 \text{ mm}$ , while the other is EJ –

230 with a larger size of  $260\text{mm} \times 100\text{mm} \times 1\text{mm}$ . The PMTs are H6533 assemblies from Hamamatsu Photonics [47]. For detailed information on the EJ-228/230 plastic scintillators and H6533 PMTs, one can refer to their official website and Ref. [18].

The system was tested at laser repetition rates of 10 kHz and 1 MHz. Signals from eight PMTs of the detectors were transmitted to our developed readout electronics, with the first four channels connected to the smaller plastic scintillation detector and the remaining four channels connected to the larger one. In addition, the output signals from the Model-935 CFD were fed into the commercial Mesytec MTDC32 module [48] to benchmark the designed TDC. The test results are summarized in Table 3. The average time resolution of all the PMT pairs was 39.4 ps when using the TDC developed in this work, compared to 46.1 ps with the Mesytec MTDC32.

At the laser rate of 1 MHz, the MTDC32 was able to record only 200 kcps when using the Wiener VM-USB VME controller with USB-2 interface [49], and 700 kcps when using the Mesytec MVLC controller with USB-3 interface [50]. In contrast, our designed TDC was capable of recording all counts without loss and achieved an average time resolution of approximately 42 ps for all PMT pairs. The comparison of time distributions for each PMT pair is displayed in Fig. 18 [Figure 18: see original paper].

The commercial electronics system is bulky and unsuitable for large-scale integration. The electronics we designed not only meet the metrics but also offer significant advantages in terms of power consumption and compactness, making them more suitable for large-scale deployment and scaling.

Furthermore, we calculated the time-of-flight between two plastic scintillation detectors with:

$$\text{ToF} = \frac{t_{b1} + t_{b2} + t_{b3} + t_{b4}}{t_{a1} + t_{a2} + t_{a3} + t_{a4}} \quad (4)$$

where  $t_{ai}$  and  $t_{bi}$  denote the arrival times of the PMTs corresponding to the small and larger plastic scintillators, respectively. Fig. 18 shows the ToF distribution measured at a laser repetition rate of 1 MHz. The FWHM value is 24.3 ps, indicating the system amply satisfies the requirements for the ToF resolution (below 94 ps for FWHM) of the HFRS beamline operating at high beam intensity.

## VI. Conclusion

This study utilizes a high-precision pulse generator and pulsed laser to evaluate the time resolution and counting rate performance of a prototype readout electronics for the plastic scintillation ToF detectors of the HIAF-HFRS facility. The system comprises a constant-fraction discriminator, a logic level conversion board, and a time digitization board.

An 8-channel time resolution test and a maximum counting rate evaluation were conducted using the prototype. Based on the results from the high-precision pulse generator, the time resolution of each individual channel of the electronic system we designed is around 24 ps, with a single channel capable of handling a maximum counting rate of  $1.6 \times 10^6$  cps. According to the test results with pulsed laser, which can be used to simulate the actual ion beam, our designed circuit system demonstrates time resolution performance comparable to that of the commercial Mesytec-MTDC32 electronics system. The time resolution of our readout system is better than 42 ps for all the PMT pairs. Under high counting rate testing at 1 MHz using laser, the readout system still exhibits excellent performance, with average time resolution of approximately 42 ps for all the PMT pairs. Based on the test results using both the pulse generator and the laser, the performance of the readout electronics meets the requirements of the HFRS beamline for ToF resolution and counting rate.

Next, we will develop and design a constant fraction timing discriminator board to replace the existing ORTEC 935 discriminator in the readout system, aiming to fully achieve an independent design for this system. We plan to re-design the TDC board to integrate 16 readout channels into this system, synchronizing and optimizing the back-end data transmission links, with the goal of developing a system with better time resolution and counting rate for the ToF detectors. Ultimately, after upgrading the readout electronics system, we intend to conduct heavy-ion beam experiments at the HIRFL-RIBLL2 and HIAF-HFRS beamlines to test its time performance and counting rate metrics.

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