# Low Leakage Switch Technology for Ion Signal Detection for N DEx

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## Abstract

The detection of neutrinoless double-$\beta$ decay ($0\,\beta\beta$) holds profound implications for determining the Majorana nature of neutrinos and probing beyond the Standard Model physics. This study focuses on the critical challenge of weak signal detection in high-pressure gas time projection chambers (TPCs) in N DEx, where the ion drift velocity in high-pressure $SeF_6$ gas necessitates extending the detector' s recovery time to prolong its sensitive window for signal acquisition. We present the integration of a Low Leakage Switch (LLS) with the TopMetal CMOS sensor, designed to mitigate recovery currents and enhance slow-signal detection capabilities. The LLS employs Vds-regulated switches to minimize leakage to sub-0.6 fA levels, extending the time constant to several tens of seconds–surpassing prior limits by one order of magnitude of TopMetal-S. Experimental validation demonstrates the effective ion detection capability in the atmospheric environment by leveraging a microfocus X-ray source and a low leakage switch array. In a proper design, the LLS primarily introduces noise outside the signal frequency to the charge measurement system. The results highlight the LLS-TopMetal integration as a transformative approach for next-generation Ion detectors.

## Full Text

## Preamble

Low Leakage Switch Technology for Ion Signal Detection for N DEx∗

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The detection of neutrinoless double-$\beta$ decay (0 $\beta\beta$) holds profound implications for determining the Majorana nature of neutrinos and probing beyond the Standard Model physics. This study focuses on the critical challenge of weak signal detection in high-pressure gas time projection chambers (TPCs) in N DEx, where the ion drift velocity in high-pressure SeF6 gas necessitates extending the detector' s recovery time to prolong its sensitive window for signal acquisition. We present the integration of a Low Leakage Switch (LLS) with the TopMetal CMOS sensor, designed to mitigate recovery currents and enhance slow-signal detection capabilities.

The LLS employs Vds-regulated switches to minimize leakage to sub-0.6 fA levels, extending the time constant to several tens of seconds–surpassing prior limits by one order of magnitude of TopMetal-S. Experimental validation demonstrates the effective ion detection capability in the atmospheric environment by leveraging a microfocus X-ray source and a low leakage switch array. In a proper design, the LLS primarily introduces noise outside the signal frequency to the charge measurement system. The results highlight the LLS-TopMetal integration as a transformative approach for next-generation ion detectors.

Keywords: neutrinoless double-beta decay, CMOS sensor, time projection chamber (TPC), Low Leakage CMOS Switches

## INTRODUCTION

The Standard Model (SM) of particle physics serves as a cornerstone of modern physics, yet it fails to explain neutrino oscillations, which indicate neutrinos possess non-zero mass beyond the SM framework. Whether neutrinos are Dirac or Majorana fermions remains one of the most pivotal questions in contemporary particle physics. The detection of neutrinoless double-$\beta$ decay (0 $\beta\beta$) represents a critical avenue to resolve these issues. Observation of 0 $\beta\beta$ decay would confirm the Majorana nature of neutrinos, provide direct insights into neutrino mass generation, and potentially elucidate the matter-antimatter asymmetry in the universe, thereby unveiling new physics beyond the SM.

Numerous international experiments have been dedicated to searching for 0 $\beta\beta$ decay through diverse technological approaches and isotopes, including GERDA [1], MAJORANA [2], CUORE [3], CUPID [4], KamLAND-Zen [5], and EXO [6].

In China, experiments such as CDEX [7], PandaX [8], CUPID-China [9], and JUNO [10] are operational or under development to probe 0 $\beta\beta$ decay. While these experiments employ distinct methodologies, they universally confront challenges in background suppression and signal readout. Although 0 $\beta\beta$ decay

remains unobserved to date, these efforts have laid a crucial foundation for next-generation experiments.

A high-pressure gas time projection chamber (TPC) using 82SeF6 as the working medium was first proposed by Dr. R. Nygren and others to detect neutrinoless double-$\beta$ decay [11]. This is because the high double-$\beta$ decay energy value (Q$\beta\beta$) of 82SeF6 (2.996 MeV) positions its signal region well above most natural radioactive backgrounds. The gas TPC enables reconstruction of the two-electron trajectories from double-$\beta$ decay events, leveraging their unique topological features for effective signal-background discrimination. This TPC was constructed and used in the Neutrinoless Double-$\beta$ Decay Experiment (N DEx) [12]. Furthermore, N DEx benefits from the ultra-low background environment of the China Jinping Underground Laboratory (CJPL) [13], significantly suppressing experimental backgrounds. Building on this concept, N DEx-100 is currently under development [14], with detector installation at CJPL scheduled for completion in 2025.

However, the strong electronegativity of 82SeF6 causes rapid attachment of ionization electrons to gas molecules, precluding detection of weak signals via conventional electron avalanche amplification. To address this challenge, a CMOS sensor, named TopMetal-S, was developed to directly collect ions, achieving a noise floor as low as 114 e− [15]. The first-generation TopMetal-S charge-sensitive amplifier (CSA) features a millisecond-level RC time constant [16], while the second-generation TopMetal-S sensor has achieved an RC time constant of 1.5 seconds [17].

In the detectors currently used for N DEx, simulations indicate that the ion drift speed is significantly slower than that of electrons, with the average arrival time spread for a single ion species being 36 ms, and the maximum reaching approximately 300 ms (Fig. 1 [Figure 1: see original paper]). When the signal rise time approaches its decay time, the performance of the detector degrades. Based on this, at least a signal attenuation time of several seconds is required, or the feedback resistor should be removed and the switch reset method should be adopted [18]. The feedback resistor in TopMetal-S is implemented through a near-cutoff MOS design, achieving a resistance in the gigaohm range with a leakage current of approximately 100 femtoamps.

Since this resistance value is close to the manufacturing limits of industrial CMOS processes and the leakage current approaches the analog boundary, it has become difficult to further increase the detector' s RC constant using traditional methods. In solutions that utilize the switch reset method instead of resistors, the switch itself must exhibit extremely high impedance. This approach, along with the large RC constant method, ultimately converges on the issue of leakage current suppression. Therefore, investigating the suppression of leakage current in on-chip MOS switches is critically important, and developing an innovative current bleeding architecture is essential. We developed the Low Leakage Switch (LLS), and successfully integrated the LLS with TopMetal. This integration transformed TopMetal into a low-leakage node capable of long-

duration, high-precision detection. It is important to note that investigating the noise contribution of the LLS to the low-noise CSA is necessary for this research. Therefore, in Section IV, we discuss the impact of LLS on the low-noise CSA and verify the noise contribution of this structure through simulations. This technology is expected to be applied to next-generation TopMetal-S detectors, extending the RC time constants to several tens of seconds.

## II. DESIGN OF THE DETECTOR

### A. Vds-regulated switches

The current leakage issue is directly related to the leakage current of CMOS switches. A positive aspect is that we have substantial engineering experience for reference. In nearly all circuits, CMOS switches serve as critical circuit modules, participating extensively in sampling [19], channel multiplexing [20], dynamic element matching [21], chopping operations [22], etc. Therefore, high-performance low-leakage switches are essential for superior system performance. Fig. 2 illustrates the basic structure of a PMOS (P-type Metal-Oxide-Semiconductor Field-Effect Transistor) and the key components of its leakage model. The PMOS comprises the following fundamental structures: The substrate is N-doped silicon serving as the device base, typically connected to the highest circuit potential (e.g., VDD) to maintain reverse bias. The source (S) and drain (D) are P+ heavily doped regions formed on the substrate, acting as the injection and outflow terminals for carriers (holes). The source is usually connected to a high potential (e.g., VDD), while the drain connects to the load or low potential. The gate (G) consists of a gate oxide layer and gate electrode. The gate oxide is an ultra-thin silicon dioxide (SiO2) insulating layer above the substrate, isolating the gate from the substrate. The gate electrode, made of polysilicon or metal, covers the oxide layer and controls channel conduction via applied voltage [23].

Fig. 2 also reveals four primary leakage current sources in CMOS switches: Ipn: parasitic diode leakage, Ib: gate-induced drain leakage, Ig: gate direct tunneling leakage, and Ic: subthreshold leakage. In CMOS processes, the gate direct tunneling leakage (Ig) can be neglected in practical analysis due to the insulating oxide layer. The remaining components are described by the following equations:

Ipn = Is ⋅ n T − 1 Ib = I(Vds, Vgd, $V^3$) Ic = Iconst(Vgs−Vth) ⋅ e^( Vds/n T) ⋅ (1 − e^(−Vds))

where Is is a function related to the MOS transistor' s dimensions, process, and temperature, n is the subthreshold swing coefficient, T is a temperature-dependent function, and Ib has a complex relationship with Vds, Vgd, and $V^3$sb, but we can at least reduce Ib by decreasing $V^3$sb [24], Iconst = 100 nA (used to define the transistor' s threshold voltage) [25], is the model parameter of the source-side MOS transistor. Ipn can be reduced by decreasing Vsb, and the same applies to Ib. Ic can be reduced by lowering Vth and Vds, while increas-

ing Vgs. To suppress switch leakage and nonlinearity, various strategies have been proposed including bootstrapped switches [26], using low-Vth MOS devices, adaptive body biasing [27], Vds-regulated switches [28], and leakage compensation techniques [29]. Among these approaches, bootstrapped switches, low-Vth MOS devices, and dynamic substrate biasing demonstrate limited effectiveness in leakage reduction, while leakage injection methods introduce excessive complexity and potential noise risks. Currently, Vds-regulated switches represent the most effective solution for leakage current suppression.

Fig. 3 shows a typical Vds-regulated switches configuration, where a capacitor is used to store the signal voltage Vsignal, two MOS transistors form a transmission gate (TG) switch, the operational amplifier (OPA) is configured as a high-gain amplifier in unity-gain connection, with two additional TG switches for selecting whether to regulate Vds.  and  are complementary control signals. When  is low, TG1 and TG3 are simultaneously turned on while TG2 is turned off, allowing Vsignal = Vin to be received by the capacitor. When  is high, TG2 is turned on while TG1 and TG3 are simultaneously turned off, maintaining similar voltages across TG1 and preserving Vsignal for extended periods. The devices with the most significant impact on Vsignal are the two adjacent MOS transistors (TG1). As the capacitor is directly connected to their source terminals, stored charge leaks through these transistors. The typical Vds-regulated switches configuration integrates a TG with an analog buffer to minimize Vds to near-zero levels, thereby reducing leakage currents to approximately 100 fA [28].

### B. Integration of LLS with TopMetal

The fundamental theory of Vds-regulated switches is discussed in the previous section. Below, we will explore how to integrate these principles with the detector design. In our earlier developed TopMetal series of integrated circuit detector chips [30–36], the design of the charge-collection electrode (TopMetal node) has been successfully verified for direct spatial electron collection. If the TopMetal node can be a low-leakage node, the influence of internal circuits on its voltage signal will be minimized, leaving it determined solely by external signal charges. However, the TopMetal node cannot be left as an absolute floating node, as its voltage becomes uncontrollable due to the lack of a defined reference potential. Therefore, the TopMetal node requires a switch to reset its voltage to a reference potential, which is implemented using Vds-regulated switches.

In practice, if a single MOS transistor can function as a switch, the substrate and drain of a single PMOS switch are shorted, its Vth will decrease, thereby reducing leakage currents. This Vds-regulated switch, where the transmission gate (TG) is replaced with a PMOS, is abbreviated as LLS in this work.

Fig. 4 illustrates the single-pixel schematic with the following key components: The TopMetal is the metal layer featuring a top-side charge-collection window for external ionization charge reception. The LLS is a PMOS switching circuit

with a clamping buffer, controlled by complementary digital signals and for TopMetal reset and low-leakage node configuration. The Comparator & High-Pass Filter is the control loop generating the signal to compensate for leakage currents. The Two-Stage Source Follower (SF) is a dual-buffered analog readout chain with low-noise characteristics. Additionally, a counter is designed to track reset events for handling large signal inputs, and an RST signal is included for external system reset control. The input signals ROW_{SEL} and ROW_{SEL} are complementary control signals for serial readout. The OUT signal and CNT[13:0] signals represent the analog and digital outputs to be read. The OPA in the LLS structure is a core component, as shown in Fig. 4. To achieve superior voltage-following characteristics, this module is designed using negative feedback techniques, providing extremely high open-loop gain (Av $>$ 75 dB) and sufficient phase margin (PM $\geq 60°$). A limitation of the LLS lies in its inability to conduct low-voltage signals during activation, though this constraint proves inconsequential in our design as rail-to-rail signal transmission is not required.

Given the empirically reported sub-femtoampere leakage levels for Vds-regulated switches, experimental validation through practical testing remains imperative to confirm these specifications.

During system initialization, RST is set to a low logic level, externally forcing the digital signal to zero. This shorts the TopMetal node to Vreset and establishes the reset state. When transitions to a high logic level, the LLS activates and the system enters the measurement state. The TopMetal operates as a low-leakage node, with its potential varying according to collected external charges. When the TopMetal voltage crosses the Vref threshold, the comparator outputs a digital step signal. This signal is converted into a pulse-width modulated signal through the high-pass filter, triggering an automatic reset cycle that discharges accumulated charges via digital control. Post-discharge, the system re-enters the measurement state with the TopMetal restored as a low-leakage node. Fig. 4 shows the waveforms of Vsignal and during TopMetal' s reception of negative charge ions. When is logic 0, Vsignal is reset to Vreset. The typical value of the detection dead time caused by resetting is 10 ns. When is logic 1, the TopMetal begins collecting negative charge ions, causing its voltage to gradually decrease. Vsignal triggers to transition back to logic 0 once it crosses Vref.

### C. Simulation

Fig. 5 [Figure 5: see original paper] shows simulation results. We use the transient analysis of SPECTRE [37] to simulate our circuit. The solution at a specific point in transient analysis heavily depends on the solution from the previous step. Consequently, errors propagate from one step to the next, making the pattern of error propagation crucial. However, whether errors shrink or amplify is determined solely by the circuit itself rather than the simulator, meaning absolute high precision cannot be guaranteed through simulator settings.

Truncation errors arise from approximating time derivatives with discrete-time equivalents.

It is useful to separately consider: Local Truncation Error (LTE), the truncation error generated in a single step under the assumption that all previous steps are accurate; Global Truncation Error (GTE), the maximum accumulated truncation error, influenced by both LTE at each step and the circuit' s tendency to accumulate or dissipate errors. The most critical factor determining GTE is the circuit' s propensity to accumulate errors. Circuits particularly sensitive to simulator errors include those with long time constants: charge storage circuits (e.g., switched-capacitor circuits, dynamic memories), chaotic circuits (e.g., oversampling analog-to-digital converters), autonomous circuits (e.g., oscillators). Notably, our dynamic charge storage circuit with high time constants falls precisely into the category where simulator errors fail to dissipate.

SPECTRE provides the following parameters to enhance simulation precision: -reltol: Global precision control (range: 0–1). Lower values indicate higher precision. Directly affects Newton convergence criteria and time-step control. Defines error limits relative to signal magnitudes. Reducing reltol decreases errors but offers no absolute guarantees. -vabstol: Voltage absolute tolerance. Specifies the minimum meaningful voltage; values below this threshold are ignored during convergence checks and time-step selection. -iabstol: Current absolute tolerance. Specifies the minimum meaningful current; values below this threshold are similarly ignored.

Excessively loose tolerance settings degrade precision, while overly stringent settings may prevent simulator convergence. The integration methods used in circuit simulation are taken from a general class of methods called multistep methods. Specifically, the Spectre simulator employs three distinct integration techniques: the backward-Euler method, the trapezoidal rule, and the second-order Gear method. The integration method can be specified using the method parameter, which offers six possible configurations to enable different combinations of these three methods. The allowable settings and their corresponding integration methods are detailed in Table 1 .

**Table 1: Integration Method Settings and Allowed Methods**

| Method | Integration Technique |
|---|---|
| euler | Backward Euler |
| traponly | Trapezoidal |
| gear2only | Second-Order Gear |
| gear2 | Second-Order Gear |
| trapear2 | Trapezoidal |
| gear2_{presim} | Second-Order Gear |

The simulation parameters are configured with reltol set to $1 \times 10^{-4}$, iabstol to $1 \times 10^{-15}$ A, and vabstol to $1 \times 10^{-5}$ V. The voltage thresholds are defined

with Vreset at 0.9 V and Vref at 0.5 V, at a temperature of 22°C. Higher precision settings failed to converge in our circuit design. Simulation results obtained using different algorithms are displayed in Fig. 5, where the red curve represents transistor-level simulation results (pre-simulation), and other curves correspond to layout simulation results (post-simulation).

The pre-simulation indicates that the TopMetal node voltage drifts toward the supply voltage with a leakage current of approximately 12 fA, whereas post-simulation shows the TopMetal node voltage drifting toward 0 V potential, even triggering automatic reset, with a leakage current of about 70 fA. The discrepancy between pre-simulation and post-simulation suggests that the layout impacts leakage current. Although post-simulation results from different algorithms exhibit minor variations, the leakage current already approaches the Iabstol threshold. Considering the continuous accumulation of errors during simulation, the accuracy of these results remains questionable. However, the clear suppression effect of LLS on leakage currents warrants proceeding with tape-out for further investigation.

### D. Pixel Array

To address the inter-pixel uniformity issue, we implemented several methods. The circuit design, layout, and physical dimensions of each type of pixel cell were designed to be fully consistent. Additionally, to ensure environmental uniformity between pixels, we used a dummy pixel technique to guarantee that edge pixels exhibit the same parasitic parameters as interior pixels. The conventional pixel array design concept employs row/column selection switches combined with shared source followers and tail current sources to form the basic serial pixel-by-pixel readout structure [20]. Our pixel array implements this architecture. To maximize integration density, the SCAN Module exclusively receives external digital control signals (CLK, RST, SPEAK, START) to generate serial readout control signals (ROW_{SEL}, COL_{SEL}). The entire chip is synchronized by the clock signal CLK (Fig. 6 [Figure 6: see original paper]).

The chip' s overall architecture, shown in Fig. 7a [Figure 7: see original paper], comprises: a 24$\times$38$pixelarraywith$300$m\times$$259.8 µm pixel pitch and 150 µm staggered column layout; the SCAN Module, which initiates scanning after RST = 0 is maintained for 7 clock cycles, followed by setting SPEAK = 1. The START signal is pulled high for 1 clock cycle to activate scanning within the next 2 clock cycles. The scan can be restarted at any time by asserting START = 1, or paused by pulling SPEAK low, enabling flexible and efficient array control. The SCAN Module also outputs the MARKER signal, a frame marker that transitions high when scanning reaches the pixel at coordinates (1,1). Current mirrors provide current drive for the source follower structures. Fabricated in the TSMC 180nm CMOS process, the chip micrograph is shown in Fig. 7b.

# III. EXPERIMENTAL VERIFICATION

## A. Experimental Setup

Figure 8 [Figure 8: see original paper] depicts the readout system architecture comprising five primary sections. Section A corresponds to the field cage assembly integrated with a CMOS sensor, while Section B constitutes the data conversion stage. Analog signals from the chip enter the readout system and are first buffered through the AD8062 [38] module to enhance driving capability. The buffered analog signal is then converted into differential pairs via the THS4521 [39], followed by digitization using the AD9629 [40] (12-bit analog-to-digital converter) operating at 40 MSPS (Million Samples Per Second). Analog supply signals for the chip are generated by the DA8568 [41] digital-to-analog converter (DAC). Section C implements the digital processing core through an AMD Kintex-7 FPGA (field-programmable gate array) KC705 [42], handling computational tasks and PC communication. Section D provides signal conditioning circuitry with level adaptation for interface compatibility, and Section E integrates a dedicated power management unit delivering regulated system voltages. Digital and analog signal streams from the chip converge at the FPGA for buffering in DDR3 memory and system integration, ultimately being transferred via Ethernet interface to a host computer for comprehensive data analysis.

Notably, as the chip readout speed is configured at 2 MSPS (significantly lower than the ADC' s 40 MSPS sampling rate), the firmware implements clock synchronization and oversampling techniques for both digital and analog outputs. Invalid data packets are filtered prior to PC transmission.

The analog signals received at the PC originate from the chip' s analog output channels, but require specialized decoding. The ADC output employs offset binary coding, necessitating software-based decoding with specific bit-shifting algorithms. More critically, the physical signal of interest—the TopMetal node voltage reflecting external charge quantity—is not directly measurable. A two-stage source follower circuit between the TopMetal node and chip output introduces a non-linear mapping relationship, despite its ultra-low noise characteristics. Therefore, raw data acquired through the ADC and FPGA require calibration to reconstruct true physical quantities. The DA8568 DAC, being a mature commercial IC, is assumed to provide precise reference voltages. Calibration involves: (1) resetting the TopMetal node to a known DA8568-generated voltage baseline, (2) operating the TopMetal chip in single-pixel mode, and (3) acquiring 500 consecutive analog output samples through the readout board. Averaging these measurements filters high-frequency noise, establishing discrete mapping points of the two-stage source follower. Although the DA8568 was configured with 1 mV resolution across 0.4-1.2 V, the resultant calibration remains discrete. Linear interpolation algorithms were subsequently applied to generate continuous mapping functions for analytical purposes. The entire test system control and data analysis pipeline was implemented through Python 3.9.

### B. Chip Functional Verification

We will utilize the chip to continuously collect ion signals in the air under operating conditions, so as to demonstrate the functional verification of the chip and prove that the LLS-enhanced TopMetal maintains effective detection capability for ions in ambient air. The fundamental physical principle of this experiment is that X-rays emitted from a microfocus X-ray source (MFX) at appropriate energy levels can ionize air. The ionized air molecules are directly collected by TopMetal under the electric field of the field cage. The charges are converted into voltage signals within the chip and transmitted to the PC through the signal chain shown in Section III A for analysis.

Creating slits on the lead plate produces significantly non-uniform charged particle distributions in space, resulting in characteristic voltage patterns on the pixel CMOS sensor. The MFX is manufactured by Hamamatsu, with the model number L14351-02. Its X-ray generation mechanism is as follows: electrons emitted from the cathode are accelerated by the electric field between the cathode and anode to form high-speed electrons. When these high-speed electrons collide with target atoms, their trajectories are altered, causing deceleration and emission of X-rays with energy equal to the energy difference before and after the collision. Thus, X-ray characteristics are controlled by two parameters: tube voltage and tube current. Higher tube voltage produces X-rays with greater energy, shorter wavelengths, and stronger material penetration capability. Higher tube current increases the number of high-speed electrons striking the target per unit time, equivalent to enhancing the X-ray dose over a given area. The complete experimental setup is shown in Fig. 9a [Figure 9: see original paper].

To balance penetration capability and X-ray dose, the MFX was configured at 50 kV and 300 µA, with the Focus Mode set to “large”. The slitted lead plate and protective box are displayed in Fig. 9b, with the slit positioned at the center of the pixel array. The field cage parameters shown in Fig. 9c were obtained from COMSOL [43] electrostatic field simulations, with the figure also indicating the X-ray incidence direction and detector array placement. The field cage consists of five copper rings (1 mm thickness, 6 mm length, 300 mm outer diameter) arranged with 8.42 mm center spacing, with the top layer covered by copper foil. The voltage of the top layer is -1500 V, and the voltage divider resistor is approximately 25 MΩ. In the figure, surface distribution shows the absolute value of the magnitude of the electric field, streamlines indicate field direction, and contours represent equipotential surfaces.

Continuous 1.04 s measurements revealed enhanced charged particle signals along the central y-axis of the pixels, as shown in Fig. 10a [Figure 10: see original paper]. Background signals were acquired without field cage bias voltage, and the 2D plot results were obtained after subtracting this background and calculating the accumulated voltage over 1.04 s. The integration process for a single pixel is visually demonstrated in Fig. 10b, consistent with theoretical predictions from the schematic in Fig. 4. This demonstrates that the LLS-enhanced

TopMetal maintains effective detection capability for ions in ambient air. In the N DEx high-pressure gas time projection chamber, the exceptionally slow ion drift velocity necessitates extended signal integration. The implemented LLS achieves a 32.961 s time constant, significantly enhancing slow-signal detection capability.

### C. Leakage Current Characterization

Under atmospheric conditions at room temperature (22°C), the TopMetal node was initialized to 0.9 V, with the output voltages of the two-stage source follower sampled at 2-second intervals during a 100-second continuous monitoring period. This experimental configuration generated the operational stability characteristics presented in Fig. 11 [Figure 11: see original paper], where Pixel 1 (Row 13, Column 21) and Pixel 2 (Row 13, Column 20) are centrally located in the array (see Fig. 7). Due to the difference in the positions of Pixel 1 and Pixel 2 in the chip, their initial voltages vary. A dual Y-axis was used to plot the upper part of this graph to prevent this variation from affecting the display of signal details in the image. The upper panel displays temporal voltage decay profiles following reset operations, while the lower panel shows calculated leakage current magnitudes derived from voltage derivatives. The asterisks located over the top graph curves in Fig. 11 denote the time constant obtained through exponential fitting of the decay profiles using:

$V(t) = V_0 e\hat{}(-t/\tau) + Vb$

yielding time constants of 41.230 ± 4.134 s ($3\sigma$) for Pixel 1 and 32.961 ± 3.309 s ($3\sigma$) for Pixel 2, with coefficients of determination $R^2 = 1.0121$ and 1.0014 respectively. Leakage currents were computed via:

$Ileak = Cnode \cdot \Delta V$

where Cnode = 183 fF (extracted from Calibre PEX simulations). The lower panel confirms sub-0.6 fA leakage levels at the low-leakage node, demonstrating relatively small circuit variations induced by layout dependencies. This also demonstrates that there are significant discrepancies between the real test results and simulation results.

## IV. THE IMPACT OF LLS ON LOW-NOISE CHARGE-SENSITIVE AMPLIFIER

Since noise is an extremely critical metric for N DEx, this chapter will discuss the impact of LLS on low-noise CSA (Charge-Sensitive Amplifier) systems based on the TSMC 180nm process using the SPECTRE simulator. As LLS is an active device, different CSA architectures employ distinct LLS implementations for LLS-CSA systems. This section introduces an LLS-CSA system based on a low-noise CSA [44], and examines how LLS influences the performance of low-noise CSAs.

A simple LLS-CSA system is shown in Fig. 12 [Figure 12: see original paper]. A typical CSA consists of OPA1, capacitors, and a current discharge path formed by M1 and M2. OPA2 generates $V_0$ through a unity-gain feedback loop. Since OPA1 and OPA2 are identical, $V_0$ represents the CSA baseline voltage. $V_0$ controls the voltage at node O through the controlled MOS transistor M3. When M3 is turned on, the source and drain voltages of M1 become similar, causing M1 and OPA2 to function as LLS and making the TopMetal a low-leakage node.

We injected 2000 electrons into the system within 1 ms to observe the system response, and the simulation results are presented in Table 2 . The results show that the CSA-LLS system exhibits an improvement in Amplitude compared to the CSA itself, indicating more complete charge collection by the TopMetal, while the RC time constant is increased by approximately four orders of magnitude. The ENC (Equivalent Noise Charge) of the CSA alone is as low as 29 $e^-$, but after incorporating the LLS, the noise increases significantly to 487 $e^-$, with OPA1 and OPA2 each contributing about 50% of the total noise. The ENC is given by ENC = N × Vrms/Amplitude [44], where the noise voltage Vrms is obtained by integrating the noise power spectral density over the frequency range from 1 mHz to 10 GHz, N is the number of injected charges, and Amplitude refers to the signal magnitude at the output (OUT). Simulations reveal that the primary reason for OPA1' s noise contribution is the degradation in noise performance due to changes in its loop state, while OPA2 introduces low-frequency noise into the TopMetal node through the high-impedance switch M1. This low-frequency noise is then amplified by OPA1 and affects the system measurements. The frequency domain distribution of the noise is shown in Fig. 13 [Figure 13: see original paper].

Compared to the CSA, the CSA-LLS system exhibits a significant amount of low-frequency noise. Since the ion injection duration ranges from 1 ms to 300 ms, we constructed a CRRC (CR-RC) filter module using noiseless ideal components to perform band-pass filtering targeting the frequency range of approximately 1 Hz to 1 kHz. As shown in Fig. 13, noise outside the target frequency range is effectively filtered out in the CSA-LLS-CRRC system. Table 2 demonstrates that this system achieves an ENC as low as 39 $e^-$, and the noise contributed by OPA2 is effectively eliminated, which means the noise introduced by LLS lies outside the signal frequency range.

To demonstrate the advantages of the LLS structure, 2000 electrons were injected into the system over a duration ranging from 1 ms to 300 ms to observe the system response. Simulation results reveal that due to the RC time constant of the CSA being approximately 7.90 ms, its response amplitude (Fig. 14 [Figure 14: see original paper]) decreases rapidly as the injection duration increases. In contrast, the response amplitude of the CSA-LLS system remains relatively stable throughout the 300 ms injection period. As the signal frequency decreases with longer injection durations, the CRRC filtering system used in this study attenuates the response amplitude. The variation of the ENC with injection duration for each system is illustrated in Fig. 15 [Figure 15: see original paper].

The ENC of the CSA system increases significantly due to the reduction in response amplitude, whereas the ENC of the CSA-LLS system remains relatively stable owing to its consistent amplitude. The ENC of the CSA-LLS-CRRC system increases from 39 $e^-$ to 52 $e^-$.

The LLS structure significantly increases the RC time constant of the CSA, but it also leads to a degradation in system noise performance. This deterioration can be attributed to two main factors: the increased loop impedance of the CSA affects the noise performance of the OPA, and the LLS directly introduces additional noise into the low-leakage node, with such additional noise lying outside the signal frequency range. To address these issues, potential solutions include optimizing the noise performance of the OPA under the target loop conditions and designing high-performance filtering circuits. These measures are expected to enhance the RC time constant while maintaining low noise performance in the system. We plan to conduct more detailed studies on this approach and aim to carry out practical experimental validation in the future.

## V. SUMMARY

This study successfully integrates the Low Leakage Switch with TopMetal, establishing the latter as a low-leakage node that significantly enhances slow particle detection capability. In Section II, we analyze the theory of low-leakage switches and confirm that Vds-regulated switches are the most suitable technology to be implemented for ion detection. The simulation of LLS demonstrates that this technique has the potential to effectively suppress leakage current, but SPECTRE cannot accurately quantify this capability. Leakage current measurements demonstrate that the TopMetal-LLS combination achieves a time constant not lower than $32.961 \pm 3.309(3\sigma)$ seconds, whereas the second-generation TopMetal-S exhibits a maximum RC time constant of approximately 1.5 s. Ion detection experiments verify that the LLS-enhanced TopMetal maintains effective detection capability for ions in ambient air. In the conceptual design presented in Section IV, the LLS primarily introduces noise outside the signal frequency to the low-noise CSA system. In future research, the LLS will be considered for application in N DEx to detect slow-moving ions within high-pressure TPCs for track reconstruction.

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