Hardware Design of FPGA-Based Simulated Nuclear Signal Generator

Authors: Yang Yao, Li Xiaohui, Fan Hui, Huang Huan, Li Daowu, Wei Long, Wei Long

Date: 2025-09-09T09:55:51+00:00

Abstract

To address the problems of radiation exposure risk and limited experimental flexibility inherent in traditional nuclear experiments that depend on radioactive sources, this study designs a high-safety analog nuclear signal generator based on an FPGA (Field Programmable Gate Array) and DAC (digital-to-analog converter) architecture. This device generates nuclear signals conforming to Poisson distribution and energy spectrum distribution through an all-digital hardware solution, supporting custom waveform simulation and pile-up effect emulation. The hardware system adopts a layered design: the digital board uses a Xilinx Kintex-7 FPGA as its core, integrating Flash firmware storage, USB 3.0 protocol communication, SPI touchscreen control, and precision clock management modules; the analog board is equipped with a dual-channel AD9764 DAC and high-speed ADC, achieving 12-bit resolution, 125 MSPS signal output, and real waveform acquisition functionality. This design achieves hardware integration of dual-channel independent output, touchscreen control, and networked debugging functionality, providing a zero-radiation-risk experimental platform for nuclear detector calibration and nuclear imaging electronics design, which is of significant importance for enhancing safety in nuclear technology applications.

Full Text

Hardware Design of an FPGA-Based Nuclear Signal Generator

Yao Yang,[1,3,4] Xiaohui Li,[1,3,4] Fanhui Meng,[1,3,4] Huan Huang,[1,3,4] Daowu Li,[1,3,4] Long Wei[1,2,3,4]*
*Corresponding author, weil@ihep.ac.cn

[1]Beijing Engineering Research Center of Radiographic Techniques and Equipment, Institute of High Energy Physics, Chinese Academy of Sciences, Beijing

100049, China
[2]School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing 100049, China
[3]CAEA Center of Excellence on Nuclear Technology Applications for Nuclear Detection and Imaging, Beijing 100049, China

Abstract

Traditional nuclear experiments relying on radioactive sources face risks of radiation exposure and limited experimental flexibility. To address these issues, this study presents a highly safe FPGA (Field Programmable Gate Array) and DAC (Digital-to-Analog Converter)-based nuclear signal generator. The device employs an all-digital hardware solution to generate nuclear signals conforming to Poisson distribution and energy spectrum distribution, supporting customizable waveform simulation and pile-up effects emulation. The hardware system adopts a layered design: Digital board: Centered on a Xilinx Kintex-7 FPGA, integrating Flash firmware storage, USB 3.0 protocol communication, SPI touchscreen control, and precision clock management. Analog board: Equipped with dual-channel AD9764 DAC and high-speed ADC, achieving 12-bit resolution and 125 MSPS signal output alongside real-time waveform acquisition. The proposed design achieves hardware integration dual-channel independent output, touchscreen control, network-based debugging. It provides a zero-radiation-risk experimental platform for nuclear detector calibration and nuclear imaging electronics development, holding significant implications for enhancing the safety of nuclear technology applications.

Keywords: Nuclear signal generator, FPGA, Signal generation

Nuclear technology is a modern high-tech field widely applied in medicine, agricultural production, environmental protection, and other domains. However, we must recognize that while nuclear technology creates benefits for humanity, it also introduces certain hazards [1]. Therefore, to ensure public safety while developing and utilizing nuclear technology, we designed a simulated nuclear signal generator to support advancements in the field [2]. Compared to real radioactive sources, it offers several advantages: (1) Safety: Using simulated nuclear signals instead of real radioactive sources eliminates radiation risks during experiments and reduces dose exposure. (2) Flexibility: Real radioactive sources are limited in variety, and certain specific nuclides are difficult to obtain, whereas simulated nuclear signals can flexibly adjust parameters to provide simulation of various types of radioactive source signals.

Research on nuclear signal generators began in the 1950s, with early analog component-based solutions exhibiting poor performance [3]. In recent years, with the rapid development of electronic technology, the combination of Field Programmable Gate Array (FPGA) and Digital-to-Analog Converter (DAC) has become the mainstream hardware architecture. In 2017, Ponikvar developed a nuclear signal generator conforming to exponential decay patterns [4];

Yin and Jin also developed related equipment in 2018 and upgraded it again in 2024 [5,6]. Additionally, commercial products such as the CAEN DT series employ similar schemes, enabling specific energy spectrum and time distribution configurations through parameter settings [7]. Building upon this foundation, we have designed a high-quality simulated nuclear signal generator that, in addition to meeting the temporal requirements of Poisson distribution and amplitude requirements of energy spectrum distribution, supports custom waveform and pile-up simulation. Equipped with a touchscreen, it can operate independently without a host computer. While assisting in the design of nuclear detection and imaging electronics, it also promotes the development of nuclear technology as a whole. This paper focuses on the hardware design; for firmware details and comprehensive test results, please refer to [8].

2 Hardware Design of the Simulated Nuclear Signal Generator

The simulated nuclear signal generator designed in this paper consists primarily of a digital board and an analog board, as shown in Figure 1 [Figure 1: see original paper]. The digital board uses an FPGA as its main chip, primarily responsible for implementing nuclear signal simulation algorithms and communication with the host computer. The analog board centers on a DAC chip, converting the digital signals generated by the FPGA into analog signals. Data communication between the two boards is achieved through Samtec board-to-board connectors.

2.1 Digital Board Design

The digital board comprises several modules. FPGA: The main control chip of the digital board, which receives commands from the host computer or touchscreen, performs corresponding logical or data processing based on these commands, and ultimately generates nuclear signals. FLASH: Used to store the FPGA's firmware program, ensuring normal operation after power cycling. Clock: Provides operating clocks for all modules on both digital and analog boards. Power Supply: Provides power for all modules on both digital and analog boards. USB: Enables communication between the FPGA and the host computer. Microcontroller: Facilitates communication between the FPGA and the touchscreen. Detailed hardware descriptions for each component follow below.

2.1.1 Digital Board FPGA Circuit Design FPGA is a programmable logic device—a semiconductor component whose circuitry can be reconfigured through programming. Its circuits are not fixed during manufacturing but can be programmed and reconfigured as needed during use. This design employs a Xilinx Kintex-7 series FPGA with the following primary connections: Bank12 connects to the USB module for host computer communication, Bank18 connects to the microcontroller for touchscreen communication, and Banks 13, 15,

and 16 connect to Samtec's 156-pin connector for communication with the analog board. Additionally, a DDR chip is incorporated for data caching, physically connected through Banks 33 and 34.

2.1.2 FLASH Circuit Design Since the FPGA's internal program is lost after power-off and requires reprogramming, a FLASH chip is integrated on the digital board. Upon each power-up, the program stored in the FLASH chip is automatically loaded into the FPGA. The hardware design is illustrated in Figure 2 [Figure 2: see original paper]. The chip operates with a 3.3V power supply. This design utilizes four data lines for simultaneous configuration, accelerating the FPGA configuration process during power-up.

2.1.3 Digital Board Clock Design This project employs a clock chip to generate a 200 MHz differential clock signal, which is directly input to the FPGA's clock port. After processing through the FPGA's internal MMCM and PLL clock IP cores, multiple clock frequencies are generated, among which the 125 MHz clock serves as the system's main clock, meeting the timing requirements of the DAC and other components. Additionally, the hardware uses another clock chip to generate a separate 125 MHz differential clock signal, which enters a CDCLVD1208RHDT clock fanout chip to produce three source-synchronous clocks at 125 MHz. These three clock signals are ultimately fed to the FPGA clock input port, the FPGA GT module clock input port, and the analog board.

2.1.4 Power Supply Circuit Design The power supply design for this project is relatively complex and can be divided into three main modules, as shown in Figure 3 [Figure 3: see original paper]. The first module provides power required for FPGA operation. The second module supplies power for peripherals such as USB and microcontroller components. The third module delivers power for the analog board.

The first module includes bank voltages of 3.3V, 2.5V, and 1.8V, enabling different I/O standards for various banks. It also provides a 1V core voltage and 1.8V auxiliary voltage. Finally, to ensure proper operation of the GT modules, three MGT power supplies—MGTAVCC, MGTAVTT, and MGTVCCAUC—deliver 1.0V, 1.2V, and 1.8V respectively. Since GT modules operate at high speeds with stringent power requirements, all MGT power supplies in this design are generated using LDO chips to minimize power ripple.

The second power module caters to the microcontroller and USB chip, with dedicated 3.3V and 1.2V supplies designed to ensure adequate power delivery.

The third module relates to the analog board. To meet the analog board's high-performance power requirements and diverse voltage needs, relevant power conversions are implemented on the digital board. DC-DC converter chips transform the input 12V supply into three voltage levels: 12V, 5V, and -12V. The analog board subsequently uses LDO chips to further convert these three volt-

ages into the final power scheme required by the design. For detailed information on the analog board's power supply, please refer to Section 2.2.3.

2.1.5 Digital Board USB Circuit Design The primary communication method between the digital board and host computer is implemented via USB protocol, facilitated by the Cypress CYUSB3014-BZXI chip. The hardware design is illustrated in Figure 4 [Figure 4: see original paper]. The USB circuit design is relatively complex: it connects to the host computer through a USB Type-C interface, while communicating with the FPGA through a GPIF II interface. In addition to 32-bit data communication, the GPIF II interface includes control signals such as FLAGA, FLAGB, FLAGC, FLAGD, SLCS, SLOE, SLWR, SLRD, PKTEND, and PCLK. Among these, PCLK is the clock signal whose frequency determines the data transfer speed between the FPGA and CYUSB3014-BZXI chip. According to the chip datasheet, this clock signal can operate at up to 100 MHz, yielding a theoretical maximum transfer rate of 100 MHz $\times$ 32 = 3.2 Gbps. However, in practical use, the actual rate falls below 3.2 Gbps due to factors such as inter-packet gaps and overhead for upstream/downstream transactions.

2.1.6 Microcontroller Circuit Design To enable standalone operation without a host computer, the hardware design incorporates touchscreen control capability. An external STM32 chip is employed to control the display output. The communication connection between the STM32 chip and FPGA is shown in the figure below. The primary communication method consists of two SPI interfaces: one for the FPGA to control the STM32 chip for touchscreen display output, and another for transmitting touchscreen input data from the STM32 chip to the FPGA. Additionally, 14 redundant I/O connections are designed for flag bits during SPI protocol transmission, ensuring transmission stability.

Simultaneously, the STM32 chip connects to a W5500 network chip. This chip's primary function is to transmit SPI protocol data over the network to the host computer, enabling observation of SPI protocol status and the nuclear signal generator's operational state during debugging. When necessary, small amounts of data can also be transmitted from the host computer to the FPGA board through this network port.

Figure 5 [Figure 5: see original paper] SPI Chip Connection Circuit Diagram

2.1.7 Digital Board Final Circuit Design The final circuit design of the digital board is shown in Figure 6 [Figure 6: see original paper]. This circuit board comprises 12 layers total, including 4 ground layers and 8 signal layers. In addition to the aforementioned designs, a 156-pin connector is integrated on the far right side of the board for data communication between the digital and analog boards. This connector is divided into three sections, each containing 56 pins, with each section connected to one FPGA bank, utilizing a total of three banks.

2.2 Analog Board Design

The analog board centers on a DAC to implement digital-to-analog conversion functionality. In this project design, two DAC chips are employed to enable simultaneous dual-channel conversion. Additionally, an ADC is incorporated into the analog board, endowing the designed board with the capability to acquire real analog signals.

2.2.1 Analog Board DAC Circuit Design The analog board employs two single-channel AD9764 DAC chips to form a dual-channel analog signal output, with connections shown in Figure 7 [Figure 7: see original paper]. The AD9764 is a single-channel, high-speed 14-bit DAC that operates normally simply by inputting the DA conversion clock frequency at the CLOCK port, supporting rates up to 125 MSPS. The DB0-DB13 pins on the left side serve as digital signal input ports, connecting to FPGA Bank13 through the Samtec interface. The IOUTA and IOUTB pins on the right side provide analog signal outputs (in current form), which are subsequently converted to more standard voltage signals through AD8047 chips.

2.2.2 Analog Board ADC Circuit Design While a simulated nuclear signal generator does not inherently require analog-to-digital conversion (ADC) functionality, an ADC is included in this design to facilitate acquisition of real nuclear signals. Real nuclear signals can be captured through the ADC and stored as data in the host computer to establish a real waveform database. When needed, appropriate signals can be selected from this waveform library and sent back to the FPGA for use as custom waveforms. The ADC circuit connection diagram is shown below. Its operation is inverse to that of the DAC: analog signals are input through the two Ain ports on the left side and ultimately converted to digital signals transmitted to FPGA Bank15 via D0-D11, enabling waveform sampling functionality.

Figure 8 [Figure 8: see original paper] ADC Chip Connection Circuit Diagram

2.2.3 Analog Board Power Supply Circuit Design Compared to digital circuits, analog circuits are more susceptible to noise interference, necessitating power supplies with minimal ripple and noise for the analog board. All analog board power supplies utilize LDO chips to further convert voltages from the digital board, as shown in Figure 9 [Figure 9: see original paper]. As mentioned in Section 2.1.4 (Figure 3), the digital board outputs 5V, 12V, and -12V voltages. The analog board converts the 5V supply into two 3.3V supplies—one for digital 3.3V and another for analog 3.3V. The 12V supply is converted to 5V for use as analog 5V power to supply the ADC chip. The -12V output from the digital board is converted to -5V power for the AD8047 current-to-voltage amplifier chip.

2.2.4 Analog Board Final Circuit Design The final circuit design of the analog board is shown in Figure 10 [Figure 10: see original paper]. This circuit board comprises 6 layers total, including 2 ground layers and 4 signal layers. In addition to the aforementioned designs, a 156-pin connector is integrated on the far left side of the board, corresponding to the digital board's 156-pin connector for data communication between the digital and analog boards.

2.3 Circuit Board Final Design

The final assembled circuit board is shown in Figure 11 [Figure 11: see original paper], comprising both digital and analog board sections. The digital board is primarily responsible for communication and algorithm processing, while the analog board handles analog-to-digital and digital-to-analog conversion functions.

5 Hardware Testing

For test results related to firmware and software components, please refer to [8]. This section focuses on hardware testing results.

5.1 Hardware Testing

Initial hardware testing primarily includes ground resistance, power supply output voltage, and clock frequency measurements. Table 1 presents the ground resistance test results. All resistance values are normal with no short circuits detected, indicating the board can be powered on for subsequent testing.

Table 1 Ground Resistance Table FPGA3V3 FPGA2V5 FPGA1V8 FPGA1V5 FPGA1V0 MGT1V8 MGT1V2 MGT1V0 Ground Resistance/kΩ USB3V3 DACBOARD_{5V} DACBOARD_{12V} DACBOARD_-12V AVDD5V AVDD3V3 DVDD3V3

Table 2 shows the power supply output voltage test results. All voltages fall within expected ranges, with no overvoltage or undervoltage issues.

FPGA3V3 FPGA2V5 FPGA1V8 FPGA1V5 FPGA1V0 MGT1V8 MGT1V2 MGT1V0 USB3V3 DACBOARD_{5V} DACBOARD_{12V} DACBOARD_-12V AVDD5V AVDD3V3 DVDD3V3 Table 2 Voltage Output Table Output Voltage/V

5.2 USB Testing

To facilitate USB protocol testing, a dedicated FPGA USB test program was developed, as shown in Figure 12 [Figure 12: see original paper]. The FPGA side comprises three modules: the first is a data generation module that produces continuously incrementing integers with each clock cycle; the second is a FIFO for cross-clock domain data transfer between the data generation module and USB protocol; and the third is the USB protocol module on the FPGA. After

connecting the board to a computer, data reading tests are conducted, including both data integrity and data rate testing.

Figure 12 Test Program Structure Diagram The host computer test software utilizes the Cypress receiver program, which receives data in 1024-byte packets. Each packet therefore contains 256 data words. Starting from 0, each packet ends with 255 (FF in hexadecimal). The test results are shown in Figure 13.

Figure 13 [Figure 13: see original paper] USB Multi-Packet Data Results Data rate testing employs the Cypress speed test program. Results are verified from two aspects: first, the receive rate test on the host computer side, and second, FPGA packet capture for auxiliary verification. The test results are shown in Figure 14 [Figure 14: see original paper].

The left image shows the test rate on the host computer, displaying a rate of 248,200 KBps (approximately 2 Gbps). The right image shows the FPGA packet capture auxiliary verification results, where the fx3_{wdb} variable changes during most of the time, further confirming that data is indeed being transmitted continuously.

Figure 14 USB Rate Test Results

5.3 ADC Testing

ADC sampling functionality results are shown in Figure 15 [Figure 15: see original paper]. After generating a sine wave using a signal generator, an ILA (Integrated Logic Analyzer) is first used on the FPGA to capture signals and verify whether the digital input to the ADC chip is normal. The display shows a continuous sine wave, confirming proper ADC sampling functionality. The ADC sampling results are then directly input into the corresponding FIFO and uploaded via USB protocol. The sampled data received via USB is saved, parsed using Python, and displayed as a final image that matches the waveform captured by the ADC.

Figure 15 ADC Sampling Results

6 Prototype Demonstration

This research has successfully developed a dual-channel simulated nuclear signal generator based on FPGA+DAC architecture. Through an all-digital hardware design, it achieves high-precision simulation of nuclear radiation signals and zero-radiation-risk experimental verification. The physical unit is shown in Figure 16 [Figure 16: see original paper]. The front panel features two touchscreens for displaying and controlling the generator's two channels. The bottom has three interfaces: the two side interfaces are DAC outputs, while the middle interface is the ADC input. The top features a circular vent area for active cooling.

Figure 16 Simulated Nuclear Signal Generator Enclosure Display This research was supported by the Shandong Provincial Natural Science Foundation Project

ZR2022QA086.

References

[1] CAI Yongcheng, LIU Xueyu, CAI Yongjun, HE Lin. Hazards of nuclear radiation and research progress Metallurgy Industry,2023,33(02):96-102.DOI:10.13228/j.boyuan.issn1006-6543.20220083.
[2] Wang M, Zhou J, Ouyang X, et al. Gaussian shaper for nuclear pulses based on cascade convolution[J]. Nuclear Science and Techniques,2022,33(12):118-129.
[3] H.C. Hamers,A. Marseille. A double and sliding pulse generator for testing electronic instruments used in nuclear physics[J]. North-Holland,1956,22(1-5).
[4] Ponikvar, Duan. "An FPGA-based nuclear pulse generator with a prescribed amplitude distribution - ScienceDirect." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 877(2018):371-374.
[5] Yin W , Chen L , Li F ,et al.A Reconfigurable Virtual Nuclear Pulse Generator via the Inversion Method[C]//International conference on Technology and Instrumentation in Particle Physics.Springer, Singapore, 2018.DOI:10.1007/978-981-13-1313-4_{76}.
[6] Ma, Shengjie , et al. "Design and implementation of a virtual nuclear pulse signal generator." Nuclear Inst. and Methods in Physics Research, A 1058(2024).
[7] CAEN. Digital Detector Emulators. https://www.caen.it/subfamilies/digital-detector-emulator/.
[8] Yang Y , Li X , Meng F ,et al.A signal generator for simulating radiation sources based on FPGA[J].IOP Publishing Ltd, 2025.DOI:10.1088/1748-0221/20/08/T08004.

Note: Figure translations are in progress. See original paper for figures.