Research on the Evolution of Reconfigurable Chip Technology

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Abstract

This paper comprehensively reviews the evolution, technical principles, market applications, development trends, and challenges of reconfigurable chip technology. With the rapid development of information technology, emerging technologies impose higher requirements on chip performance, while traditional chip architectures struggle to meet these new demands. Reconfigurable chips, leveraging their high energy efficiency, high scalability, and high flexibility, have gradually become a key solution to this problem. The article provides a detailed review of the development trajectory of reconfigurable chip technology from theoretical inception to industrial deployment, and delves into its core technical characteristics, including dataflow-driven architecture and multi-level reconfiguration capabilities. In terms of market applications, reconfigurable chips have demonstrated significant effectiveness and broad prospects in domains such as artificial intelligence, edge computing, and data centers. Looking ahead, reconfigurable chip technology will continue to advance towards architecture innovation, ecosystem construction, integration with other emerging technologies, and vertical-domain specialization. Simultaneously, this article identifies challenges confronting reconfigurable chip technology, including dynamic reconfiguration speed, configuration information storage and loading, fragmented ecosystem development, and high market application costs. It proposes countermeasures such as optimizing dynamic reconfiguration algorithms, promoting standardization efforts, and strengthening industry-academia-research collaboration, aiming to provide scientific basis and reference for further research and application of reconfigurable chip technology.

Full Text

Preamble

Abstract: This paper comprehensively examines the evolution, technical principles, market applications, development trends, and challenges of reconfigurable

chip technology. With the rapid advancement of information technology, emerging applications have imposed increasingly demanding requirements on chip performance, while traditional architectures struggle to meet these new needs. Reconfigurable chips, with their high energy efficiency, scalability, and flexibility, have emerged as a critical solution. This article reviews the development trajectory of reconfigurable chip technology from theoretical conception to industrial deployment, delving into its core technical characteristics such as dataflow-driven architecture and multi-level reconfiguration capabilities. In market applications, reconfigurable chips have demonstrated remarkable effectiveness and broad prospects in artificial intelligence, edge computing, and data centers. Looking ahead, reconfigurable chip technology will continue to evolve toward architectural innovation, ecosystem development, integration with other emerging technologies, and specialization for vertical domains. The paper also identifies key challenges including dynamic reconfiguration speed, configuration storage and loading, ecosystem fragmentation, and high market application costs, proposing countermeasures such as optimizing dynamic reconfiguration algorithms, promoting standardization efforts, and strengthening industry-academia-research collaboration to provide a scientific foundation and reference for further research and application of reconfigurable chip technology.

Keywords: Reconfigurable chips, New architecture chips, Evolutionary history

1.1 Project Background and Significance

As information technology advances rapidly, chips have become the foundation and core of the modern information industry, with their technical level serving as an important indicator of a nation' s scientific and technological strength. In recent years, the rise of artificial intelligence (AI), Internet of Things (IoT), and 5G communications has placed higher demands on chip computational capabilities, energy efficiency, and flexibility. However, traditional chip architectures such as CPUs and GPUs have proven inadequate in addressing these emerging requirements. Reconfigurable Processing Units (RPUs), as a new class of chips capable of dynamically configuring computational resources, are gradually becoming a key solution due to their superior energy utilization, exceptional flexibility, and strong scalability. This paper aims to comprehensively review the evolutionary trajectory of reconfigurable chip technology, analyze its technical principles, market applications, development trends, and challenges, and provide a scientific basis for further research and application.

1.2 Research Purpose and Tasks

The research objectives of this paper are as follows: First, to trace the evolutionary trajectory of reconfigurable chip technology, providing a comprehensive review from theoretical conception to industrial application. Second, to analyze the technical principles of reconfigurable chips, with in-depth exploration of core characteristics such as dataflow-driven architecture and multi-level reconfigura-

tion capabilities. Third, to investigate market applications of reconfigurable chips, analyzing their current deployment and future potential in artificial intelligence, edge computing, and data centers. Fourth, to forecast development trends of reconfigurable chips, predicting future directions based on current technological trends and market demands. Fifth, to propose challenges and countermeasures for reconfigurable chips, offering solutions and recommendations for problems that may arise during development and application. Specific tasks include analyzing the current status and trends of domestic and international reconfigurable chip technology, evaluating technical feasibility and identifying innovation points and potential risks, designing product plans with clear positioning and advantages, conducting economic feasibility analysis to predict investment returns, and formulating R&D and application plans to ensure smooth project progression.

1.3 Research Methods and Scope

This study employs literature review, data analysis, and expert interviews, combined with an examination of current domestic and international development status and trends, to conduct a comprehensive analysis of reconfigurable chip technology. The research scope covers market analysis, technical feasibility assessment, product planning and design, economic feasibility analysis, and technology R&D and application planning, aiming to provide a holistic feasibility evaluation for further research and application of reconfigurable chip technology.

2.1 Definition and Characteristics of Reconfigurable Chips

A reconfigurable chip is a novel type of chip capable of dynamically configuring computational resources. Its core lies in containing programmable processing elements and interconnect networks that can, based on specific application requirements and dataflow characteristics, dynamically configure computational units, interconnect structures, and data paths during runtime using dynamic reconfiguration technology, thereby performing data-driven computation in a manner approaching that of Application-Specific Integrated Circuits (ASICs). The main characteristics of reconfigurable chips include high energy efficiency, as dynamic reconfiguration technology optimizes hardware resource utilization according to different application requirements, substantially improving energy efficiency ratios. They also exhibit high scalability, supporting multi-level reconfiguration capabilities including computational unit reconfiguration, interconnect network reconfiguration, and storage system reconfiguration. Additionally, they provide high flexibility, enabling programmability similar to CPUs while maintaining ASIC-level energy efficiency to meet diverse application requirements.

2.2 Technical Principles of Reconfigurable Chips

2.2.1 Dataflow-Driven Architecture

Unlike traditional CPUs that use instruction-driven models, reconfigurable chips employ a dataflow-driven architecture. Their hardware resources (processing elements and interconnect networks) are dynamically mapped in real-time by dataflow characteristics, eliminating traditional overheads such as instruction decoding and branch prediction, thereby achieving energy efficiency improvements of up to tenfold. This architecture enables reconfigurable chips to process complex algorithms and large-scale data more efficiently.

2.2.2 Multi-Level Reconfiguration Capabilities

Reconfigurable chips support multi-granularity reconfiguration from microarchitecture to circuit level, including computational unit reconfiguration, interconnect network reconfiguration, and storage system reconfiguration. This multi-level capability allows reconfigurable chips to dynamically adjust hardware resource utilization according to different application requirements, achieving elastic scheduling and efficient reuse of computational resources across spatial and temporal dimensions. Computational unit reconfiguration defines operator functions (such as operator type and precision switching) through configuration parameters, enabling dynamic configuration of computational units. Interconnect network reconfiguration dynamically adjusts connection topologies between computational units, optimizing data transmission paths and improving efficiency. Storage system reconfiguration optimizes caching allocation strategies based on data access patterns, enhancing data storage and access efficiency.

2.2.3 Internal Structure Composition

The internal structure of reconfigurable chips primarily consists of a computational array, reconfiguration controller, and memory. The computational array comprises processing element (PE) arrays, where each PE possesses multiple arithmetic and logic capabilities and forms complex data paths through programmable interconnect networks. The reconfiguration controller issues "configuration information" to dynamically adjust the connection patterns and operation modes of the computational array. This separation design (with independent dataflow and control flow) enables the chip to be as flexible and programmable as a CPU while maintaining ASIC-level energy efficiency. Memory is divided into configuration memory and data memory. Configuration memory stores the "configuration information" for the computational array, while data memory stores raw data, intermediate data, and result data required by the computational array.

3.1 Early Theoretical Research and Concept Verification

The concept of reconfigurable chips can be traced back to the 1960s, though it did not receive widespread attention due to technological limitations at the time. In the late 1960s, American scholar Geraid Estrin first proposed the concept of "reconfigurable computing," constructing a prototype system composed of fixed and programmable hardware that laid the theoretical foundation for reconfigurable chips. During the 1980s, high-level synthesis theory and methodology emerged as one of the core technological origins of reconfigurable chips. The FPGA (Field-Programmable Gate Array) architecture began developing as a branch of reconfigurable computing, though its applications remained limited to academic research and niche domains. In the 1990s, FPGA technology gradually matured, with companies such as Xilinx driving commercialization, but reconfigurable chips were still regarded as a complementary technology to traditional chips. In 1997, the University of California, Berkeley launched the GARP project to conduct concept verification of reconfigurable computing architectures. By constructing a reconfigurable hardware platform, the project validated the advantages of reconfigurable computing architectures in performance, energy efficiency, and flexibility, gradually drawing attention from academia and industry.

3.2 Key Technology Breakthroughs and Industrial Exploration

Entering the 21st century, reconfigurable chip technology has made significant progress alongside advancements in integrated circuit design and microelectronics manufacturing. In 2000, Chinese scholars achieved breakthroughs in core technologies such as dynamic reconfiguration and dataflow-driven architecture, proposing hardware-software co-design methodologies that endowed reconfigurable chips with the characteristic of "hardware dynamically changing with software," propelling China to become a leader in this field. In 2003, MIT launched the MORPHEUS project to explore reconfigurable computing applications in specialized domains, successfully achieving efficient support for specific algorithms and applications through a reconfigurable hardware platform. In 2006, Tsinghua University established the Reconfigurable Computing Laboratory to research reconfigurable computing theory and architecture implementation, achieving multiple key technological breakthroughs in reconfigurable chips with support from national and local governments. During the 2010s, reconfigurable chips began industrial exploration, with Samsung integrating them into consumer electronics (such as 8K TVs and Exynos SoCs) to optimize video decoding and AI image enhancement functions, validating technical feasibility. In 2015, Tsinghua University' s research on reconfigurable chips won the second prize of the National Technical Invention Award. That same year, the International Technology Roadmap for Semiconductors (ITRS) listed reconfigurable chips as "the most promising chip architecture technology for the future." In 2018, Xilinx launched the Versal series Adaptive Compute Acceleration Plat-

form (ACAP), which for the first time integrated CGRA (Coarse-Grained Reconfigurable Array) IP into FPGAs, significantly enhancing DSP processing capabilities for applications in data centers and intelligent driving [23]. In 2022, Intel integrated reconfigurable computing units into Xeon processors, improving data center energy efficiency by 40% through dynamic resource allocation, while PACT Corporation implemented reconfigurable technology in aerospace applications. By 2025, dynamic reconfiguration technology has matured to support multi-level reconfiguration from computational units and interconnect networks to storage systems, achieving tenfold energy efficiency improvements over traditional CPUs and becoming a core computing platform for AI and edge computing [16].

3.3 Commercial Application and International Competition

As reconfigurable chip technology continues to mature, its commercial applications have gradually expanded. In 2017, China' s State Council included reconfigurable computing in the "Key Common Technology System for New Generation Artificial Intelligence" in its "New Generation Artificial Intelligence Development Plan," providing key support for its development. That same year, a Tsinghua University team achieved breakthroughs in dynamic reconfiguration and multi-granularity fusion technologies, developing the "Thinker" series of reconfigurable AI chips. These chips demonstrated significantly higher energy efficiency than comparable GPUs when running typical AI tasks and were featured in a special report by MIT Technology Review. In the international market, prominent companies such as Xilinx, Samsung, and Intel have also positioned themselves in the reconfigurable chip domain. In 2018, Xilinx launched the landmark Versal series Adaptive Compute Acceleration Platform (ACAP) FPGA products, embedding advanced CGRA reconfigurable computing IP that brought revolutionary improvements to DSP processing capabilities. In early 2019, Tsingmicro Intelligence' s first reconfigurable chip—the world' s first mass-produced commercial reconfigurable chip—marked the official entry of reconfigurable chip technology into commercial application.

3.4 Technological Innovation and Ecosystem Construction

In recent years, with the rapid development of AI, IoT, and other emerging technologies, reconfigurable chip technology has continued to innovate and improve. In terms of technological innovation, reconfigurable chips have evolved from single architectures toward multi-level, multi-granularity architectures supporting dynamic reconfiguration capabilities from data level to task level. Simultaneously, reconfigurable chips have deeply integrated with other emerging technologies such as computing-in-memory and Chiplet, further enhancing their performance and energy efficiency. Regarding ecosystem construction, a complete ecosystem from algorithms to hardware has gradually formed in the reconfigurable chip domain. Multiple domestic and international companies and research institutions have launched development platforms and toolchains based

on reconfigurable chips, lowering development barriers and costs. Additionally, reconfigurable chips have actively integrated into open-source communities and standardization organizations, promoting widespread application and innovation of the technology.

4.1 Artificial Intelligence Domain

In the AI domain, reconfigurable chips have gradually become a key technology for accelerating AI algorithm execution due to their high energy efficiency, scalability, and flexibility. Reconfigurable chips can dynamically adjust hardware resource utilization according to different AI algorithms and application requirements, achieving efficient use of computational resources. For example, during deep learning training, reconfigurable chips can dynamically configure computational units and storage systems based on network structure and parameter scale, improving training efficiency and accuracy. Currently, multiple domestic and international companies have launched AI accelerators and solutions based on reconfigurable chips, such as Tsingmicro Intelligence' s TX8 series cloud reconfigurable AI chips and SambaNova' s SN40L chip systems, which have achieved remarkable results in image recognition, speech recognition, and natural language processing.

4.2 Edge Computing Domain

In the edge computing domain, reconfigurable chips have gradually become a key technology supporting intelligent edge devices due to their low power consumption, high real-time performance, and flexibility. Edge computing devices are typically deployed in resource-constrained environments requiring efficient processing of large volumes of real-time data. Reconfigurable chips can dynamically adjust hardware resource utilization according to different application scenarios and data processing requirements, achieving efficient use of computational resources. For instance, in smart home applications, reconfigurable chips can support collaborative operation of multiple intelligent devices, enabling intelligent management and control of smart home systems. In smart manufacturing, reconfigurable chips can support real-time production line monitoring and fault diagnosis, improving production efficiency and product quality.

4.3 Data Center Domain

In the data center domain, reconfigurable chips have gradually become a key technology for enhancing computational capability and energy efficiency due to their high performance, energy efficiency, and scalability. With the rapid development of big data and cloud computing, data centers face increasing computational pressure and energy efficiency challenges. Reconfigurable chips can dynamically adjust hardware resource utilization according to different workloads and dataflow characteristics, achieving efficient use of computational resources and improved energy efficiency. For example, Intel' s project integrating

reconfigurable computing units into Xeon processors effectively improved data center energy efficiency through intelligent dynamic resource allocation. Test data shows that the product reduced power consumption per unit of computing power by 40%, making an important contribution to energy savings and efficiency improvements in data centers.

5.1 Architecture Innovation and Performance Enhancement

In the future, reconfigurable chip technology will continue to develop toward architecture innovation and performance enhancement. On one hand, reconfigurable chips will adopt more advanced integrated circuit design techniques and manufacturing processes to improve chip performance and energy efficiency. On the other hand, reconfigurable chips will explore multi-level, multi-granularity architecture design and dynamic heterogeneous computing modes to achieve elastic scheduling and efficient reuse of computational resources across spatial and temporal dimensions.

5.2 Ecosystem Construction and Standardization Promotion

As reconfigurable chip technology matures and commercial applications expand, ecosystem construction and standardization promotion will become important future directions. On one hand, the reconfigurable chip domain will form a complete ecosystem from algorithms to hardware, encompassing development platforms, toolchains, and application cases. On the other hand, reconfigurable chips will actively integrate into open-source communities and standardization organizations to promote widespread application and innovation of the technology.

5.3 Integration with Other Emerging Technologies

In the future, reconfigurable chip technology will deeply integrate with other emerging technologies such as computing-in-memory and Chiplet to further enhance performance and energy efficiency. Computing-in-memory technology eliminates latency and energy overhead in data transmission by tightly integrating storage and computing units, while Chiplet technology improves integration and flexibility by packaging multiple small chips into a larger chip. The deep integration of these technologies with reconfigurable chips will provide new approaches for future computing architecture innovation.

5.4 Vertical Domain Specialization Evolution

As reconfigurable chip technology continues to develop and expand into application domains, vertical domain specialization will become an important future trend. Targeting requirements and characteristics of vertical domains such as

autonomous driving, industrial IoT, and biological computing, reconfigurable chips will form configurable template libraries and agile development kits to accelerate algorithm-chip co-optimization and customized design. This will help enhance application effectiveness and competitiveness of reconfigurable chips in specific domains.

6.1 Technical Challenges and Countermeasures

Reconfigurable chip technology faces numerous technical challenges, including dynamic reconfiguration speed, configuration information storage and loading, and control-intensive task processing. To address these challenges, several countermeasures can be adopted: optimizing dynamic reconfiguration algorithms by researching more efficient dynamic reconfiguration algorithms and dataflow mapping strategies to improve speed and efficiency; employing high-efficiency storage technologies such as high-speed, low-power SRAM and eFlash to enhance configuration information storage and loading speeds; and exploring parallel processing methods for control-intensive tasks on reconfigurable chips to improve processing speed and efficiency.

6.2 Ecosystem Construction Challenges and Countermeasures

The ecosystem construction for reconfigurable chip technology faces issues such as fragmentation and poor compatibility. To address these challenges, several countermeasures can be implemented: promoting standardization by actively participating in domestic and international standardization organizations to advance the standardization process; establishing open platforms that build comprehensive ecosystems from algorithms to hardware, providing unified development kits and programming interfaces to attract more developers and partners; and strengthening industry-academia-research collaboration to foster cooperation and exchange among universities, research institutions, and enterprises to jointly promote innovation and application of reconfigurable chip technology.

6.3 Market Application Challenges and Countermeasures

The market application of reconfigurable chip technology faces challenges such as high costs and development difficulty. To address these issues, several countermeasures can be adopted: reducing chip costs through optimized design and improved manufacturing processes to enhance market competitiveness; providing development tools and support services to lower development barriers and costs, attracting more developers to adopt reconfigurable chip technology; and expanding application domains to actively explore new application areas and market spaces, improving effectiveness and competitiveness across different fields.

7.1 Summary of Research Findings

This paper has comprehensively reviewed and analyzed reconfigurable chip technology from multiple perspectives including definition and characteristics, technical principles, evolutionary trajectory, market applications, development trends, and challenges. Through in-depth research and analysis, this report has reached the following main conclusions: Reconfigurable chip technology, with its advantages of high energy efficiency, scalability, and flexibility, has gradually become a key solution to bottlenecks in traditional chip architectures. Reconfigurable chip technology has achieved remarkable results in AI, edge computing, and data centers, demonstrating broad market prospects and application potential. In the future, reconfigurable chip technology will continue to evolve toward architectural innovation, ecosystem construction, integration with other emerging technologies, and vertical domain specialization. Although reconfigurable chip technology faces numerous challenges, these can be effectively addressed through measures such as optimizing dynamic reconfiguration algorithms, promoting standardization, and strengthening industry-academia-research collaboration to further advance the technology.

7.2 Future Outlook

Looking ahead, reconfigurable chip technology will play an increasingly important role in the information technology domain. As the technology continues to develop and expand into new application areas, reconfigurable chips will become an important cornerstone supporting future intelligent computing and IoT development. Simultaneously, we must remain attentive to the challenges and issues facing reconfigurable chip technology and actively seek solutions and countermeasures to promote continuous technological progress and enhanced application effectiveness.

Note: Figure translations are in progress. See original paper for figures.