

A Novel Pixel-Chip-Based Region-of-Interest Readout Design

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Abstract

This paper presents a novel pixel chip readout scheme: the Region-of-Interest Readout Circuit (ROIRC), which is designed for large area, large array pixel chips and Gas Pixel Detector (GPD). This design employs a sentinel pixel detection strategy, enabling rapid identification and prioritized readout of the pixel regions containing signal events. During the scanning readout of these signal events, ROIRC employs a Block-based readout approach, effectively minimizing the readout of non-signal pixels. The functionality of ROIRC has been successfully implemented on both the ASIC and FPGA platforms. In the tests of the ROIRC, the detector is capable of detecting low-energy X-rays in the range of 2-10 keV and support multiple event readouts, and the detector can perform effective readout of effective photons with a flux of up to $15\text{k} \cdot (\text{cm}^{-2} \cdot \text{s}^{-1})$.

Full Text

Preamble

A Novel Pixel-Chip-Based Region-of-Interest Readout Circuit Design

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This paper presents a novel pixel chip readout scheme: the Region-of-Interest Readout Circuit (ROIRC), designed for large-area, large-array pixel chips and Gas Pixel Detectors (GPD). This design employs a sentinel pixel detection strategy, enabling rapid identification and prioritized readout of pixel regions containing signal events. During the scanning readout of these signal events, ROIRC utilizes a block-based readout approach, effectively minimizing the readout of non-signal pixels. The functionality of ROIRC has been successfully implemented on both ASIC and FPGA platforms. In tests of the ROIRC, the detector is capable of detecting low-energy X-rays in the range of 2–10 keV and supports multiple event readouts, and the detector can perform effective readout of photons with a flux of up to $15\text{ k cm}^{-2}\text{ s}^{-1}$.

Keywords: ROIRC, Topmetal-L, LPD, pixel chip, X-ray

Introduction

POLAR-2 is the next-generation space station detector for the Chinese POLAR experiment, which is based on the same Compton scattering measurement principle as POLAR, but with an extended energy range and an order of magnitude increase in total effective area for polarized events. The Low Energy X-ray Polarization Detector (LPD) is one of the three payloads in the POLAR-2 experiment. LPD is specifically designed to observe the polarization of Gamma-Ray Burst (GRB) prompt emission in the energy range of 2–10 keV and to measure the polarization of GRBs as well as their very early X-ray afterglow, both in terms of polarization degree and polarization direction [1–3]. This observation is achieved using an array of X-ray photoelectric polarimeters based on GPD. Pixel chips have excellent characteristics in terms of energy resolution, fast time response, and high spatial resolution. They have been widely used in space exploration; thus, the anode pixel readout chip is one of the core devices [4–10]. Pixel chips typically consist of two parts: the pixel array and the readout circuit. The readout circuit significantly impacts the performance of the pixel chip.

Currently, there have been a series of studies on the readout design of pixel chips. Typical readout designs of pixel chips, such as the ALPIDE chip, are applied in the ALICE ITS experiment at the Large Hadron Collider at CERN. The pixel chip readout of ALPIDE employs a hit-driven fashion, reading out only the pixels that are hit by particles. The in-pixel multiple-event is read out asynchronously by the priority encoder circuit in each double column. This design is not only fast in response but also power efficient, as the expected occupancy is low, and only hit pixels are read out in a hit-driven fashion [11–14]. In the Imaging X-ray Polarimeter Explorer (IXPE) and the Enhanced X-ray Timing Polarimetry (eXTP) mission, the XPOL-I and XPOL-III pixel chips are employed. These pixel chips possess self-triggering capability, enabling the

localization of regions of interest that contain photoelectron tracks. Inside the chip, every 2×2 pixel array is connected in a logical OR-ed configuration to form a trigger mini-cluster. Once this structure is triggered by signal events, the core logic automatically triggers all pixels within the smallest rectangular area that includes the trigger mini-cluster. The chip calculates and provides the coordinates of the upper-left and lower-right corners of this rectangular area, thus enabling rapid and complete readout of the signal event [15–18].

The electronics system for cosmic X-ray polarization detection (CXP), which functions as a prototype detector for the LPD, employs the Topmetal-II— chip for its anode readout [?, ?]. The successful operation of CXP has determined that the Topmetal series of chips will be used as the anode readout for GPD in the LPD, with the series having developed chips such as Topmetal-II—, Topmetal-M1, and Topmetal-M2. The readout modules of these chips all employ the Rolling Shutter readout scheme, which operates by sequentially reading out each pixel, regardless of whether the pixel has been hit by the signal event, and requires a wait time of one frame for the next readout [21–24]. As the array size of Topmetal pixel chips increases, the scanning frame rate of the chips will significantly decrease, and power consumption will also increase. Compared to CXP, the pixel chips in LPD require key characteristics such as high effective area, high energy resolution, and low power consumption. This indicates that the chip design should be capable of reducing readout time for signal events, and the pixel circuit structure must meet low-power requirements. However, pixel chips based on the Rolling Shutter readout have limitations in terms of performance and power consumption, which makes it difficult to meet the demands of the LPD project. Therefore, new readout schemes need to be developed based on Topmetal chips to achieve superior performance.

This paper introduces a novel readout scheme: Region-of-Interest Readout Circuit (ROIRC), which consists of two components: the scanning module and the co-processing module. The scanning module serves as the readout circuit for the pixel chip Topmetal-L, which will be integrated into the LPD design. The co-processing module is implemented within the FPGA in the electronics. The design purpose of the ROIRC is to rapidly identify the pixels hit by signal events as priority readout areas, thereby reducing the waiting time for event readout. Compared to XPOL and ALPIDE, the ROIRC method for determining priority readout areas is implemented through the FPGA in the electronics, without the need for comparators to perform threshold comparisons. This approach meets the LPD requirement for low-power design in pixel chips. This paper has tested the ROIRC readout scheme and successfully validated it.

II. Topmetal-L Readout Module Design

Topmetal-L is a large-area CMOS pixel sensor chip designed for LPD. It is based on the Topmetal-M and Topmetal-M2 chips and fabricated using GSMC 130 nm CMOS process. As shown in [Figure 2: see original paper], the total size of the Topmetal-L chip is $17 \text{ mm} \times 24 \text{ mm}$ including a pixel matrix of $356 (\text{row}) \times 512$

(column) with the periphery circuit. As shown in [Figure 1: see original paper], the readout circuits are placed at the left and bottom of the pixel matrix. All the IO PADs are located at the left, right, and bottom of the chip to make it easy to be assembled in multi-chip applications. The total size of each pixel sensor is $45 \times 45 \text{ } \mu\text{m}^2$ and the exposed non-insulated area is $26 \times 26 \text{ } \mu\text{m}^2$. Each Topmetal is surrounded by a guard ring with the same metal layer, which is covered by an insulating layer. The coupling capacitance between the guard ring and the top metal can be used for pixel performance calibration. The guard ring of each pixel can be applied with an external voltage signal to emulate the electrons generated by particle hits. While testing the pixel cell, this voltage signal is supplied with a signal generator to characterize the performance of the CSA.

As shown in [Figure 3: see original paper], each pixel unit consists of a Topmetal sensor, a charge sensitive amplifier (CSA), a two-stage source follower circuit, and row readout selection switches. The Topmetal working principle is based on a patch of the topmost metal layer acting as a charge collection electrode, placed in each pixel cell, and the Topmetal is connected directly to the CSA. The Topmetal sensor of the pixel unit is responsible for collecting charge signal and converting it into voltage signal through the CSA for amplification. The CSA consists of a folded cascode operational amplifier, a feedback capacitor (C_f), and a discharge resistor (M_f). The folded cascode architecture provides high gain and superior linearity, as shown in [Figure 4: see original paper].

The feedback capacitor C_f (1 fF) is formed by the parasitic capacitance between two metal layers. The charge-to-voltage conversion gain of the CSA is $\Delta V_{out}/Q_{in} = -1/C_f$, where Q_{in} is the input charge, and ΔV_{out} is the output voltage. The decay time constant of the CSA output signal is given by $\tau = R_f \cdot C_f$, where R_f represents the equivalent resistance of M_f . By adjusting the gate voltage of M_f , we can modify the value of R_f , thereby controlling the decay time of the output signal. Since the CSA discharges the charge stored in C_f to realize signal attenuation, the readout logic of the chip needs to read out the pixels containing the charge signals as quickly as possible. As shown in [Figure 5: see original paper], the single pixel response to a particle signal is depicted. Upon charge deposition, the sensor output exhibits a rapid step increase, followed by an exponential decay. The X-axis shows relative decay time, while the Y-axis indicates output signal amplitude. Time 1-4 represent readouts of the signal at different instances.

The output signal from the CSA is processed through two stages of the two-stage source follower. The signal is read out via row and column switches. In each column, all row readout selection switch outputs are connected to the column readout selection switch. The readout circuit of the Topmetal-L chip, as an important component of the ROIRC (i.e., the scanning module), is implemented using the standardized digital ASIC process. Designed in an L-shape, this scanning module is embedded in the lower left corner of the pixel chip and is responsible for the data readout function of the Topmetal-L chip. Compared to the traditional Rolling Shutter readout circuit, the advantage of this scanning

module lies in its ability to adjust its working method through multiple sets of parameter configurations, thereby offering flexibility and diversity in scanning schemes.

As shown in [Figure 6: see original paper], each parameter configuration method of the scanning module employs serial input of multi-bit data. The scanning logic and parameter configuration logic operate on independent clocks. This approach allows for customized design of different logic blocks to meet their specific timing requirements. The row readout enable switch of the pixel unit, the chip-level column readout enable switch, and the control of the column start switch are all connected by the scanning module. The pixel scanning module achieves timing convergence under the 50 MHz clock constraint for both the scanning logic and data configuration logic. However, due to analog readout circuit limitations, the 10 MHz scanning clock is utilized in chip testing. The function of each parameter is shown in . The pixel switching time T_{scan} is 100 ns, the data configure time T_{shift} is 20 ns, and the data configuration time is 20 ns per bit. Each parameter configuration involves a 10-bit serial data and two enable load bits. The time required to complete one data configuration T_{data} is 220 ns.

The input signals for the scanning module are all provided by the co-processing module, and the circuit function of the co-processing module is implemented in the FPGA. The FPGA provides enhanced flexibility and adaptability in the design of the co-processing module, significantly improving its compatibility with low-energy X-ray detectors across diverse electronic systems. The design developed for the co-processing module on the FPGA can also be ported to digital ASIC implementation. The operational principles of the scanning module and the co-processing module, their working relationship, and the implementation scheme are illustrated in [Figure 6: see original paper]. This section primarily focuses on the circuit design from the perspective of the ASIC. In the following section, we will present a comprehensive overview of the ROIRC design, integrating the FPGA within the electronics system.

III. Region of Interest Readout

The ROIRC workflow is as follows: (1) In the initial phase, the co-processing module directs the scanning module to perform scanning readout at equal row and column intervals. This process is defined as “sentinel monitoring scanning,” where the pixels scanned in this process are defined as “sentinel pixels.” Those sentinel pixels that are hit by signal events are defined as “trigger pixels.” (2) The scanning module calculates the area that needs to be scanned based on the positions of the “trigger pixels.” (3) To ensure complete readout of the signal events, the ROIRC also performs a peripheral expansion of the area that needs to be read out; this process is defined as “inflation processing.” This paper will elaborate on three aspects of the ROIRC algorithm: sentinel detection scanning, region scanning, and inflation processing.

As illustrated in [Figure 7: see original paper], the schematic diagram shows the random selection of rows 123–136 and columns 51–71 from the chip matrix. The scanning module divides the parameters received from the co-processing module into six distinct groups: row start, row end, row step, column start, column end, and column step. With these six sets of parameters, the working method of the scanning module can be determined. Figure 7: see original paper demonstrates how configuring these parameters enables switching between different scanning modes, such as sentinel detection scanning and area scanning. Furthermore, [Figure 8: see original paper] illustrates the process by which the ROIRC captures and records the complete particle trajectory.

The readout architecture comprises two core components: the scanning module integrated into the Topmetal-L chip and the co-processing module implemented in the FPGA. The scanning module receives parameters from the co-processing module, updates the scanning configurations, and reads out the pixels that have been scanned. The co-processing module is responsible for determining the scanning method and for sending control parameters to the scanning module. The scanning area is determined by setting the pixel start address, pixel end address, and the number of row and column steps.

A. Sentinel Monitoring Scanning and Threshold Comparison

The sentinel monitoring scanning process is illustrated in Figure 7: see original paper. Sentinel pixels are uniformly distributed across rows and columns of the pixel array. The purpose of sentinel detection scanning is to quickly determine the arrival of particle events by increasing the frame rate. If no signal event occurs, the scanning module repeatedly performs this process. The distribution interval of the sentinel pixels is determined by the row/column step parameters, and only these pixels are read out during sentinel scanning. In each frame of scanning, the co-processing module stores the sentinel pixel data for that frame. During subsequent frame scans, the current sentinel pixel data are subtracted from corresponding values in the previous frame. If the difference exceeds the set threshold, it is determined that an effective signal event has occurred around that sentinel pixel, and the pixel is identified as the trigger pixel. The co-processing module records the address information of all trigger pixels in the current frame.

The time T_{sen} required for sentinel monitoring scanning per frame can be calculated using equation (1), where N_{pixel} is the total number of pixels in the array, N_r -step is the number of row steps, and N_c -step is the number of column steps during the scanning process. T_{scan} and T_{data} are known (see more details in Section II).

$$T_{sen} = \frac{N_{pixel}}{(N_{r-step} \times N_{c-step})} \times T_{scan} + T_{data} \quad (1)$$

B. Region Scanning

The region scanning scheme is initiated upon detecting the trigger pixel, as shown in Figure 7: see original paper. This method employs a block-based approach to define the readout region. Compared to the alternative method of calculating minimum bounding rectangles through ROIRC logic (i.e., determining the coordinates of Xmax, Xmin, Ymax, Ymin for the area), the block approach can effectively reduce the number of pixels in the region scanning and decrease the readout time for signal events. This method is more efficient in capturing the complete signal events with minimal readout overhead.

The ROIRC performs a sequential row-by-row and column-by-column scan of these block regions, outputting the corresponding pixel information. As depicted in Figure 7: see original paper, the dimensions of each block are determined by the row and column spacing of the sentinel pixels. This configuration enables contiguous readout areas through cascading of adjacent triggered blocks, eliminating redundant partial-pixel scanning during single-event readout. If the row spacing between sentinel pixels is 2 and the column spacing is 4, then the size of each block is 3 pixels by 5 pixels. Region scanning proceeds block-by-block, where each sentinel pixel defines a distinct block. The spacing of the sentinel pixels can be optimally allocated according to the specific application environment, which enhances the refresh rate during monitoring and improves the capture rate of particle events. Once the region scanning readout is completed, sentinel monitoring scanning resumes to monitor for subsequent signal events. Each block scan requires scanning module parameter reconfiguration; thus, the single-block scanning time T_{block} is calculated using equation (2), where N_{block} is the number of pixels in a single block.

$$T_{block} = T_{shift} + T_{scan} \times N_{block} \quad (2)$$

C. Dilation Processing

As shown in [Figure 8: see original paper], particle signal events typically deposit energy in irregular, spatially stochastic patterns across the pixel array. When edge signals exhibit insufficient amplitude, the difference between the sentinel frames before and after the event may not change significantly. This prevents the sentinel from being triggered as a trigger pixel. Consequently, reading out only the blocks containing the trigger pixels may result in incomplete readout of the signal event. To address this issue, an inflation process is introduced during region scanning to ensure complete signal-event readout. The concept of inflation processing is as follows: not only are the blocks containing the trigger pixels read out, but also the blocks surrounding the trigger pixels that contain sentinels are read out to ensure the complete readout of the signal event. [Figure 9: see original paper] illustrates the implementation process of the inflation algorithm.

The time required for region scanning can be calculated using equation (3),

where $N_{trigger}$ is the number of blocks containing trigger pixels, and N_{dp} is the number of blocks after dilation processing.

$$T_{area} = N_{trigger} \times T_{block} + N_{dp} \times T_{block} \quad (3)$$

IV. Test Results

This paper validates the ROIRC based on the Topmetal-L chip and GPD, focusing on aspects including the readout mechanism, readout rate, completeness of readout signal events, and readout implementation for different particle tracks. Section IV.A details the setup of the testing platform.

A. Test Setup

The experimental test platform is depicted in [Figure 16: see original paper]. The testing system is composed of the GPD, an electronic system, and experimental test instruments. As shown in [Figure 16: see original paper], the chip is placed within the gas chamber. The interior of the gas chamber approximately consists of three critical regions: the electron drift region, the electron multiplication region, and the charge collection region. The gas microchannel plate (GMCP) is employed as the electron multiplier in the electron multiplication region. The working gas within the chamber consists of helium and dimethyl ether (DME) in a 3:7 ratio. The mixed gas inside the chamber enhances the interaction between the X-rays and the gas molecules in the electron drift region, effectively inducing photoelectric effect and converting X-rays into photoelectrons. Under the influence of the electric field, these electrons move to the upper surface of the GMCP and enter the channels through the small orifices. Within these channels, a cascade multiplication of the initial electrons occurs, leading to the generation of a significant number of secondary electrons. These secondary electrons eventually exit the GMCP and are collected by the Topmetal. X-rays are emitted by the ^{55}Fe source or the X-ray generator. These X-rays pass through a beryllium window on the gas chamber to enter the chamber.

The test electronics are divided into the bonding board, the read-out board, and the FPGA core control board, with the interconnections of these three electronic boards depicted in [Figure 11: see original paper]. The function of the read-out board is to connect with the bonding board and transmit the pixel readout signals to the ADC on the FPGA core control board. The input dynamic range of the ADC is -1 to 1 V, and the sampling resolution is 12 bits. The role of the FPGA core control board is to implement the functions of the co-processing module and to handle data transfer. The control commands and data transmission between the electronic system and the PC are all through the Peripheral Component Interconnect express (PCIe) interface. The readout board can be connected to the oscilloscope to display the output signals of the pixels. Testers can inject square wave signals into the guard-ring structure of

Topmetal-L to simulate the process of negative charge injection into the top metal layer.

As shown in [Figure 12: see original paper], the yellow signal represents the CSA output of the pixel chip, and the pink signal line indicates the injected square wave signal. Each pixel responds to the falling edge of the square wave signal and decays slowly.

B. Noise Testing and Pixel Shielding

As described in Section IV.C, the condition of “trigger pixels” is closely related to the trigger threshold set in the co-processing module. Due to the limitations of CMOS technology, some pixels in the chip may exhibit higher noise levels, as shown in [Figure 13: see original paper]. If these high-noise pixels are selected as sentinel pixels, their noise fluctuations can exceed the set threshold, causing the co-processing module to trigger erroneously and leading to frequent initiation of region scanning. To address this issue, this paper proposes implementing a bad-pixel masking algorithm in the ROIRC.

In this test, we compared the output signal baseline of all pixels in the Topmetal-L chip across consecutive frames and visualized in binary the pixels with differences exceeding the threshold, as shown in Figure 14: see original paper. As the threshold increases, the number of white points (pixels with differences exceeding the threshold) decreases. However, setting the threshold too high may obscure “defective pixels” while causing valid signal events to be missed due to the failure in triggering pixels, especially during the detection of low-energy X-ray signal events. Therefore, according to the test requirements, pixels with noise levels exceeding the set threshold are defined as “defective pixels”. The ROIRC can record the addresses of these defective pixels and shield them to prevent further participation in processing. As shown in Figure 14: see original paper, with the trigger threshold of 100 mV and no signal injected into the chip, the system no longer processes these defective pixels, and this strategy effectively suppresses noise-induced false triggering.

C. Validation of Readout Scheme Feasibility

Testers can configure the ROIRC parameters based on the pixel count and energy of the signal event. The scanning module’s start address for rows and columns is set to 0, with end addresses at row 356 and column 512. The step size for both rows and columns is 5 pixels. Each block corresponding to a sentinel pixel contains 25 pixels, and the trigger threshold is set to 100 ADC counts. This section validates the implementation of the ROIRC readout mechanism. The radioactive element ^{55}Fe emits monoenergetic X-rays of 5.9 keV, and the detection range of the LPD detector is between 2 and 10 keV. Consequently, ^{55}Fe can be utilized to validate whether the ROIRC enables the detector to capture photoelectron signals generated by low-energy X-rays.

[Figure 15: see original paper] illustrates the capture of signal events by ROIRC. Figure 15: see original paper displays the sentinel scanning process in the 512×356 pixel matrix, where the evenly spaced blue dots represent the pixel values read out by ROIRC during sentinel monitoring scanning, with all other pixel values set to 0, and the red wireframe enclosing the triggered scout pixels. Figure 15: see original paper represents the event signals from the regional readout, while Figure 15: see original paper provides a magnified view of these event signals. Figure 15: see original paper shows the sentinel pixel information at the local position of the pixel chip. Each readout sentinel pixel is evenly spaced and uniformly distributed. The scanning region in Figure 15: see original paper corresponds to the position of the triggered scout pixel in Figure 15: see original paper. Figure 15: see original paper demonstrates that in one single frame of sentinel monitoring scanning, ROIRC can support the triggering of multiple sentinels and perform multi-region readout operations based on the sequence of trigger pixel positions. According to equation (1), equation (2), and equation (3), under the scanning step of 5 pixels in both row and column directions, the maximum dead time required for reading effective event signals is 709.24 s. In contrast, under the Rolling Shutter readout mode, the maximum dead time reaches 18227.2 s. Because of this scanning scheme, the frame rate depends only on the chip's pixel cells and its highest scanning frequency.

D. Complete Readout Rates

ROIRC is capable of rapidly reading out event signals while ensuring that the signal events are entirely located within the pixel region of the region scanning. In [Figure 17: see original paper], pixels marked in red indicate the triggered sentinel pixels. Address information of the sentinel data enables the backend data processing to determine the scanning region. In the readout logic, all sentinel pixels are positioned at the center of the block region. By locating sentinel pixels, the data processing can determine whether the entire trajectory of the signal event is within the scanning region, thereby confirming whether the signal event has been fully read out. The experiment collected approximately 5,000 signal events, and the validation results showed that the trajectories of all events were fully read out.

ROIRC uses the block-based readout to capture signal events of various track shapes and pixel coverage. Even if multiple event signals are triggered in one single sentinel scanning, the readout logic ensures all event readout during the subsequent regional scanning. [Figure 18: see original paper] shows that Figure 18: see original paper presents particle tracks from ^{55}Fe signals, and Figure 18: see original paper shows tracks from alpha particle signals. Figure 18: see original paper illustrates the simultaneous generation and reading of both signals during the same sentinel scanning period. As indicated in Figure 18: see original paper, the black wireframe indicates the pixel area (composed of all sentinel pixels' blocks) during region scanning.

E. Readout Rate

As described in Section II, the signal event amplitude collected by the Topmetal-L pixel chip decays over time. Failure to read out signal events in time may result in partial data loss. The chip's event readout rate—defined as the number of fully processed events per unit time—is a key metric for measuring chip performance.

As shown in Figure 19: see original paper, which depicts the test platform, the chip is placed within the GPD. By adjusting the intensity of the X-ray generator, we can alter the quantity of signal events. Figure 19: see original paper shows the distribution of all signal events, where areas with higher brightness indicate a greater number of signal events passing through those regions. All these signal events were read out by the ROIRC. As shown in [Figure 20: see original paper], under the ROIRC readout mode, when the effective photon count rate is less than $15\text{k cm}^{-2}\text{s}^{-1}$, the count rate of the chip increases linearly with the X-ray intensity, meaning there is no signal event overlap. However, when the effective photon count rate exceeds $15\text{k cm}^{-2}\text{s}^{-1}$, the count rate no longer increases linearly, and some events will overlap. This demonstrates that the detector can effectively read out signals with effective photon fluxes up to $15\text{k cm}^{-2}\text{s}^{-1}$.

V. Conclusion

We have designed and tested a novel readout circuit design based on the pixel chip Topmetal-L, named ROIRC, which is implemented by the digital ASIC and the FPGA in the electronics. We have detailed its design structure, logical working principle, and functional behavior. Additionally, we have introduced test results, which include X-ray tests based on the radioactive element ^{55}Fe and the X-ray generator. ROIRC can be divided into two parts: the scanning module and the co-processing module. The scanning module, serving as the readout circuit for Topmetal-L, is primarily responsible for receiving parameters sent by the co-processing module, updating the scanning method, and reading out the scanned pixels. The main function of the co-processing module is to determine the scanning method and send control parameters to the scanning module. The entire algorithm achieves rapid and complete readout of signal events through sentinel monitoring scanning and regional scanning.

Under the ROIRC operating mode, GPD can detect low-energy X-rays in the range of 2 to 10 keV. Multiple regions can be triggered and read out in one single frame of sentinel scanning detection. The block region readout method can effectively reduce the scanning of invalid pixels. When the effective photon count rate is less than $15\text{k cm}^{-2}\text{s}^{-1}$, the readout rate of ROIRC for signal events increases linearly. Due to the flexibility of ROIRC, its operating modes are diverse, making it particularly suitable for scenarios where pixel chips require large-scale assembly, low power consumption, and large detection areas.

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