Design and Implementation of a Novel Integrated Timing and Fast Protection System for In-Hospital AB-BNCT

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Abstract

Boron neutron capture therapy (BNCT) is an advanced targeted radiotherapy that exploits the high affinity of the 10B nucleus for capturing neutrons. This therapy involves the use of neutron beams in combination with boron compounds, which preferentially accumulate in cancer cells. Recent advancements in accelerator-based neutron sources have propelled accelerator-based BNCT (AB-BNCT) to the forefront as a highly promising modality. This is due to its significant advantages, including reduced capital investment, simplified operation, and ease of implementation in hospitals worldwide. In 2022, the first fully independent AB-BNCT facility in China, located at Dongguan People's Hospital, was successfully developed by the Institute of High Energy Physics of the Chinese Academy of Sciences. The timing and fast interlock systems are two essential components of an accelerator facility. Designing a reconciled control system that integrates a timing system and a fast protection system characterized by high performance, stability, and reliability for accelerators is essential. Consequently, a novel architecture, which is based on in-house hardware within a compact PCI platform, has been designed and adopted for timing systems and fast protection systems to meet the requirements of AB-BNCT accelerators. The timing and fast interlock systems have been intricately involved in and have successfully completed the full suite of equipment commissioning and beam-target experiments, meeting the requirements for precise treatment in-hospital AB-BNCT. This paper focuses on a comprehensive description of the integrated system architecture, detailing the hardware and software development, and the

strategy underlying highly efficient interlocking functions. Additionally, the testing and operational status related to the system's implementation are validated for reliability, underscored the expanded applications in the field of cancer treatment.

Full Text

Design and Implementation of a Novel Integrated Timing and Fast Protection System for In-Hospital AB-BNCT

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Abstract. Boron neutron capture therapy (BNCT) is an advanced targeted radiotherapy that exploits the high affinity of the 10B nucleus for capturing neutrons. This therapy involves the use of neutron beams in combination with boron compounds, which preferentially accumulate in cancer cells. Recent advancements in accelerator-based neutron sources have propelled accelerator-based BNCT (AB-BNCT) to the forefront as a highly promising modality due to its significant advantages, including reduced capital investment, simplified operation, and ease of implementation in hospitals worldwide. In 2022, the first fully independent AB-BNCT facility in China, located at Dongguan People's Hospital, was successfully developed by the Institute of High Energy Physics of the Chinese Academy of Sciences. The timing and fast interlock systems are two essential components of an accelerator facility. Designing a reconciled control system that integrates a timing system and a fast protection system characterized by high performance, stability, and reliability for accelerators is essential. Consequently, a novel architecture based on in-house hardware within a compact PCI platform has been designed and adopted for timing systems and fast protection systems to meet the requirements of AB-BNCT accelerators. The timing and fast interlock systems have been intricately involved in and have successfully completed the full suite of equipment commissioning and beam-target experiments, meeting the requirements for precise treatment in-hospital AB-BNCT. This paper focuses on a comprehensive description of the integrated system architecture, detailing the hardware and software development, and the strategy underlying highly efficient interlocking functions. Additionally, the testing and operational status related to the system's implementation are validated for reliability, underscoring the expanded applications in the field of cancer treatment.

Keywords: AB-BNCT; Timing System; Fast Protect System; Integrated Hardware Architecture; Compact PCI; Data Driven

1 Introduction

Boron neutron capture therapy (BNCT) is a cutting-edge radiotherapy modality recognized for its ability to target tumors at the cellular level, which makes it particularly effective in treating infiltrative, recurrent, and refractory metastatic tumors [**?**]. Recent advancements in accelerator-based neutron sources have allowed accelerator-based BNCT (AB-BNCT) to mitigate the nuclear safety risks traditionally associated with reactor-based neutron sources, thereby facilitating their rapid development. Researchers utilize a method where the front-end accelerator produces neutrons by bombarding targets with proton beams [**?**]. Given the requirements of neutron irradiation, compact accelerator-based neutron source installations suitable for hospital environments are being developed globally, with projects in Russia, the UK, Italy, Japan, Israel, and Argentina advancing various accelerator types through collaborations between manufacturers and research institutes worldwide [**?**]. In 2020, the first fully domestic AB-BNCT facility was opened by the Institute of High Energy Physics of the Chinese Academy of Sciences, which has completed related cell, animal, and drug experiments [**?**]. In reference to this experimental facility, AB-BNCT in-hospital rooms were officially established at Dongguan People's Hospital to facilitate early clinical treatment experiments in 2022 [**?**]. As illustrated in Fig. 1 [FIGURE:1], this facility is composed of complex and precise components, including a proton linear accelerator, a rotating lithium target, and two linear treatment accelerator cyclotron resonance (ECR), radio frequency quadrupole (RFQ) and beam transport lines. Two of the high-energy beam transport lines lead to two horizontal treatment rooms, whereas the third high-energy beam transport line has been initially designed for beam commissioning of the accelerator and can be upgraded in the future to serve as a beam transport line for a vertical treatment room, with treatments alternating between the various treatment rooms.

To ensure the operational availability and reliability of AB-BNCT in-hospital facilities, this paper provides a novel solution to meet the requirements of accelerator timing and a fast protection system. The outline of the article is as follows. First, a brief overview of requirements for the timing system and fast interlock system is presented. Subsequently, distinguishing and critical components, an in-house hardware solution and a custom data-driven protocol based on the compact peripheral component interconnect (CPCI) bus are introduced in detail. Finally, the implementation and performance test results of these systems in online operation are discussed.

2 System Requirements

2.1 Timing System

To ensure the operational sequence of all equipment or instruments of the accelerator with beam synchronization, a global timing system is necessary to provide precise and strict triggers for subsystems and related equipment distributed in different physical spaces, such as the ECR, RFQ, beam measurement system, and neutron detection electronics acquisition system [**?**]. A detailed diagram of the timing system is shown in Fig. 2 [FIGURE:2]. An external RF signal synchronized with the RFQ and a 200 MHz onboard crystal oscillator are alternately utilized as the system input clock. A phase-locked loop (PLL) within the field-programmable gate array (FPGA) is employed to generate a 250 MHz clock from the global clock using frequency division technology, which is optimized during the logic generation process. Using digital counting, the system generates a sequence of pulses with adjustable delay, width, and frequency, enabled by high-precision counting and synchronous reset. To increase beam commissioning efficiency and address the complex tuning requirements of research applications, the pulse signal for AB-BNCT is designed to achieve high temporal resolution, as shown in Table 1 .

2.2 Fast Protection System

The AB-BNCT accelerator is engineered to deliver an average beam power surpassing 55 kW. Nonetheless, equipment malfunctions or irregularities in the beam trajectory can precipitate beam loss, potentially resulting in partial or total operational cessation [**?**]. Such occurrences pose risks to personnel safety and may disrupt the standard functioning of equipment. Consequently, the fast protection system (FPS), as a rapid response system that initiates operational shutdowns within microsecond-level reaction times, must be implemented to safeguard accelerator components from beam damage. The architecture of the interlock system and its relationship with related equipment is illustrated in Fig. 3 [FIGURE:3], while Table 2 defines important signals of the fast protection system. This paper focuses on the FPGA-based fast protection system, which interfaces with systems associated with beam current, such as the power supply, RFQ, low-level RF (LLRF), and beam instrumentation system. The complex interlocking logic among various device systems is illustrated in Fig. 3. To meet the stringent requirements associated with critical faults, the total FPS time for acquisition, redundancy, and processing must not exceed 10 µs [**?**].

3 Architecture Design of Hardware and Upper-Layer Software

3.1 Design Principles

In accordance with AB-BNCT design physics, RFQ technology facilitates precise control over the energy and flux intensity of generated neutrons, thereby

enabling tailored treatment plans for diverse clinical requirements [**?**]. By optimizing the RFQ design, neutron generation efficiency can be significantly improved, enhancing overall treatment effectiveness. Consequently, RFQ control is paramount to the stable and reliable operation of the AB-BNCT system [**?**]. Our design emphasizes RFQ requirements, incorporating functional extensions as critical elements to support both performance and flexibility. Furthermore, compared with traditional neutron sources that generally require large-scale equipment, RFQ-based technology offers a more compact and efficient design, reducing space requirements in hospitals, as shown in Fig. 4 [FIGURE:4]. Hence, the necessity for the AB-BNCT facility to be compact and highly integrated has been a guiding principle throughout the design process.

3.2 Hardware Architecture

In response to significant signal interaction requirements between the RFQ low-level control system, the timing system, and the fast protection system, a compact hardware architecture has been developed based on the standard CPCI platform, as depicted in Fig. 5

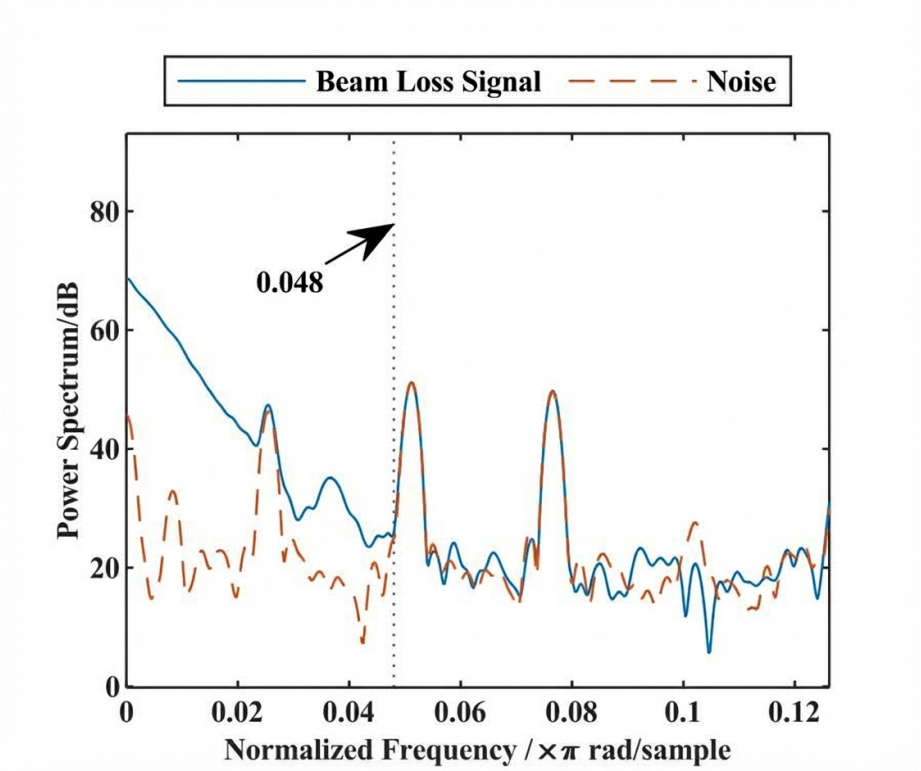

Figure 1: Figure 5

. This architecture comprises several core boards and expansion boards interconnected via a custom reverse-backboard to ensure real-time, high-speed signal interaction. Specifically, core boards are integrated into a standard CPCI chassis and utilize the CPCI bus to read and write high-performance field-programmable gate arrays (FPGAs) [**?**]. The expansion boards are customized as interface boards with various input/output interfaces according to specific functional requirements. Additionally, the reverse-backboard for CPCI J2 has been tailored with signal interaction definitions specific to their respective boards. The architecture adheres to standard 19-inch rack dimensions and includes dual power input interfaces to facilitate system reboots following power disruptions. The system conforms to standard CPCI specifications and operates within a 5 V signal environment.

Typically, the controller board interfacing the entire chassis with the host computer is installed in slot 1. The main board for the LLRF system of the RFQ is positioned in slot 3, with its expansion slots located in slots 5 and 7. The main board for the timing system is situated in slot 10, with expansion slots at 9 and 11. Similarly, the main board for the fast protection system resides in slot 13, with expansion slots at 12 and 14. Additionally, as depicted in Fig. 6 [FIGURE:6], the customized backplane reverse buckle board for CPCI J2 spans slots 3 to 14, providing physical communication ports for interactions between these boards. The primary slots (3, 10, and 13) are configured for 8 pin-to-pin connections, whereas the main and expansion slots offer 16 pin-to-pin connectivity. The core interaction signal definitions are depicted in Table 3 . All pin-to-pin connections utilize bidirectional signal routing, allowing both front panel connectivity and connectivity from the backplane reverse buckle board as needed.

3.3 Hardware Design

The design of the timing and fast protection system incorporates two identical main logic boards with custom-designed connectivity, as illustrated in Fig. 7 [FIGURE:7]. The core logic board is responsible for core logic and functionality, utilizing a high-performance field-programmable gate array (FPGA) to meet real-time digital signal processing requirements [**?**]. To ensure optimal stability and reliability, the core logic board is a customized Compact PCI (CPCI) board incorporating a PCI bridge that interconnects with interface boards via point-to-point links through a reverse backplane.

3.3.1 Core Logic Board As illustrated in Fig. 8 [FIGURE:8], the core logic board is engineered to supply essential power, clock signals, and I/O connection distribution. This board integrates both DC-DC converters and low-dropout regulators (LDOs) to effectively minimize power noise. A reference clock from a narrowband Si511BBA-200 MHz PLL is used to decrease jitter and is then provided to the FPGA as the main clock. In the prototype system, this reference clock is synchronized at 74 MHz with the RFQ. To ensure signal and power

integrity, the board employs low-loss PCB materials, minimizes signal vias, and places numerous decoupling capacitors near power supply pads. Thermal management is critical for stable operation, and the design incorporates multiple metallized vias to facilitate heat conduction while minimizing leakage current and noise. These combined components form a robust and flexible platform, enabling the FPGA to perform complex logic operations, real-time processing, and reliable applications spanning from industrial control to medical imaging and beyond.

3.3.2 Multiple-Signal Interface Boards The multiple-signal interface board performs the following functions: (1) The optical signal output interface board converts 14-channel I/O signals received from the backplane connector into optical signals. (2) The optical signal input interface board facilitates the transmission of 16 optical signals, carried via multiple fiber modes, to the backplane connector. (3) The contact signal input interface board supports the connection of 16 channels of 24 V contact signals, which are transmitted through cables to the backplane connector. (4) The contact signal output interface board converts 16 I/O signals from the backplane connector to corresponding contact-level outputs. The main function board and multifunction interface boards communicate via the reverse-backboard for CPCI J2, supporting a total of up to 14 I/O signal channels. Fig. 9

illustrates the optical signal I/O interface board.

3.4 Upper-Layer Software Based on Compact PCI

In modern control systems, upper-layer software interacts with FPGAs via specially designed device drivers, enabling efficient read and write operations on FPGA registers for system control and monitoring [**?**]. The hardware platform comprises a Compact PCI (CPCI) central processing unit (CPU) board and multiple input/output (I/O) boards. The control software is executed on the CPU board. The architecture of the upper-layer software is structured into four hierarchical levels, including the operator interface, experimental physics and industrial control system (EPICS) device support, and the Linux driver, as illustrated in Fig. 10 [FIGURE:10]. This layered structure ensures efficient data acquisition, upload, and command execution between hardware and software, utilizing a custom data-driven protocol based on the CPCI bus. Notably, the design is portable, supporting a variety of CPCI cards from different manufacturers. The driver section operates as a kernel module, avoiding user space I/O (UIO) processing across the chassis [**?**]. All interrupts are protected.

The EPICS IOC is tailored for the timing and compact system of the accelerator facility, with a control interface configured for register access and waveform reading on a one-second update cycle, functioning without direct memory access (DMA). Registers, including integer values and control/status bits within the FPGA, are defined as 32-bit signed values, simplifying the interface and enhancing security. This configuration allows operators in the central control room to

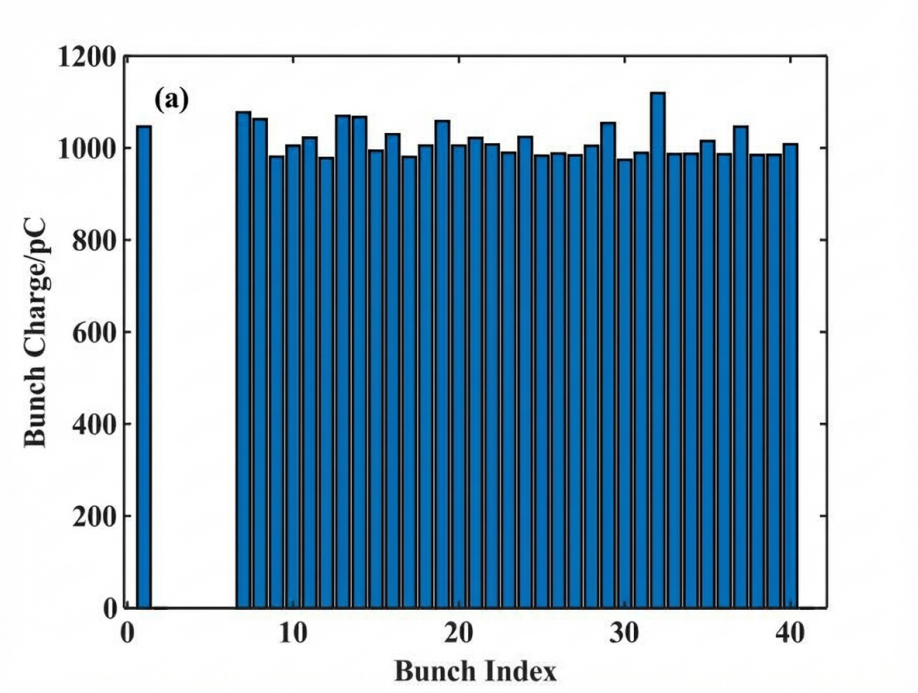

Figure 2: Figure 9

remotely adjust system settings, monitor key indicators, and diagnose performance issues, as depicted in Fig. 11 [FIGURE:11]. Furthermore, the EPICS driver features a general-purpose design that defines both the register mapping and the conversion formula between FPGA registers and EPICS records. By modifying the register mapping and conversion formula, the driver can be adapted to other I/O boards, facilitating more efficient centralized monitoring solutions. The implementation consists of a Linux kernel module PCI driver, a user-space PCI driver API, EPICS driver support through the asynPortDriver, and EPICS records. Read and write operations between user space and kernel space employ the ioctl() system call.

4 Implementation of Core Logic Functionality

4.1 Beam Operation Mode

In the design for generating synchronous logic timing signals, the extensive internal resources of the FPGA are utilized, implementing a loop method characterized by precise high-speed counting followed by resetting upon overflow. Fig. 12 [FIGURE:12] shows a schematic diagram of the synchronous timing logic processing function. The pulse generation module has various input ports, including a global clock signal, reset signal, pulse enable frequency setting register, delay signal setting register, pulse width setting register, pulse count setting register, pulse mode register, and pulse gating register. Specifically, when the pulse mode setting register is set to “0”, continuous pulse output mode is indicated; conversely, when it is set to “1”, output of a specific number of pulses is denoted, referred to as noncontinuous pulse output mode. Additionally, if the pulse gating register is set to “0”, no pulse output occurs; if it is set to “1”, output of a defined number of pulses is allowed.

Three distinct beam operation modes are integrated into the timing system to increase beam adjustment flexibility in accelerators and optimize real-time beam control during online therapy, as illustrated in Fig. 13 [FIGURE:13]. The specific logic design for synchronous timing is as follows: (1) One-shot mode: When the FPGA detects a “1” in both the pulse gating register and the FPGA pulse count setting register, the core logic activates the channel to produce a single output pulse upon detecting a transition in the trigger signal from ‘0’ to ‘1’ or from ‘1’ to ‘0’ from the trigger button, thereby enabling a single-shot beam mode. (2) Customized periodic mode: When the FPGA registers a “1” in the pulse gating register, the core logic enables the channel to produce a series of output pulses upon detecting a trigger signal transition from ‘0’ to ‘1’. (3) Continuous mode: With each rising edge of the system clock, the synchronous counter increases the delay counter. When the delay counter reaches the value specified in the FPGA delay setting register, it initiates a high-level signal and begins the pulse width counter. Once the pulse width counter matches the FPGA pulse width setting register, the pulse expires, yielding a low-level signal output. Upon synchronization with the FPGA frequency setting register, the cycle completes, resetting the delay setting register, pulse width setting register,

and frequency counter to zero to start the next timing signal generation cycle.

4.2 Machine Mode

The BNCT02 accelerator classifies machines into five distinct types based on the utilization of various beam targets during operation: ion source mode, waste beam station mode, treatment room #1 mode, treatment room #2 mode, and vertical treatment room mode (reserved). The fast protection system is tasked with making logical decisions regarding the interlocking signals of corresponding equipment and systems, depending on the selected machine mode. For a mode to be valid, only one mode should be active, with all other modes remaining inactive, as illustrated in Fig. 14 [FIGURE:14]. To enhance design generality, a hierarchical inclusion approach based on the concept of subsets and universal sets has been introduced into the shielding configuration of accelerator equipment. All devices involved across various machine modes are aggregated into a comprehensive universal set. For any specific machine mode, only a subset of this universal set is activated. Consequently, during traversal testing of device interlocking functions, a systematic and uniform test can be performed across all devices in the universal set, independent of any particular machine mode. When preparing to operate a specific machine mode, only those devices not belonging to that mode need to be bypassed, as illustrated in Fig. 15 [FIGURE:15].

4.3 Immediate Beam Shutdown

Ensuring the safety of both patients and equipment in medical applications utilizing accelerators for radiation therapy is a paramount concern [**?**]. To guarantee continuous safety and operational reliability throughout the treatment process, it is essential to implement a fast beam shutdown mechanism capable of responding effectively to unforeseen events, which demonstrates high levels of dependability. Based on the beam structure and technical characteristics of AB-BNCT, three distinct emergency beam shutdown actions have been designed to respond to various potential risk scenarios, as illustrated in Fig. 16 [FIGURE:16]: (1) Fast response for beam shutdown—immediately cut off the trigger of the ECR microwave power supply and drop off the power supply of the RFQ immediately via low-level RF; (2) Redundancy for beam shutdown—immediately drop off the power supply of the ECR microwave; (3) Stabilize the thermal state of the RFQ during beam shutdown—immediately cut off the beam gate of the RFQ via the low-level RF system, then initiate automatic recovery if the trigger of the ECR microwave power supply has stopped.

4.4 Strategy of Fast-Response Protection

Considering the distinct operating and signal characteristics of the AB-BNCT accelerator, the core fault signals include three types: interlock signals transmitted through the PLC contact interface, power system interlock signals conveyed via the optical interface, and accelerator interlock signals integrated into the hardware platform. The first type is characterized by permanent failure

of equipment once it occurs, which cannot recover automatically and requires immediate beam shutdown. In contrast, the latter type of fault is transient in nature; during momentary operation, the RFQ may experience sparking faults that typically resolve themselves within a short period without requiring manual intervention, as illustrated in Fig. 17 [FIGURE:17].

Consequently, innovative protection strategies have been developed for FPSs in response to these conditions. Specifically, upon detecting a fault, the FPS immediately initiates a beam shutdown procedure. This process involves halting the extraction timing of the ECR, reducing power to the RFQ, and disabling the beam gate signal of the RFQ. Simultaneously, the system continuously monitors the fault signal duration in real time. If the fault persists for less than 1.1 s, the FPS triggers a beam recovery sequence 1.1 s after the fault's onset, employing synchronized timing control. This recovery sequence includes reactivating the timing signal of the ECR, restoring power to the RFQ, and re-enabling the beam gate signal of the RFQ. Conversely, if the fault lasts longer than 3 s, the FPS commands the ECR ion source control system to reduce the extraction high-voltage supply to 5 kV. Upon confirmation that the voltage has successfully decreased to 5 kV, the FPS restores power to the RFQ. This protocol is designed to prevent operational anomalies such as detuning caused by prolonged power interruptions. The system locks the fault state 3 s post-fault and activates the quick stop function, which can only be re-entered into beam output mode after manual reset and release of the locks. The complete interlocking logic test is depicted in Fig. 18 [FIGURE:18].

The typical fast protection process for RFQ ignition during operation is illustrated in Fig. 19 [FIGURE:19]. Specifically, when all machinery and equipment are functioning normally, the entire accelerator can switch to beam output mode. However, if only the RFQ is ignited, the LLRF system promptly sends an interlock signal to the fast protection system. The FPS adopts two protection strategies—permanent and transient—depending on the fault duration, and executes corresponding beam shutdown actions. This approach significantly enhances operational efficiency while ensuring safe operation. Moreover, an effective beam-stopping mechanism has been implemented to improve beam availability and operation safety. This design optimizes the system's treatment plan, rendering it more clinically beneficial and cost-efficient within the in-hospital AB-BNCT environment.

4.5 Beam Commissioning

Beam commissioning requires seamless conjunction with the timing system and FPS in particle accelerators [**?**]. This coordination is essential, as the timing system depends on safety assurances provided by the FPS to prevent hazardous situations during complex beam maneuvers. Simultaneously, the FPS relies on precise operational status data from the beam manipulation and timing system to assess potential risks accurately and facilitate timely responses. Dedicated interlocking logic and modular functions, designed via a state machine approach,

are employed in the FPS, as illustrated in Fig. 20 [FIGURE:20].

In the beam operation process of AB-BNCT in hospitals, there are primarily two operational states: shutdown and startup. During the startup phase, the system is further divided into beam-on and beam-off modes. Additionally, source conditioning mode is implemented to optimize the ion source's ability to deliver a high-quality beam. Based on the flexible and reliable design of the timing system and fast protection system, transitions between these beam modes can be achieved seamlessly. This feature significantly enhances the overall availability of the facility and demonstrates excellent operational flexibility.

5 Testing and Analysis of System Performance

5.1 Synchronous Signals

The quality of synchronous signals, which serve as the timing source, significantly influences the overall performance of the system. As shown in Fig. 21 FIGURE:21, the measured frequency of the synchronous clock, which serves as the reference clock for the RFQ, is 70.4 MHz. It displays a relative jitter (peak-to-peak) of approximately 200 ps in comparison to that of the RF. This level of jitter meets the requirements for synchronous triggering, allowing for a step width of 1 µs when adjusting the pulse width or delay in ECR ion sources and other electronic devices. Conversely, as illustrated in Fig. 21(b), the frequency exceeds 1 MHz, thus meeting the criteria for in-pulse slicing of the AB-BNCT accelerator when the beam current frequency peaks at 200 Hz.

5.2 Response Time of the FPS

As described in Section 3.3, three primary types of interlock signals are integrated into the FPS. To gain a more accurate understanding of the response characteristics of each signal path, the response times of these signals were analyzed and tested individually. Fig. 22 [FIGURE:22] shows the response time for the AB-BNCT accelerator FPS, with all time parameters defined, analyzed, and explained in detail in subsequent sections.

5.2.1 Fault from RFQ When the LLRF system of the RFQ detects an internal sparking event, it rapidly shuts down the output power within approximately 300 ns and simultaneously sends an interlock signal to the FPS [**?**]. Upon receiving the signal, the termination logic immediately initiates beam gate mode. Experimental measurements show that the time difference between the power waveform and the arrival of the beam gate signal from the FPS is 180 ns, as illustrated in Fig. 23 [FIGURE:23]. In the corresponding figure, the point of pickup waveform from RFQ is P1, and the point of beam gate signal from FPS is P2. Therefore, the total response time from when the LLRF system sends the interlock signal to the FPS until the RFQ actually receives the beam termination command is 480 ns. Since both the FPS and LLRF system are integrated within the same hardware platform, the signal transmission between them does

not involve a fiber-optic link, so the transmission delay can be neglected in this process.

5.2.2 Fault from Power Supply The interlock signal from the power supply is initially transmitted via multimode optical fiber to the fiber signal interface board. It is then relayed through the CPCI backplane to the main logic board of the FPS. Within the main logic board, the core interlock logic processes the signal, prompting the system to initiate permanent beam termination. A branch of the beam-off interlock signal is dispatched to the main logic card of the timing system. Upon receipt, the logic card performs a logical AND operation with the original normal signal to generate a new control signal. This newly generated signal is then conveyed to the fiber signal output board of the timing system and subsequently transmitted via multimode fibers to the ion source extraction power supply, as depicted in Fig. 24 FIGURE:24. A detailed measurement campaign was conducted to precisely determine the time delay between P5 and P6, as shown in Fig. 24(b), which reveals a delay of 485 ns. The entire signal path includes segments of 50-meter multimode fibers. Assuming a transmission delay of 5 ns per meter, the propagation delay for each segment is estimated to be 250 ns, resulting in a total fiber transmission delay of 500 ns. Therefore, the total response time from when the power supply sends the interlock signal to the FPS until the ECR receives the termination command is approximately 1 µs.

5.2.3 Fault from MPS The machine protection system (MPS) uses electromagnetic solid-state relays to interface and output fault signals from devices such as vacuum pumps and power supplies. The overall response time is approximately 1.6 ms [**?**], as depicted in Fig. 25(a). In contrast, the FPS employs optocoupler-based contacts for signal interfacing and output. As illustrated in Fig. 25(b), the maximum transmission delay through a PLC-type node is approximately 48 µs. Considering that signals are transmitted via coaxial cables, each of the signal paths—from the device end to the MPS and from the FPS to the ion source extraction power supply—is assumed to be 30 meters, with a transmission speed of 5 ns/m [**?**]. Thus, the total transmission delay across these two segments is approximately 300 ns. Since the MPS and FPS cabinets are located next to each other, the signal transmission delay between them is negligible. Consequently, the total response time from the moment the MPS receives the interlock signal from the vacuum pumps and then sends it to the FPS until the electron cyclotron resonance (ECR) receives the termination command is approximately 1.6 ms. The time from when the MPS sends the interlock signal to the FPS until the ECR receives the termination command is not more than 100 µs.

5.2.4 Summary of Response Times Verifying that the total time required for beam stopping meets design requirements is essential. According to our analysis, Table 5 shows the typical and complete time consumption of beam

stops. The total time required to cut off the current cycle beam during RFQ ignition is calculated via Formula (1). The time needed to cut off the trigger for the extraction power supply of the ECR to intercept the current cycle beam is calculated via Formula (2), whereas the time required to drop off the high-voltage power supply of the ECR to intercept the next cycle beam is calculated via Formula (3).

$$t_{off} = t_{FPS\_logic} + t_{LLRF} = 735 \text{ ns}$$

$$t_{off} = t_{FPS\_logic} + t_{fiber} = 1.0 \ \mu\text{s}$$

$$t_{off} = t_{MPS} + t_{PLC} + t_{cable} = 1.6 \text{ ms}$$

The time consumption of the three types of beam stops, along with their performance evaluation and comparison as presented in the literature, is satisfactory. The interlocking and protection system is well suited to meet the physical requirements. The total consumption across the entire chain following a fault can be accurately determined by integrating the signal chain transmission times (as shown in Table 6) with the response time of the ECR processing to the beam stop signal. Although a detailed analysis of this process falls outside the scope of this paper, further information can be found in referenced literature [**?**].

5.3 Stability and Reliability

Since its inauguration in June 2023, the system has consistently operated for over 278 days [**?**]. The ECR proton source generates a proton beam with a maximum current of 40 mA at 200 Hz while maintaining a pulse current of 26 mA at an 80% duty cycle. The RF duty cycle of RFQ has reached 84% (200 Hz and 4.2 ms), with beam transmission efficiency over 97%, meeting design requirements. Significant modifications have been made primarily for beam uniformity, incrementally increasing the target power to 35 kW [**?**]. The beam commissioning results, as presented in Figs. 26 and 27, clearly demonstrate the stability of both the timing system and the FPS over the period from December 2024 to May 2025. The successful commissioning of the accelerator confirmed that the timing system and fast protection system's stability and reliability were assessed through protracted continuous operation, providing reliable support for future BNCT research and treatment endeavors. The hospital is currently initiating patient pre-enrollment for phase I clinical trials, with cancer treatments beginning as soon as possible. This clearly indicates that self-reliance and proficiency in BNCT technology have been achieved, establishing a technical foundation for complete domestic industrialization.

6 Summary

This paper presents an innovative comprehensive hardware and software design solution for timing and fast protection systems tailored to the AB-BNCT in-hospital project, utilizing the compact PCI platform. The test results indicate that all anticipated functions achieve consistent and reliable performance, providing essential assurances for ongoing stable accelerator operation. Compared with traditional implementations, the proposed technology approach offers several design advantages, including reduced cost, compact size, cost-effectiveness, expedited development time, adaptability, compatibility, and reusability. These benefits strongly support enhanced flexibility and the ability to independently develop and localize the entire medical BNCT treatment apparatus within China in the future. Notably, adoption of this strategy offers significant advantages in small industrial control applications.

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