A Silicon Microstrip Detector for Power-Limited and Large Sensitive Area Applications

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Abstract

A silicon microstrip detector (SSD) has been developed to have state of the art spatial resolution and a large sensitive area under stringent power constraints. The design incorporates three floating strips with their bias resistors inserted between two aluminum readout strips. Beam test measurements with the single sensor confirmed that this configuration achieves a total detection efficiency of 99.8% and spatial resolution 7.6 m for MIPs. A double- algorithm was developed to optimize hit position reconstruction for this SSD. The design can be adapted for large area silicon detectors.

Full Text

Preamble

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A silicon microstrip detector (SSD) has been developed to achieve state-of-the-art spatial resolution and a large sensitive area under stringent power constraints. The design incorporates three floating strips with their bias resistors inserted between two aluminum readout strips. Beam test measurements with a single sensor confirmed that this configuration achieves a total detection efficiency of 99.8% and spatial resolution of 7.6 µm for minimum ionizing particles (MIPs). A double- algorithm was developed to optimize hit position reconstruction for this SSD. The design can be adapted for large-area silicon detectors.

Keywords: Silicon Microstrip Detector, Bias resistor, Test Beam, Detection Efficiency, Spatial Resolution

INTRODUCTION

Silicon microstrip detectors (SSD) [1, 2] are extensively used for tracking purposes across several experiments in particle physics [3–5], nuclear physics [6], as well as in many space-borne experiments [7–15] including the Alpha Magnetic Spectrometer (AMS-02) [16, 17]. Due to stringent constraints on power consumption in space-borne experiments, the number of available readout electronic channels for SSD is limited, which necessitates careful optimization of detector designs.

The AMS-02 experiment, operating aboard the International Space Station (ISS), aims to precisely measure the composition and flux of cosmic rays throughout the ISS' s lifetime until 2030. To enhance detection acceptance by a factor of three, a new silicon tracker layer (Layer-0) will be stacked at the top of AMS-02 in 2026. Layer-0 deploys the same module design as AMS-02 flying hardware, which consists of long silicon ladders, each constructed by daisy-chaining multiple SSDs. In the Layer-0 upgrade modules, this concept will be even further stressed by daisy-chaining 8, 10, or 12 SSDs, for a total length of 65–100 cm. As depicted in Fig. 1 [FIGURE:1], the 12-SSD ladder represents the longest silicon strip detector ever built, presenting unique technical requirements.

Consequently, we have designed and implemented an SSD specifically tailored

to meet these stringent requirements for all ladders in the AMS Layer-0 tracker. In this paper, we present the detailed design of this SSD, its characterization through test beam, and performance evaluations focused on detection efficiency and spatial resolution.

II. DESIGNS OF THE SILICON MICROSTRIP DETECTOR

The SSD is a p -in-n sensor manufactured by Hamamatsu Photonics K.K, with a total area of 113 × 80 mm² and thickness of 320 µm, whose schematic is presented in Fig. 2

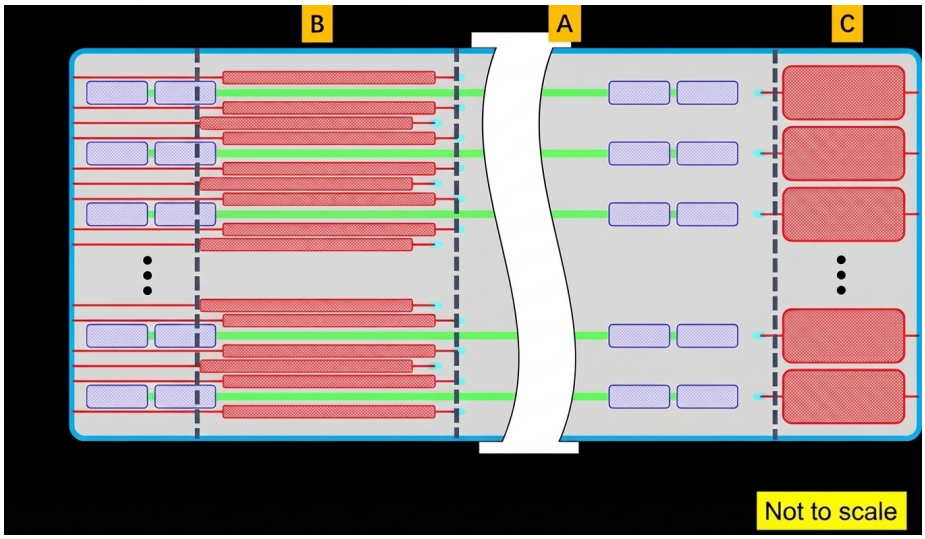

Figure 1: Figure 2

. There are two specific designs: the use of three floating strips to enhance spatial resolution without increasing the number of electronic channels, and a configuration of large bias resistors and aluminum readout strips to ensure a large sensitive area. These designs result in different regions of the SSD, as indicated in Fig. 2:

- **Region-A)** with three floating p strips, without bias resistors
- **Region-B)** with three floating p strips and their bias resistors located between two aluminum readout strips
- **Region-C)** without floating p strips, with bias resistors for p readout strips

A p strip AC-coupled to an aluminum readout strip is referred to as the readout strip, while the strips located between two readout strips are called floating strips. In the SSD, which consists of 4095 p strips with a pitch of 27.25 µm,

one out of every four p strips is a readout strip. There are three floating strips between adjacent readout strips. These floating strips facilitate charge sharing to readout strips, thereby enhancing spatial resolution [18]. The impact of floating strips is quantitatively studied by comparing the performance between Region-C and Region-A.

In a ladder, aluminum readout strips of the N (N = 8, 10, 12) SSDs are connected in series along the strip direction, forming a parallel connection between the SSDs. Consequently, the coupling capacitors and bias resistors are connected in parallel. This arrangement leads to the coupling capacitance (bias resistance) increasing (decreasing) by a factor of N. Since the coupling capacitance cannot easily be adjusted during SSD fabrication by HPK, the SSDs must incorporate a bias resistance that is N^2 100 times larger than the typical value in order to achieve proper impedance matching.

For a conventional SSD, the bias resistance is O(1) MΩ, implemented using a polysilicon resistor that occupies approximately 100 µm in length at the end of the aluminum readout strip [19–22]. In this SSD design, the O(100) MΩ bias resistor would occupy a length of O(10) mm. Placing it directly behind the aluminum readout strips would lead to a bonding wire of about 14 mm in length, which poses a potential risk of short-circuit. Therefore, a specialized bias resistor configuration was designed, as illustrated in Fig. 2. The bias resistors for the three floating strips are inserted between two aluminum readout strips, allowing the bonding pads to be placed at the left end of the aluminum strips. On the right end, the bias resistors of the readout strips occupy that space solely, requiring only 2.9 mm in length. Thus, the length of bonding wires between two SSDs is reduced to about 5 mm.

The bias resistors between two aluminum readout strips could potentially influence their AC coupling or distort the internal electric field. Therefore, we carried out studies to compare the performance between regions with (Region-B) and without (Region-A) the bias resistors.

III. BEAM TEST SETUP

The beam test described in this work was conducted in May 2024 at the Super Proton Synchrotron (SPS) at CERN. We performed the beam test behind the dumper of beam line H6. The beam mostly consisted of muons with momentum in the tens of GeV, generated by the proton beam striking the dumper, thus behaving as minimum ionizing particles (MIPs).

We designed the single SSD frame board as shown in Fig. 3 FIGURE:3. The gray rectangle in the middle is the SSD, which is wire-bonded to 16 front-end readout chips (IDE1140) [23] on the right, resulting in a total of 1024 channels. Each channel has a gain of 2.6 µA/fC and a peaking time for positive signals of 8.5 µs. The output signals from IDE1140 are amplified in two stages with a gain of 6.97 µA/fC and then routed to a 14-bit analog-to-digital converter

(ADC) with a maximum input of 4096 mV. The data are then encoded by a field-programmable gate array (FPGA) and transmitted to the back-end.

The beam monitor was constructed by several layers of single SSD frame boards, as depicted in the right panel of Fig. 3(b). The frame board is designed with 90-degree rotational symmetry, allowing flexible orientation combinations for the layers. For layers with strips along the vertical (horizontal) direction, the hit position in the X (Y) coordinate can be measured, denoted as X-layer (Y-layer). In this beam test, we arranged 5 X-layers and 5 Y-layers, as illustrated in Fig. 4 [FIGURE:4], with the indicated detector under test (DUT) and the telescope. Scintillator detectors (140×80 mm^2) [24] were deployed to generate trigger signals, forming a trigger region that fully covered the DUT along the strip direction. This arrangement enabled performance evaluation of the DUT across Regions A, B, and C.

IV. DATA ANALYSIS

A. Raw Data Processing

The raw ADC value of each channel has four components:

$$ADC_j^i = Ped_i + CN_j^i + Noise_j^i + S_j^i$$

where i and j are the channel number and event number, respectively. The Ped_i is the pedestal of channel i, defined as the average value in the absence of particle incidence. Bias voltage fluctuation would cause an overall fluctuation of all channels, named common mode noise (CN) [25]. The single event $Noise_j^i$ is a random noise resulting from combining SSD and electronic noise, whose absolute value cannot be obtained, though the noise level of the channel i ($Noise_i$) can be calculated as the standard deviation of ADC values after CN is subtracted. The noise level of one channel is about 3 Least Significant Bits (LSB), which corresponds to Equivalent Noise Charge (ENC) 240 e . Finally, S_j^i is the signal introduced by the incident particle.

The pedestal and noise level are determined through a one-minute calibration run conducted every hour during the beam test. For each event, CN is calculated by:

$$CN_j = \frac{1}{N_a} \sum_i (ADC_j^i - Ped_i)$$

where N_a is the number of valid channels on the ath IDE1140. Noisy channels ($Noise_i > 10$ LSB) and the fired channels ($ADC_j^i - Ped_i > 10$ LSB) are not used in the CN calculation.

Subsequently, for the data-taking run, we calculate the signal of channel i of event j:

$$S_j^i = ADC_j^i - Ped_i - CN_j$$

Then a cluster is identified by a channel where $S_j^i > th_{seed} \cdot Noise_i$. The cluster expands on both sides until the value of channel x satisfies $S_j^x < th_{side} \cdot Noise_x$. In this study, $th_{seed} = 3.5$ and $th_{side} = 2.0$ are chosen to reduce noise influence while maintaining detection efficiency.

B. Double- Position Finding Algorithm

For SSDs under normal incidence, the particle impact position is typically reconstructed from the top few channels with the highest values in a cluster. Numerous studies have shown that the algorithm [18, 26–28] is a proper position finding algorithm for this purpose. This algorithm reconstructs the particle impact position by using the two adjacent channels with the highest values in a cluster. Denote S_L (S_R) as the value of the left (right) channel, and x_L (x_R) as the position of the readout strip corresponding to the left (right) channel. Define the variable η:

$$\eta = \frac{S_L}{S_L + S_R}$$

The particle impact position x_η follows a function of η:

$$x_\eta = x_L + P \cdot f(\eta)$$

where P is the readout strip pitch, and $f(\eta)$ is the cumulative distribution function (CDF) of η:

$$f(\eta) = \int_0^\eta \phi(\eta')d\eta'$$

where $\phi(\eta)$ is the probability density function (PDF) of η, which can be estimated from test beam data.

An issue arises when this algorithm is applied to the SSD, which exhibits significant charge sharing. For incidents near one readout strip, the two adjacent readout strips often share similar signals. Under the influence of random noise, the second-highest strip may be incorrectly identified. In these instances, choosing the two highest strips for position reconstruction can lead to a flip across the central strip, causing a larger position error. To address this issue, we propose an iterative position finding method, namely the "double- algorithm" :

1. Pick the channel with the highest value in a cluster as the first channel. Among its two neighboring channels, the one with the larger value is denoted as the second channel, and the other as the third channel.

2. Use the first and second (third) channels to calculate two η values according to Eq. 5, denoted as η_{12} (η_{13}). Estimate two impact positions using Eq. 6, denoted as x_{12} (x_{13}).
3. Use x_{12} of all layers to reconstruct the initial trajectory.
4. For each layer, compare the residual of x_{12} and x_{13} to the initial trajectory, select the smaller one as $x^{\star}$. Use $x^{\star}$ of all layers for final track reconstruction.

The spatial resolution comparison between this algorithm and the traditional algorithm is discussed in Sec. V C 1.

C. Track Reconstruction

Due to multiple particle incidences or electronic noise fluctuations, a detector layer might have two or more clusters in a single event. In this beam test, approximately 10% of events contained two or more clusters. For these events, we evaluated all possible trajectory combinations and selected the one with the lowest χ^2 value.

Track fitting is performed using the General Broken Lines (GBL) algorithm [29], widely employed in experiments such as AMS-02 [30] and CMS [31]. GBL is capable of accurately accounting for multiple scattering effects. Additionally, GBL provides a comprehensive covariance matrix for all track parameters upon refitting, making it especially advantageous for calibration and alignment tasks when integrated with Millepede II [32], which is a global parameter optimization tool designed to efficiently handle up to approximately one hundred thousand global parameters.

Detector alignment is performed using 1% of the collected data. Subsequently, track fitting is carried out for all events that used telescope layers. Following this procedure, more than 10 million tracks with precise hit information were reconstructed for analyzing the performance of the DUT.

V. PERFORMANCE OF THE SSD

We studied the impact of the SSD designs by comparing performance across different regions, with a primary focus on charge collection and sharing performance, detection efficiency, and spatial resolution.

A. Charge Sharing and Charge Collection

Charge sharing refers to the phenomenon where a single particle incident induces signals on multiple readout channels. The sharing is primarily due to capacitive coupling between neighboring strips and carrier diffusion. The charge sharing effect can be quantified by the number of channels within a cluster, referred to as the cluster size. The right panel of Fig. 5 [FIGURE:5] shows the variation of cluster size along the strip direction. The average cluster size is 2.03 for Region-

A and 1.38 for Region-C, indicating the enhancement of charge sharing by the floating strips.

Additional information can be gained by investigating the cluster size as a function of the relative position between two readout strips. For each track, the hit position inner strip is defined to be the position at the DUT mapped onto the range from [-54.5, 54.5], where -54.5 is the center of the nth strip, and 54.5 is the center of the (n+1)th strip. The fraction of different cluster sizes as a function of hit position inner strip is shown in Fig. 6 [FIGURE:6] for Region-A and Region-C. When floating strips are present, if the hit positions are slightly offset from the readout strips, there is a rapid increase in the fraction of clusters with size 2. Conversely, in areas without floating strips, clusters of size 2 become dominant only when the hit occurs near the midpoint between two adjacent readout strips. This further underlines the role of floating strips in enhancing charge sharing.

The impact of bias resistors for charge sharing located between two aluminum readout strips can be evaluated by comparing Region-B and Region-A. The magnified plot in Fig. 5 illustrates that the cluster size in Region-B is about 1% larger than that in Region-A. This indicates that the presence of bias resistors leads to a few percent increase in charge sharing between aluminum readout strips, possibly due to the additional equivalent capacitance introduced by the polysilicon.

The variable η also serves as an effective indicator of the degree of charge sharing. An η value close to 0 or 1 indicates that most of the signal is collected by a single readout channel, while a value near 0.5 implies substantial sharing between two adjacent readout channels. Fig. 7 [FIGURE:7] shows a comparison of the η distributions between regions with and without three floating strips. It can be seen that in the region without floating strips, two prominent peaks appear near $\eta = 0$ and $\eta = 1$. In contrast, the presence of three floating strips introduces three additional peaks in the η distribution. These peaks indicate that a specific fraction of charges is shared with the neighboring readout strip with the help of floating strips.

While enhancing charge sharing, the presence of floating strips leads to a reduction in charge collection efficiency (CCE) due to capacitive coupling to backplane, signal loss through bias resistor, etc. [19]. As the absolute CCE cannot be determined directly, the most probable value (MPV) of a cluster signal is used to represent the relative CCE across different regions. By binning the particle incident position along strips in steps of 500 µm, the MPV was determined by fitting each bin with a Landau function convoluted with a double Gaussian function as shown in Fig. 8 [FIGURE:8]. Fig. 9 [FIGURE:9] illustrates how the MPVs change along the strip direction. From left to right, the MPV gradually rises from 45 LSB to 46 LSB, likely due to the closer proximity to the readout chip. Upon reaching Region-C, the MPV suddenly increases to 65 LSB, reflecting a notable improvement in CCE once the three floating strips are no longer present. While the three floating strips reduce the MPV, the SSD maintains a

high detection efficiency due to the low noise level (3 LSB), as detailed in Sec. V B.

B. Detection Efficiency

In this study, detection efficiency refers to the ability of the DUT to detect MIPs. It is one of the essential performance metrics for silicon detectors, evaluated through the following procedure: (1) the telescope predicts a hit position x_{pred} of a track on the DUT plane; (2) the DUT then searches for a cluster within a window of $x_{pred} \pm 109$ µm; (3) if a cluster is found, the track is considered to have been successfully detected by the DUT. Based on this, the efficiency along the strip is analyzed to determine the total sensitive area, and the relationship between detection efficiency and the hit position between two readout strips (hit position inner strip) is then investigated.

Owing to the large telescope coverage, tracks spanning the full length of the SSD along the strip direction can be reconstructed. Fig. 10 [FIGURE:10] shows the detection efficiency along the strip direction. The detection efficiency remains close to 1 across the entire SSD (total efficiency = 99.8%), with the detector edges clearly delineated. This indicates that: (1) the bias resistors located between two aluminum readout strips did not affect the efficiency; (2) the introduction of three floating strips does not lead to a reduction in detection efficiency.

The detection efficiency versus inner strip hit position for different regions is shown in Fig. 11 [FIGURE:11]. All regions exhibit the highest detection efficiency near the two readout strips and the lowest in the middle, which is consistent with the charge collection behavior of the SSD. For Region-A and Region-B, the efficiency decreases gradually from the readout strip to the first floating strip but drops more rapidly after crossing the first floating strip. For Region-C, with no floating strips, the efficiency remains relatively stable over a wider range, with only a small drop in the central range. Generally, the total detection efficiency of all three regions is 99.8%.

C. Spatial Resolution

Spatial resolution is another key performance metric of silicon tracking detectors, determined by both the detector hardware and the reconstruction algorithm. In the following, we first present the effect of the double- algorithm and then evaluate the improvements introduced by the three floating strips.

The measured unbiased resolution (σ_{mea}) is defined as the standard deviation of the difference between the position reconstructed by the DUT and the telescope prediction. It comprises two components:

$$\sigma_{mea} = \sqrt{\sigma_{dut}^2 + \sigma_{tele}^2}$$

where σ_{dut} is the intrinsic spatial resolution of the DUT and σ_{tele} is the resolution of the telescope. Assuming each layer has the same intrinsic spatial resolution, the telescope' s contribution can be readily subtracted [33], giving $\sigma_{dut} = 0.89\sigma_{mea}$ in our beam test setup.

1. Effect of the Double- Algorithm The measured residual distributions for Region-A obtained using the algorithm and the double- algorithm are shown in Fig. 12 FIGURE:12 and (c), respectively. The first exhibits a broader distribution with pronounced tails on both sides. Meanwhile, in the two-dimensional distribution of measured residual versus inner strip hit position shown in Fig. 12(c), a clear Z-shape is observed, with the two horns contributing to the tails in Fig. 12(a). These events correspond to the "swapping phenomenon" discussed in Sec. IV B.

After applying the correction using the double- algorithm, the Z-shaped structure disappears, as shown in Fig. 12(d). As a result, σ_{mea} was optimized from 10.6 µm to 8.1 µm, and the intrinsic σ_{dut} improves from 9.4 µm to 7.2 µm. All spatial resolution results discussed below are obtained using the double- algorithm.

2. Improvement from the Three Floating Strips The measured residual distribution with and without the three floating strips is shown in Fig. 13 FIGURE:13 and (c). The three floating strips significantly improve σ_{mea} from 17.2 µm to 8.1 µm (σ_{dut} from 15.2 µm to 7.2 µm). This enhancement is primarily due to the larger charge sharing effect introduced by the floating strips. This can also be demonstrated by comparing the η distributions in the two regions as shown in Fig. 7(a) and (c). The three floating strips lead to a flatter η distribution, indicating increased sensitivity of the η value to the inner strip hit position. As a result, the function $f(\eta)$ becomes closer to the linear function ($f(\eta) = \eta$), as shown in Fig. 7(b) and (d), which leads to better spatial resolution [18]. In addition, Fig. 13(b) shows the same plot of the residual in Region-B. The σ_{mea} (σ_{dut}) of this region is 8.1 µm (7.2 µm), indicating that placing bias resistors between two aluminum readout strips does not affect the spatial resolution.

Eventually, by area-weighting the three regions, the overall spatial resolution of the SSD is 7.6 µm for MIPs.

VI. SUMMARY

We have designed an SSD for large-area, power-limited applications and performed a detailed performance characterization for a single sensor by beam test. Introducing three floating strips and inserting their bias resistors between two aluminum readout strips are the distinctive designs of this SSD. Our study shows that the three floating strips significantly enhance the charge sharing effect, which improved spatial resolution from 15.2 µm to 7.2 µm without com-

promising detection efficiency. The presence of bias resistors between two aluminum strips does not degrade the spatial resolution or detection efficiency in the corresponding region. As a result, the SSD achieves an overall efficiency of 99.8% and spatial resolution of 7.6 µm for MIPs. During this study, a double-algorithm for hit position reconstruction was developed to suit this SSD. The SSD from this design has been successfully applied in the AMS Layer-0 tracker upgrade, and the design principles can be utilized for future silicon detectors in space-borne cosmic ray experiments.

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