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Full Text

Preamble

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Design of Readout and Characterization System for Multi-pixel Superconducting Terahertz MKIDs

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Abstract

We propose a design for a microwave superconducting kinetic inductance detector (MKID) array readout system that characterizes MKID performance through a digital homodyne frequency mixing architecture. The readout system is implemented using a frequency division multiplexing circuit system, coupled with an FFT design to enable the readout of MKID arrays. The system is characterized by its compact size, low cost, portability, and ease of further development. These features have significant implications for the design and readout of terahertz MKID arrays, while simultaneously advancing both the theoretical and practical aspects of MKID technology.

Key words: Astronomical Instrumentation, Methods and Techniques –instrumentation: detectors –methods: observational

1. Introduction

Microwave superconducting kinetic inductance detectors (MKIDs; Day et al. 2003) are vital for astronomical observations due to their high sensitivity and broad wavelength detection capabilities, spanning from ultraviolet to infrared. These detectors are commonly used in large telescope arrays to study cosmic phenomena, such as the cosmic microwave background, exoplanet atmospheres, and distant galaxies (Fruitwala 2021). In optical and infrared observations on telescopes, MKIDs facilitate the detection of faint objects and enable precise photon counting with minimal noise (Meeker et al. 2018). Furthermore, MKIDs have played a critical role in millimeter and submillimeter astronomy, contributing significantly to the study of cold cosmic structures, including interstellar dust and molecular clouds. Many MKID telescopes, such as ARCONS (Mazin et al. 2010), KISS (Macías-Pérez et al. 2024), and SOFIA (Pipher et al. 2021), are set to be deployed or are already conducting observations. These instruments are poised to provide significant scientific support in the field of astronomy, offering a more advanced platform for future observations.

After the fabrication of MKID chips, it is necessary to characterize their performance in order to measure and calibrate key parameters, such as the equivalent noise power, resonance characteristics, quality factor, saturation power, and linear operating range of the detector (Mazin et al. 2006). Meanwhile, multi-pixel array MKIDs need to observe astronomical signals, which require readout at room temperature. This necessitates devices capable of generating arbitrary frequency combs on a transmission line, along with systems for collecting and

processing the readout signals using fast Fourier transforms (FFTs) to enable the readout functionality of the multi-pixel array MKIDs (McHugh et al. 2012).

Generally, two separate systems are typically required to complete the performance characterization and room-temperature readout of MKIDs. Traditional systems tend to be large in size, consume significant power, and come with a high cost. Additionally, there are substantial differences in the programming and communication formats between the various components, making it challenging to integrate calibration algorithms into the intermediate processes. Commercially available measurement and signal generation tools, such as vector network analyzers, spectrum analyzers, and arbitrary waveform generators, cannot directly incorporate these calibration algorithms, resulting in limited operational flexibility.

We propose an integrated development board based on ZYNQ7020 (FPGA+ARM) and AD9361, which implements MKID performance characterization and room-temperature readout on a single platform. This approach effectively addresses the aforementioned challenges, providing a better performance characterization and readout platform for the development of MKID arrays.

2. Principle of MKIDs

The detection principle of MKIDs (Day et al. 2003) is illustrated in Figure 1 [Figure 1: see original paper]. Incident photons, serving as detection signals, interact with the superconducting thin film on the surface of the MKIDs. When the photon energy exceeds twice the superconducting energy gap, Cooper pairs within the superconducting material are broken, generating quasiparticles and releasing phonons. This increase in quasiparticle density modifies the dynamic inductance and surface impedance of the superconducting resonator, leading to a leftward shift in its resonant frequency and a reduction in its quality factor (Q). By analyzing the variations in the transmission properties of a superconducting transmission line coupled to the resonator, changes in the resonant frequency and phase can be precisely characterized. These variations enable the determination of the energy of incident photons, facilitating signal detection through the translation of physical property relationships.

3. Design of MKID Readout and Characterization System

The design employs the ZYNQ7020+AD9361 development board, which integrates a programmable logic (PL) FPGA and a dual-core ARM Cortex-A9 system-on-chip as shown in Figure 2 [Figure 2: see original paper]. This combination enables the seamless implementation of signal processing algorithms in the FPGA while ARM cores handle high-level control and communication tasks. The AD9361 provides a highly configurable RF front end for transmitting and receiving signals. The integration of FPGA and ARM enhances flexibility, computational efficiency, and real-time data processing, as shown in Figure 3

[Figure 3: see original paper]. Additionally, the compact design reduces system size, power consumption, and cost, making it ideal for MKID performance characterization and readout in complex astronomical applications.

As shown in the figure, the ZYNQ7020+AD9361 integrated development board has a compact size of only 50 mm × 100 mm, with a power consumption not exceeding 5 W. It offers a 2 × 2 MIMO configuration with a working bandwidth ranging from 70 to 6000 MHz. The DAC and ADC sampling rates can reach up to 61.44 Msamples s^{-1}. The board also features a built-in 70 dB adjustable amplifier and is equipped with a 1000 Mbps Ethernet port, a general-purpose UART serial interface, and an OTG interface.

3.1. Design of Homodyne Mixing System

Based on the AD9361 transceiver, Xilinx FPGA, and DSP IP cores, an efficient digital zero IF mixing system is designed. The system generates two synchronized signals through the 2 × 2 MIMO configuration of the AD9361 DAC. The AD9361 ADC then collects IQ signals, which are processed using the Xilinx DSP core for digital mixing. An FIR filter module is used to remove high-frequency components, achieving precise digital homodyne mixing, as shown in Figure 7 [Figure 7: see original paper].

The system first generates two signals TX1 and TX2 using the AD9361 DAC in 2 × 2 MIMO configuration. These signals are precisely synchronized in frequency (f_0), phase (ϕ_0), and amplitude (A_0) to ensure consistency across different channels. This synchronization is crucial for accurate and stable mixing. Two signals TX1 and TX2 are expressed in the formula in Equation (1).

$$TX1 = A_0 \sin(2\pi f_0 t + \phi_0)$$
$$TX2 = A_0 \sin(2\pi f_0 t + \phi_0)$$

The AD9361 ADC captures synchronized signals RX1 and RX2 in a 2 × 2 MIMO configuration. The ADC supports a sampling rate of up to 61.44 MSPS. To ensure signal quality, the signals are down-converted to a baseband frequency of 50 MSPS using the built-in mixer in the AD9361, preparing them for digital processing. The captured RX1 and RX2 data sequences are divided into I_{RX1}, Q_{RX1}, I_{RX2}, and Q_{RX2}. In theory, I_{RX1} and I_{RX2} are identical signals, Q_{RX1} and Q_{RX2} are also identical, while I_{RX1} and Q_{RX1} have a phase difference of 90°, and I_{RX2} and Q_{RX2} also have a phase difference of 90°.

After downconversion, the signals (I_{RX1}, Q_{RX1}, I_{RX2}, and Q_{RX2}) are transmitted to the Zynq SoC' s DDR via the high-performance (HP) bus using DMA technology, allowing for efficient, low-latency data transfer and minimizing the processor load. DMA refers to a technology that allows external devices to directly access the computer' s memory without involving the CPU in the data transfer process, improving data transfer efficiency and reducing CPU load. The

HP bus refers to High-Performance Bus, the high-speed data bus between the PL and Processing System (PS) of the ZYNQ7020 chip.

Digital homodyne mixing is achieved through the DSP core and DMA control as illustrated in Figure 7. By selecting the IQ signal RX1(I_{RX1}, Q_{RX1}) and the I signal from RX2(I_{RX2}), the signals undergo digital homodyne mixing to generate difference and sum frequencies, as described in Equation (2). I_{mix} and Q_{mix} are the IQ sequences after digital homodyne mixing.

$$I_{mix} = I_{RX1} \times I_{RX2}$$
$$Q_{mix} = Q_{RX1} \times I_{RX2}$$

As demonstrated in Figures 4 and 5, the frequency spectrum of RX1 and RX2 is obtained. After homodyne mixing in the system, the signals $f_0 - f_0$ and $f_0 + f_0$ are the Zero-IF signal and the Co-frequency combined signal, respectively.

A 21st-order FIR low-pass filter was implemented using the Xilinx FIR Compiler IP core to remove high-frequency noise and ensure the phase linearity of the mixed signal. The filter was designed using MATLAB' s FIR design tool and integrated into the system via DMA for efficient processing. The LPF has a passband of 4 MHz, a cutoff frequency of 5 MHz, and 80 dB of suppression. As shown in Figure 5, by performing data decimation on the 50 MSPS sampled sequence, different effective sampling rates are achieved. In Figure 6, it can be seen that the signals above 4 MHz are effectively suppressed by the LPF, and the high-frequency components of the mixed signal are filtered out, leaving the zero-IF signal intact. The zero-IF mixing and LPF design are validated successfully.

This system combines AD9361, mixing function, Xilinx FPGA DSP cores, and FIR filter modules, achieving an efficient and accurate digital zero IF mixing system. Key advantages include high synchronization and precision, efficient data transfer, digital mixing and filtering, and flexibility for different frequency and bandwidth requirements.

3.2. Design of MKID Readout System

The system uses the Xilinx Zynq7020 SoC with an ARM Cortex-A9 processor, DDR memory, DMA controller, and AD9361 transceiver to generate a frequency comb for readout. By DDS technology, the system precisely generates and modulates multiple frequency signals, mapping them to different frequency bands. DDS offers highly flexible frequency synthesis, enabling signal generation with adjustable phase and frequency across various bands. The AD9361 transceiver converts these digital signals into RF signals for transmission via the RF front end.

After the upper-level machine determines the required frequency points $(f_0, f_1, ..., f_n)$, the amplitude corresponding to each frequency point

$(A_1, A_2, ..., A_n)$, and the phase $(\Phi_1, \Phi_2, ..., \Phi_n)$, the ARM Cortex-A9 chip calculates the FDM sequences $I(t)$ and $Q(t)$ using Equation (3). Subsequently, the sequences are scaled (to match the 12-bit DAC value range), quantized to the 12-bit range, and then combined. The combined sequences are transferred to DDR memory via DMA. The DAC generates the local oscillator signal based on a 100 MHz reference frequency and mixes it with the sequence data transferred from DDR via DMA. The result is a frequency comb corresponding to the upconverted frequencies, as diagrammed in Figure 9.

$$I(t) = \sum_{i=1}^{n} A_i \sin(2\pi f_i t + \Phi_i) Q(t) = \sum_{i=1}^{n} A_i \cos(2\pi f_i t + \Phi_i)$$

The system employs a Frequency Division Multiplexing (FDM) system using Direct Digital Synthesis (DDS) technology. The ARM processor calculates the FDM signal sequences, storing the frequency values in DDR memory. The frequency sequence is then transmitted using the HP bus and DMA, enabling efficient data transfer. DMA allows seamless access to the frequency data in memory, avoiding bottlenecks and ensuring fast, efficient data flow to the AD9361 control unit for further processing, as illustrated in Figure 8.

Using the 12-bit differential ADC functionality of the AD9361 transceiver, the system captures RF signals and stores the acquired data in DDR memory via the high-speed HP bus. Coupled with Xilinx' s FFT core, this design enables efficient FFT processing for high-resolution frequency-domain analysis. The 12-bit differential ADC channels of the AD9361 are used to collect RF signals. To ensure efficient data transfer, the HP bus and DMA controller in the Zynq7020 SoC are employed to transmit the captured ADC data from the AD9361 to DDR memory. The use of the DMA controller reduces the processing load on the ARM processor, enabling high-speed, large-capacity data transfer. The DDR memory serves as an intermediate storage medium, ensuring that the captured data are quickly stored and ready for subsequent processing.

After the data captured by ADC are stored in DDR, the sampled data undergo FFT processing using Xilinx' s FFT core inside the Zynq7020. The FFT core is a hardware accelerator that significantly enhances FFT computation speed and performance, supporting FFT transformations of various sizes, including 2048, 4096, 8192, and 16384 points.

3.3. Design of Overall System and Upper-level System

The overall system is designed using the Xilinx Zynq-7020 SoC and AD9361 transceiver, implementing an efficient hardware architecture. The ARM Cortex-A9 core handles computation and system control, while the FPGA processes algorithms, low-level drivers, and hardware interfaces. Communication with the upper-level machine is achieved via UART for command control and status

exchange, and lwIP provides a Gigabit Ethernet interface for high-speed data transmission, as illustrated in Figure 10.

The Zynq7020 integrates an ARM Cortex-A9 processor and FPGA, with the ARM processor managing control tasks and data processing, and the FPGA handling real-time signal processing and hardware control. The AD9361 transceiver offers a wide frequency range (70 MHz–6 GHz) and performs operations like frequency conversion and modulation. Communication with the upper-level machine is through UART for low-speed control and lwIP for high-speed Ethernet communication, supporting data exchange and remote control. The system is designed for high flexibility, leveraging the ARM and FPGA collaboration to optimize performance. The FPGA enables real-time signal processing with low latency, while the ARM processor manages complex tasks. Integration with Zynq-7020 reduces hardware complexity and costs, and the wide frequency support of AD9361 simplifies the design. This system offers high performance, scalability, and flexibility for various applications.

The Upper-Level System integrates the Zynq-7020 and AD9361-based hardware with the MATLAB App Designer-designed upper-level machine to provide an efficient and user-friendly data processing and visualization solution, as depicted in Figure 11. The upper-level machine communicates with the lower-level machine via UART for command transmission and UDP for data packet exchange, supporting real-time interaction, data visualization, and processing. MATLAB App Designer offers a platform for designing intuitive user interfaces, enabling real-time signal monitoring, data analysis, and control of the lower-level machine. The system' s dual communication modes (UART and UDP) ensure efficient data transfer and real-time operation, meeting the performance and interaction needs of modern communication and signal processing applications.

4. Result

To achieve the superconducting transition temperature of the materials used for the MKID chip, we employ a cryogenic platform capable of providing an ultra-low-temperature environment down to 50 mK, ensuring the proper operation of the MKID detector. As shown in Figure 12, the schematic diagram of the MKID testing system illustrates the signal chain. The MKID array is mounted at the center of a specially designed block, which is installed below the mK cold plate of the cryocooler (dewar). Devices at various cooling stages are arranged as depicted in the schematic. A dedicated testing platform is utilized for characterizing the MKIDs and reading out their signals.

It can be observed that the PS section consumes a total of 1.56 W, while the PL section consumes 0.24 W, from Table 1. The remaining power is attributed to the AD9361 driver, I/O interfaces, clocks, and other components. The total power consumption of the ZYNQ7020+AD9361 board is only 3.51 W, achieving low-power operation for room-temperature readout. This significantly reduces the power demand of the room-temperature readout section in astronomical

observation platforms.

We verified the system' s capability to characterize the performance of MKIDs by testing various parameters (the specific calculation methods and formulas for parameters can be found in Zhang et al. 2024), including the transmission characteristics (S21 parameter), input saturation power, amplitude and phase noise (PSD, Power Spectral Density), responsivity, and noise-equivalent power (NEP), as shown in Figures 13, 14, 15, 16, 17 and 18.

At a temperature of 80 mK, the resonance depth of MKIDs is 35 dB. As the detection signal power (temperature) increases, the resonance shifts to the left, and the quality factor Q increases. After fitting, the dA/dT of MKIDs is found to be 1.3 (1/K). The saturation power of MKIDs is -80 dBm, and the NEP is approximately $10^{-18}\mathrm{W/Hz}^{1/2}$. The measurement results were satisfactory, effectively demonstrating the reliability and feasibility of the testing system.

Next, we validated the system' s ability to read out MKIDs. We generated 10 frequency comb signals within a 50 MHz bandwidth, each corresponding to a resonance frequency of the MKIDs on a transmission line. After processing by the system, the resulting spectrogram was transmitted back to the host computer, as displayed in Figure 19. The obtained results demonstrate the capability of the system to fulfill the readout requirements of the MKIDs, thereby affirming the functionality of this part of the system.

5. Conclusion

The integrated system based on ZYNQ (FPGA+ARM) and AD9361 provides an efficient solution for MKID performance characterization and room-temperature readout. By integrating these functions on a single platform, this approach addresses the challenges posed by traditional systems, such as large size, high power consumption, and limited operational flexibility. The system eliminates the need for multi-devices, enabling precise measurement and calibration of key parameters. Furthermore, the system facilitates multi-pixel array MKID readout by generating arbitrary frequency combs and processing signals using FFTs. This solution supports the advancement of MKID array development, offering a more compact and flexible platform for future astronomical observations.

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Note: Figure translations are in progress. See original paper for figures.