Performance study of a prototype readout electronics for the time-of-flight detectors of HIAF-HFRS facility

Authors: Wen, Mr. Shihai, Mr. She Qianshun, Kong, Dr. Jie, Wang, Dr. Kailong, An, Mr. YiLang, Yang, Mr. Zuoqiao, Yan, Dr. Jun-Wei, Dr. Yi Qian, Yu, Dr. Yuhong, Dr. Guangshun Li, Sun, Prof. Zhiyu 孙志宇, Kong, Dr. Jie

Date: 2025-04-25T00:00:00+00:00

Abstract

In the High Energy FRagment Separator (HFRS) at the High Intensity heavy-ion Accelerator Facility (HIAF), plastic scintillation detectors are used for high-precision time-of-flight (ToF) measurements to identify the secondary ions from the reaction between the primary beam and the target. During the day-one experiments, the readout electronics for the ToF detectors is required to achieve a time resolution of 40 ps with a single-channel counting rate up to 10^6 counts per second (cps). This study presents a prototype readout electronics for plastic scintillation ToF detectors, the system comprises a constant-fraction discriminator (ORTEC Model-935), a level conversion board, and a time digitization board. We developed an octal logic signal adapter to convert NIM signals into LVDS differential signals. For time digitization, a Filed Programmable Gare Array (FPGA) is utilized through the internal tapped delay line (TDL). The performance of time resolution and counting rate of the electronics system is evaluated using a high-precision pulse generator and a picosecond pulsed laser. The test results indicate that the single-channel time resolution is around 10 ps, with a maximum counting rate of 1.6×10^6 cps. The overall average ToF resolution achieves 17.9 ps during the laser test at a repetition rate of 1 MHz. These results validate that the developed system meets the HFRS beamline' s requirements for ToF resolution and counting rate.

Full Text

Preamble

Performance Study of Prototype Readout Electronics for Time-of-Flight Detectors at the HIAF-HFRS Facility

Shi-Hai Wen,[1],[2] Qian-Shun She,[1],[2] Jie Kong,[1],[2],† Kai-Long Wang,[1],[2],‡ Yi-Lang An,[1],[2] Zuo-Qiao Yang,[1],[2] Jun-Wei Yan,[1],[2] Yi Qian,[1],[2] Yu-Hong Yu,[1],[2] Guang-Shun Li,[1],[2] and Zhi-Yu Sun[1],[2]

[1]Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China
[2]School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing 100049, China

In the High Energy Fragment Separator (HFRS) at the High Intensity Heavy-Ion Accelerator Facility (HIAF), plastic scintillation detectors are employed for high-precision time-of-flight (ToF) measurements to identify secondary ions produced in reactions between the primary beam and target. For the day-one experiments, the readout electronics for these ToF detectors must achieve a time resolution of 40 ps with a single-channel counting rate up to 10^6 counts per second (cps). This study presents a prototype readout electronics system for plastic scintillation ToF detectors, comprising a constant-fraction discriminator (ORTEC Model-935), a level conversion board, and a time digitization board. We developed an octal logic signal adapter to convert NIM signals into LVDS differential signals. For time digitization, a Field Programmable Gate Array (FPGA) is utilized through its internal tapped delay line (TDL). The system' s time resolution and counting rate performance were evaluated using a high-precision pulse generator and a picosecond pulsed laser. Test results indicate a single-channel time resolution of approximately 10 ps, with a maximum counting rate of 1.6×10^6 cps. The overall average ToF resolution reaches 17.9 ps during laser testing at a repetition rate of 1 MHz. These results validate that the developed system meets the HFRS beamline requirements for ToF resolution and counting rate.

Keywords: HIAF-HFRS, Plastic scintillation detectors, Time-of-flight (ToF), Time-to-digital converter (TDC), High counting rate, Trigger-less, Readout electronics

Introduction

Radioactive ion beam facilities have played a crucial role in exotic nuclear physics research for over three decades [1–3]. Among the primary techniques for producing and investigating exotic nuclei, in-flight separation stands out as particularly important [4]. Currently, several major laboratories worldwide operate in-flight separators, including BigRIPS at RIKEN-RIBF in Japan [5], ARIS at FRIB in the USA [6], FRS at GSI in Germany [7], and RIBLL at HIRFL in China [8, 9]. In the coming years, new state-of-the-art separators will become operational, such as Super-FRS at FAIR in Europe [10] and the High Energy Fragment Separator (HFRS) at the High Intensity Heavy-Ion Accelerator Facility (HIAF) in China [11, 12].

At HIAF-HFRS, numerous exotic nuclei far from the stability line can be produced, making accurate identification of each ion essential for subsequent exper-

iments. Typically, the ΔE-ToF-B technique is employed for particle identification, which simultaneously measures energy loss (ΔE), time-of-flight (ToF), and magnetic rigidity (B) to determine the proton number (Z) and mass-to-charge ratio (A/Q) of the ions [13, 14]. Simulations specific to the HFRS beamline indicate that achieving effective particle identification requires a ToF resolution of 40 picoseconds [12]. Furthermore, these simulations predict a maximum secondary beam intensity of approximately one million particles per second (pps). Consequently, a time-of-flight detector with superior timing performance and high-intensity beam handling capability is imperative for accurate ToF measurements.

Plastic scintillation detectors represent one of the most mature and widely used ToF detector technologies, offering high time resolution at relatively low cost. These advantages have led to their extensive deployment across various radioactive beam lines worldwide, including BigRIPS at RIKEN-RIBF [14], ARIS at FRIB [6], Super-FRS at FAIR [15], and RIBLL1 and RIBLL2 at HIRFL [16-18]. Given this established performance and reliability, plastic scintillation detectors are a prudent choice for the HFRS ToF detection system. A prototype plastic scintillation ToF detector for HFRS has been constructed and evaluated using conventional electronics consisting of Mesytec MCFD16 and MTDC32 modules [19], achieving a best ToF resolution of approximately 10 ps. However, due to inherent conversion and readout times, this commercial electronics system is limited in counting rate, with a maximum single-channel capacity of 700 kilo-counts per second (kcps). Additionally, the MTDC32 module requires an external trigger signal to operate.

In modern time measurement readout electronics, time-to-digital converters (TDCs) implemented using both application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs) are widely employed across various applications [20–23]. FPGA-based TDCs offer advantages of lower cost and higher flexibility, leading to their extensive use in time-of-flight measurements for nuclear physics experiments [20, 24–26]. According to recent reviews [20], the tapped delay line (TDL) architecture represents a mainstream TDC structure. Ultra-high time resolutions have been achieved using TDL-based TDCs on Xilinx Kintex-7 FPGA [27–29] and Xilinx Zynq Ultrascale+ FPGA [30, 31].

Recently, FPGA-based TDCs have been extensively deployed in various nuclear physics experiments. In the Cooling Storage Ring External-target Experiment (CEE) at the Heavy Ion Research Facility in Lanzhou (HIRFL), a ToF detector readout electronics prototype achieved an electronic time resolution better than 10 ps (root mean square, RMS) [25, 32]. The ToF system of the CBM experiment at FAIR achieved an electronic time resolution better than 20 ps using FPGA TDC technology [33]. The High Granular Neutron ToF detector (HGND) for the BM@N experiment developed a 100 ps TDC based on a Kintex 7 FPGA [34]. In the HL-2A tokamak device, a real-time double-ring neutron ToF spectrometer system achieved a time resolution of 52 ps based on FPGA TDC technology [35].

Building on these successful applications, we aim to design a readout electronics system based on FPGA for plastic scintillation ToF detectors capable of achieving an electronic time resolution better than 20 ps under counting rates up to 1 MHz per channel. The readout electronics comprises a constant-fraction discriminator (ORTEC Model-935), a level conversion board, and a time digitization board.

Structure of the Readout Electronics

As shown in Fig. 1 [Figure 1: see original paper], the readout electronics for plastic scintillation detectors consist of three main components: a constant-fraction discriminator (CFD), a logic level converter, and a time-to-digital converter (TDC). Analog negative signals from the detector photomultiplier tubes (PMTs) are sent to the CFD for timing, which generates fast negative logic signals conforming to the Nuclear Instrument Module (NIM) standard. To meet the requirements of high-precision and ultra-fast TDC, these logic signals are converted to Low-Voltage Differential Signaling (LVDS) standard by a NIM-to-LVDS level converter. The LVDS signals are subsequently transmitted to the TDC board for digitization and interfaced with the data acquisition (DAQ) system via either USB 3.0 cable or optical fiber.

For timing methodology, constant-fraction discrimination was selected to meet the stringent ToF resolution and counting rate requirements of the HFRS beamline. While a custom CFD addressing these demands is currently under development, this work employs a commercial unit—ORTEC Model-935 [36]—as a provisional solution. The Model-935 performs constant-fraction timing on fast signals as narrow as 1 ns, making it suitable for very fast detectors such as the plastic scintillators used at HFRS. The module' s maximum input rate reaches 200 MHz, which comfortably exceeds the HFRS requirement of over 1 MHz. Additionally, its input range from 0 to -10 V accommodates the relatively large signals from PMTs, ensuring compatibility with the ToF detectors.

The fast negative NIM output signals from the Model-935 are processed by the logic level converter and time-to-digital converter, which have been meticulously designed and manufactured. We have successfully developed a logic level conversion board for signal level translation and a time-digitization board for high-precision time measurement, whose specifications and functionalities are described in subsequent sections.

Design of the Logic Level Converter

The NIM-to-LVDS logic level conversion board is shown in Fig. 2 [Figure 2: see original paper]. The conversion process primarily comprises two stages: NIM signals are first converted to TTL signals, which are then transformed into LVDS differential signals featuring strong noise immunity and low power consumption [37]. The NIM signal from the constant-fraction timing discriminator is passed to a differential amplifier to generate an MECL signal, which is subsequently

converted into a TTL signal. The TTL signals are then converted into LVDS signals.

In the current design, we have implemented an 8-channel logic level converter board. The board' s specific parameters are detailed in Table 1 . It supports a maximum input rate of 20 Mbps per channel, with drivers compatible with NIM input standards and LVDS output standard compliance.

Table 1. Logic level converter board main parameters

Parameter	Value
Function	Logic Level Conversion
Number of channels	8
Input rate (single channel)	20 Mbps
Input standard	NIM
Output standard	LVDS

Design of the Time-to-Digital Converter

The TDC board we developed is shown in Fig. 3 [Figure 3: see original paper]. This board integrates a time-digitization module for precise time measurement and a data-transfer module for fast data transmission. To accommodate high-speed LVDS signals, we selected the DS25BR150 chip from Texas Instruments, which features an integrated 100-Ω termination resistor [38]. This configuration typically introduces random jitter of approximately 1 ps, contributing minimally to overall system time jitter. The LVDS signal, after being driven by a high-speed buffer, is sent into the High Range (HR) BANK of a Kintex-7 FPGA from AMD Xilinx, which is specifically designated for receiving and processing time-digitized signals.

A. High-Precision Time-Digitization Module

Dead time significantly impacts readout electronics performance at high counting rates. To effectively measure adjacent hit signals, TDCs must minimize the conversion time interval between successive hits, ideally approaching zero. In our high-precision time digitization board, all functional modules operate in a pipeline architecture with virtually zero dead time during data transfer. As shown in Fig. 4 [Figure 4: see original paper], the high-precision time digitization module is implemented using an FPGA-based TDC constructed with a time interpolation method [39]. In this design, a 500-MHz counter generates "coarse-time stamps" while intra-cycle subdivision produces "fine-time stamps" through delay line analysis. By combining coarse and fine time stamps, high measurement precision is achieved. The designed system consists of four main components: the coarse time counter module, the delay line module (latch arrays), the fine time encoding module, and the data storage FIFO arrays.

When the high-precision time measurement board is powered on, a 40 MHz clock on the board generates a 500 MHz TDC high-frequency clock and a 100 MHz system clock through a phase-locked loop (PLL). In this design, the TDC for each channel comprises a coarse counter, a 188-tap delay line, a D-type flip-flop (DFF) bank, a fine time encoder, and a data storage FIFO. Upon activation, the 44-bit coarse time counter array begins continuous sampling at 500 MHz. Meanwhile, the LVDS input signal is first sent to the trigger unit to generate a hit signal. This hit signal propagates through the delay line and is sampled by the D flip-flop array at the rising edge of the next clock cycle. After sampling, the delay line data is encoded by the encoding module, producing an 8-bit fine time. Finally, the combination of coarse time and fine time represents the timing information of the measured signal.

As shown in Fig. 5 [Figure 5: see original paper], our high-resolution TDC is constructed by cascading dedicated carry logic units on the Kintex-7 FPGA, which feature dedicated routing and minimal internal propagation delay. Multiple CARRY4 logic blocks build the delay line, with the carry outputs (CI, CO[3]) of CARRY4 units interconnected. The carry output of CARRY4 serves as the tap output. The TDL performs fine time measurement within intervals shorter than the coarse time (2 ns). The TDL is constructed from a cascade of 47 CARRY4 logic units to ensure the delay time exceeds one TDC clock cycle, meeting total delay time requirements. When no hit signal propagates through the delay line, the output is all “0”, meaning the raw position encoding sampled at the rising edge of the TDC clock is also all “0”. When the hit signal propagates through the delay line, areas not yet passed output “0”, while traversed areas output “1”. The corresponding CARRY4 logic unit’s CO transitions from “0” to “1”. At this point, the D flip-flop array samples the delay line, outputting a pattern like “···000011111···”, where the position of the 0-to-1 transition corresponds to the signal’s fine time of arrival within one clock cycle [40].

The encoder module converts the thermometer code sampled by the D-type flip-flop array into binary code through step-by-step calculation, summing the logical “1”values from the entire carry chain output and encoding them into 8-bit data. We currently employ the Wallace encoder, which reduces encoding errors caused by bubble errors. As shown in Fig. 6 [Figure 6: see original paper], the raw position encoding is first grouped into 6-bit sets. We use the 6-input LUT (LUT6) from the Kintex-7 FPGA’s underlying logic resources to convert the number of logical “1”s in each group into a 3-bit count output [41]. A 2-input adder then converts each group’s 3-bit count into 4-bit encoding. This process repeats multiple times using adders, ultimately producing 8-bit fine time data corresponding to the delay chain position output encoding.

The data storage FIFO array serves two purposes: first, it frames and packages coarse-time stamps, fine-time stamps, trigger counts, and other TDC data into the FIFO array, which is then read out from different channels according to backend data transmission module instructions. Second, since the TDC module

operates at a high-frequency 500 MHz clock while the backend data processing and transmission module uses a 100 MHz clock, the FIFO array isolates clock domains and prevents timing issues.

B. Ultra-Fast Data-Transfer Module

Our high-precision time measurement electronics system operates in triggerless mode, meaning it does not rely on trigger signal presence to determine operating state. Upon detecting an input LVDS signal (NIM-TTL-LVDS), the entire TDC module performs time information measurement. Given that the plastic scintillation ToF detector readout electronics system must operate at high count rates of 1 Msps, rapid data transmission is crucial to prevent TDC data loss from slow transmission speeds.

As shown in Fig. 7 [Figure 7: see original paper], after passing through the level conversion board, LVDS differential signals are sequentially sent to the TDC module for time measurement. TDC data from all channels are first individually framed and stored in a first-in-first-out (FIFO) array. The data readout control module manages TDC data in the FIFO array and handles clock domain crossing. This module first checks for TDC data presence in each FIFO, then reads TDC time data from different FIFOs.

To minimize time overhead during intermediate data transmission, a data splitting module is incorporated. This module serves two purposes: (1) Aggregating data and splitting it into 32-bit chunks for continuous transmission to the backend while simultaneously generating a data valid signal; (2) Avoiding direct data transfers from the high-frequency TDC clock domain to the system' s low-frequency clock domain.

In the data packaging module, split frontend data is aggregated and packaged. This module also performs high-low bit reversal. Finally, processed TDC data is uploaded to the server via the USB 3.0 module.

Test Results

We evaluated the readout electronics performance using a pulse generator and plastic scintillation detectors, with time resolution per channel as the primary assessment metric.

A. Calibration of the Delay Line

According to the TDC design, the arrival time of a signal to one channel is given by:

$$t = N_C \cdot T_{clk} - T_F$$

where N_C represents the number of clock periods T_{clk} (2 ns in this work), and T_F is the fine-delay time within one T_{clk}. This equation shows that the TDC

module's sub-nanosecond timing resolution is primarily determined by fine-delay time precision. T_F is determined by the delay time of each activated delay unit within the FPGA' s underlying logic resource, CARRY4. Typically, as FPGA manufacturing processes advance, delay per unit decreases, enhancing TDC resolution. However, variations in signal propagation times through the carry chain and clock jitter at clock distribution network edges can cause delay-tap width fluctuations [42]. To assess this delay chain nonlinearity, we performed code density tests to calibrate delay time using the bin-by-bin approach [43]. We first obtained the firing density distribution (d_j) of each delay unit, shown by the blue line in Fig. 8 [Figure 8: see original paper]. The fine-delay time until the ith unit is then calculated as:

$$T_{F,i} = T_{clk} \cdot \sum$$

as depicted by the red line in Fig. 8. By combining these equations, we obtain the signal arrival time.

B. Test with Pulse Generator

To evaluate the time resolution performance of our ToF detector readout electronics system and verify whether it meets HFRS beamline requirements, we conducted comprehensive tests. To accurately replicate real signals from plastic scintillation detectors, we utilized Tektronix' s ArbExpress software [44] to import detector signals originally captured by a Tektronix MSO54 oscilloscope. These waveforms were exported to a Tektronix AFG3252C pulse generator to produce simulated signals matching the original detector signal shape while allowing adjustable amplitude and frequency. Generated signals were sent through CFDs, the level converter, and TDC board, enabling measurement of time differences between every two channels.

Fig. 9 [Figure 9: see original paper] presents the time difference distribution between channel-6 and channel-2. The coincidence time resolution for this channel pair, represented by the sigma (σ) value of the fitted Gaussian function, is measured to be 12.5 ps. Similarly, we obtained coincidence time resolutions for seven other channel pairs. Subsequently, the time resolution for each individual channel was calculated and is illustrated in Fig. 10 [Figure 10: see original paper], with the average value around 10 ps.

Given that HFRS beamline ToF detectors must operate at high beam rates of 10^6 counts per second (cps), we evaluated the entire readout electronics system' s saturation characteristics. During testing, the pulse generator output signal was split eight ways using a power splitter, with eight channels of the readout electronics processing signals simultaneously to assess system performance under high-rate conditions. The pulse generator was configured to provide a fixed number of input signals (10^6 events) at different rates. We monitored and recorded the total output count, with results shown in Fig. 11 [Figure 11: see

original paper]. The system correctly captured all events without loss for input frequencies up to 1.6×10^6 cps. Beyond this rate, the system progressively failed to record all input events, indicating saturation onset. These results confirm that the readout electronics can meet the required count rate for plastic scintillation ToF detectors at the HFRS beamline.

C. Test with Plastic Scintillation Detectors

To further evaluate readout electronics performance for plastic scintillation ToF detectors, we conducted a joint test as shown in Fig. 12 [Figure 12: see original paper]. A PiL1-037-40 picosecond pulsed diode laser from NKT Photonics [45] served as the beam source, emitting laser pulses at 375 nm wavelength with repetition rates up to 40 MHz. Each scintillation detector consists of one thin plastic scintillator coupled to four photomultiplier tubes (PMTs). One scintillator is EJ-228 from Eljen Technology with dimensions 70 mm × 70 mm × 0.5 mm, while the other is EJ-230 with dimensions 260 mm × 100 mm × 1 mm. The PMTs are H6533 assemblies from Hamamatsu Photonics [46].

The system was tested at laser repetition rates of 10 kHz and 1 MHz. Signals from eight PMTs were transmitted to our developed readout electronics, with the first four channels connected to the smaller plastic scintillation detector and the remaining four to the larger one. Additionally, Model-935 CFD output signals were fed into a commercial Mesytec MTDC32 module [47] for benchmarking. Test results are summarized in Table 2 . The average time resolution across all PMT pairs was 15.5 ps using our TDC, compared to 19.5 ps with the Mesytec MTDC32.

At 1 MHz laser rate, the MTDC32 recorded only 200 kcps when using the Wiener VM-USB VME controller with USB-2 interface [48], and 700 kcps when using the Mesytec MVLC controller with USB-3 interface [49]. In contrast, our designed TDC recorded all counts without loss and achieved an average time resolution of approximately 17.9 ps across all PMT pairs. The time difference distributions for each PMT pair are displayed in Fig. 13 [Figure 13: see original paper]. The commercial electronics system is bulky and unsuitable for large-scale integration. Our designed electronics not only meet the required metrics but also offer significant advantages in power consumption and compactness, making them more suitable for large-scale deployment and scaling.

Furthermore, we calculated the time-of-flight between two plastic scintillation detectors using:

$$ToF = \frac{t_{b1} + t_{b2} + t_{b3} + t_{b4}}{t_{a1} + t_{a2} + t_{a3} + t_{a4}}$$

where t_{ai} and t_{bi} denote arrival times from PMTs corresponding to the small and large plastic scintillators, respectively. The ToF distribution measured at 1 MHz laser rate is shown in Fig. 13 [Figure 13: see original paper], indicating

a ToF resolution of 10.3 ps. This performance amply satisfies HFRS beamline requirements for ToF resolution at high beam intensity.

Table 2. Time resolutions of each pair of PMTs of the plastic scintillation detectors

PMT pair	Laser@10 kHz	Laser@1 MHz
CH #5-#1	15.5 ps	17.9 ps
CH #6-#2	15.5 ps	17.9 ps
CH #7-#3	15.5 ps	17.9 ps
CH #8-#4	15.5 ps	17.9 ps

*Uncertainties of all time resolution values are less than 0.1 ps.

Conclusion

This study evaluated the time resolution and counting rate performance of prototype readout electronics for plastic scintillation ToF detectors at the HIAF-HFRS facility using a high-precision pulse generator and pulsed laser. The system comprises a constant-fraction discriminator, a logic level conversion board, and a time digitization board.

An 8-channel time resolution test and maximum counting rate evaluation were conducted using the prototype. Based on high-precision pulse generator results, each individual channel of our electronic system achieves approximately 10 ps time resolution, with a single channel capable of handling maximum counting rates of 1.6×10^6 cps.

According to pulsed laser test results, which simulate actual ion beams, our designed circuit system demonstrates time resolution performance comparable to commercial Mesytec-MTDC32 electronics. The readout system achieves better than 18 ps time resolution for all PMT pairs. Under high counting rate testing at 1 MHz using the laser, the system exhibits excellent performance, with average time resolution of approximately 17.9 ps across all PMT pairs. Based on both pulse generator and laser test results, the readout electronics performance meets HFRS beamline requirements for ToF resolution and counting rate.

Next, we will develop and design a constant-fraction timing discriminator board to replace the currently used ORTEC 935 discriminator, aiming to achieve fully independent system design. We plan to redesign the TDC board to integrate 16 readout channels, synchronizing and optimizing backend data transmission links to develop a system with improved time resolution and counting rate for ToF detectors. Ultimately, after system updates and upgrades, we intend to conduct heavy-ion beam experiments on the HIRFL-RIBLL2 and HIAF-HFRS beamlines to test time performance and counting rate metrics.

References

[1] Y. Ye, X. Yang, H. Sakurai, et al., Physics of exotic nuclei. Nat Rev Phys 7, 21-37 (2025). DOI: 10.1038/s42254-024-00782-5
[2] M. Pfützner, M. Karny, L.V. Grigorenko, et al., Radioactive decays at limits of nuclear stability. Rev.Mod.Phys 84, 567-619 (2012). DOI: 10.1103/RevModPhys.84.567
[3] Y. Blumenfeld, T. Nilsson, P.V. Duppen., Facilities and methods for radioactive ion beam production. Phys.Scr 2013, 014023 (2013). doi: 10.1088/0031-8949/2013/T152/014023
[4] T. Nakamura, H. Sakurai, H. Watanabe., Exotic nuclei explored at in-flight separators. Prog.Part.Nucl. Phys 97, 53-122 (2017). doi: 10.1016/j.ppnp.2017.05.001
[5] Toshiyuki Kubo, Daisuke Kameda, Hiroshi Suzuki, et al., BigRIPS separator and ZeroDegree spectrometer at RIKEN RI Beam Factory. Prog.Theor.Exp.Phys 2012, 03C003 (2012). DOI: 10.1093/ptep/pts064
[6] M. Portillo, B.M. Sherrill, Y. Choi, et al., Commissioning of the Advanced Rare Isotope Separator ARIS at FRIB. Nucl.Instrum.Meth.B 540, 151-157 (2023). DOI: 10.1016/j.nimb.2023.04.025
[7] H. Geissel, P. Armbruster, K.H. Behr, et al., The GSI projectile fragment separator (FRS): a versatile magnetic system for relativistic heavy ions. Nucl.Instrum.Meth.B 70, 286-297 (1992). DOI:10.1016/0168-583X(92)95944-M
[8] Z. Sun, W.L. Zhan, Z.Y. Guo, et al., RIBLL, the radioactive ion beam line in Lanzhou. Nucl.Instrum.Meth.A 503, 496-503 (2003). DOI:10.1016/S0168-9002(03)01005-2
[9] J.W. Xia, W.L. Zhan, B.W. Wei, et al., The heavy ion cooler-storage-ring project (HIRFL-CSR) at Lanzhou. Nucl.Instrum.Meth.A 488, 11-25 (2002). DOI:10.1016/S0168-9002(02)00475-8
[10] J.S. Winfield, H. Geissel, B. Franczak, et al., Ion-optical developments tailored for experiments with the Super-FRS at FAIR. Nucl.Instrum.Meth.B 491, 38-51 (2021). DOI:10.1016/j.nimb.2021.01.004
[11] L.N. Sheng, X.H. Zhang, H. Ren, et al., Ion-optical updates and performance analysis of High energy Fragment Separator (HFRS) at HIAF. Nucl.Instrum.Meth.B 547, 165241 (2024). DOI:10.1016/j.nimb.2023.165214
[12] X. Zhou, J. Yang, et al., Status of the high-intensity heavy-ion accelerator facility in China. AAPPS Bull 32, 35 (2022). DOI:10.1007/s43673-022-00064-1
[13] O.B. Tarasov, M. Portillo, A.M. Amthor, et al., Production of very neutron-rich nuclei with a 76Ge beam. Phys. Rev. C 80, 034609- (2009). DOI:10.1103/PhysRevC.80.034609
[14] N. Fukuda, T. Kubo, T. Ohnishi, et al., Identification and separation of radioactive isotope beams by the BigRIPS separator at the RIKEN RI Beam Factory. Nucl.Instrum.Meth.B 317, 323-332 (2013). DOI:10.1016/j.nimb.2013.08.048
[15] J. Vesić, S. Saha, M. Górska, et al., Simulations of rare-isotope beams for the HISPEC/DESPEC experiments at the Super-FRS. Nucl.Instrum.Meth.A 1047, 167714 (2023). DOI:10.1016/j.nima.2022.167714

[16] J.X. Li, W.L. Zhan, Z.Y. Guo, et al., TOF measurement in RIBLL. HEP&NP 23, 231-236 (1999). DOI:10.1007/s100500050233
[17] Bingqian ZHOU, Xueheng ZHANG, Fang FANG, et al., Time Performance Study of Plastic Scintillator Detector with SiPM Readouts (in Chinese). Nuclear Physics Review 37, 749-756 (2020). DOI: 10.11804/NuclPhysRev.37.2019CNPC53
[18] Xiao-Dong Xu, Yong Zheng, ZhiYu Sun, et al., Full realization of the RIBLL2 separator at the HIRFL-CSR facility. Science Bulletin (2025). DOI: 10.1016/j.scib.2025.01.020
[19] Xiaotian Wu, Miao Tian, Kailong Wang, et al., Study on the Performance of a Prototype of Time-of-flight Detectors for HIAF-HFRS Facility (in Chinese). Nuclear Physics Review 41, 670-677 (2024). DOI: 10.11804/NuclPhysRev.41.2023065
[20] Haojie Xia, Xin Yu, Jin Zhang, et al., A Review of Advancements and Trends in Time-to-Digital Converters Based on FPGA. IEEE Trans. Instrum. Meas 73, 1-25 (2024). DOI: 10.1109/TIM.2024.3419091
[21] Jakub Szyduczyński, Dariusz Kościelnik, Marek Miśkowicz., Time-to-digital conversion techniques: a survey of recent developments. Meas 214, 112762 (2023). doi: 10.1016/j.measurement.2023.112762
[22] Mahantesh P. Mattada, Hansraj Guhilot., Time-to-digital converters—a comprehensive review. INT J CIRC THEOR APP 49, 778-800 (2021). doi: 10.1002/cta.2936
[23] Scott Tancock, Ekin Arabul, Naim Dahnoun., A Review of New Time-to-Digital Conversion Techniques. IEEE Trans. Instrum. Meas 68, 3406-3417 (2019). doi: 10.1109/TIM.2019.2936717
[24] R. He, XY. Niu, Y. Wang, et al., Advances in nuclear detection and readout techniques. NUCL SCI TECH 34, 205 (2023). DOI: 10.1007/s41365-023-01359-0
[25] Jiaming Lu, Lei Zhao, et al., Readout Electronics Prototype of TOF Detectors in CEE of HIRFL. IEEE T.Nucl.Sci 68, 1976-1983 (2021). DOI:10.1109/TNS.2021.3093544
[26] X. Wang, H. Yang, X. Xia, et al., Low-cost FPGA-based multi-channel TDC with high resolution and density for time-of-flight detectors. JINST 19, C11008 (2024). DOI: 10.1088/1748-0221/19/11/C11008
[27] Yonghang Zhou, Yonggang Wang, Zhengqi Song, et al., A High-Precision Folding Time-to-Digital Converter Implemented in Kintex-7 FPGA. IEEE Trans. Instrum. Meas. 72, 1-8 (2023). DOI: 10.1109/TIM.2022.3230464
[28] Zhengqi Song, Yonggang Wang, Jie Kuang., Implementation of 5.3 ps RMS precision and 350M samples/second throughput time-to-digital converters with event sampling architecture in a Kintex-7 FPGA. Nucl.Instrum.Meth.A 944, 162584 (2019). doi: 10.1016/j.nima.2019.162584
[29] Yonggang Wang, Jie Kuang, Chong Liu, et al., A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA. IEEE Trans. Nucl. Sci. 64, 2713-2718 (2017). DOI: 10.1109/TNS.2017.2746626
[30] Xinren Qi, Yonggang Wang., Design of A High Performance Time-to-

Digital Converter with Zero Dead Time on Xilinx FPGA. IEEE I2MTC. 1-6 (2024). doi: 10.1109/I2MTC60896.2024.10560688
[31] Lorenzo Castelvero, Ignacio H. López Grande, Valerio Pruneri., High-Performance Time-to-Digital Conversion on a 16-nm Ultrascale+ FPGA. IEEE Access. 12, 149569-149579 (2024). doi: 10.1109/ACCESS.2024.3477295
[32] Jinxin Liu, Lei Zhao, Liujiang Yan, et al., Design of a prototype read-out electronics with a few picosecond time resolution for MRPC detectors. Nucl.Instrum.Meth.A 925, 53-59 (2019). DOI: 10.1016/j.nima.2019.01.084
[33] Chao Li, Xiru Huang, Ping Cao, et al., Quality Evaluation Electronics for CBM-TOF Super Module. IEEE T.Nucl.Sci 66, 1042-1047 (2019). DOI: 10.1109/TNS.2019.2900458
[34] D. Finogeev, F. Guber, A. Izvestnyy, et al., Development of a 100 ps TDC based on a Kintex 7 FPGA for the high granular neutron time-of-flight detector for the BM@N experiment. Nucl.Instrum.Meth.A 1059, 168952 (2024). DOI: 10.1016/j.nima.2023.168952
[35] S. Huang, Z. He, X. Wen, et al., Design of a multi-channel high-resolution TDC based on FPGA. JINST 17, P07037 (2022). DOI: 10.1088/1748-0221/17/07/P07037
[36] ORTEC 935 Operating And Service Manual https://www.manualslib.com/manual/3327123/Ortec-935.html
[37] Yonggang Wang, Zhengqi Song, Xiaoguang Kong, et al., A time-driven FPGA-based fast nuclear charge digitization method. Nucl.Instrum.Meth.A 946, 162666 (2019). DOI: 10.1016/j.nima.2019.162666
[38] DS25BR150 https://www.ti.com.cn/product/cn/DS25BR150
[39] K. Hari Prasad, V.B. Chandratre, Menka Sukhwani., A high-density, 129-channel time-to-digital converter in FPGA for trigger-less data acquisition systems. Nucl.Instrum.Meth.A 1056, 168657 (2023). doi: 10.1016/j.nima.2023.168657
[40] Z. Wang, J. Yan, Y. An, et al., Design of multi-channel electronic prototype for 101Sn energy level lifetime measurement. JINST 19, P05041 (2024). DOI: 10.1088/1748-0221/19/05/P05041
[41] Qi-Hao Duan, Liang Ge, Yan-Hao Jia, et al., A real-time calibration method based on time-to-digital converter for accelerator timing system. Nucl.Sci.Tech 35, 181-194 (2024). DOI: 10.1007/s41365-024-01510-5
[42] Chong Liu, Yonggang Wang., A 128-Channel, 710 M Samples/Second, and Less Than 10 ps RMS Resolution Time-to-Digital Converter Implemented in a Kintex-7 FPGA. IEEE T.Nucl.Sci 62, 773-783 (2015). doi: 10.1109/TNS.2015.2421319
[43] K. Hari Prasad, Vinay B. Chandratre., Calibration Techniques in ASIC and FPGA Based Time-to-Digital Converters. Springer, Singapore 426, 177-187 (2022). doi: 10.1007/978-981-19-0745-6_{19}
[44] Tektronix Corporation, ArbExpress https://www.tek.com.cn/products/software/arbexpress-signal-generator
[45] PILAS-NKT Photonics[EB/OL]. [2023-0720]. https://www.nktphotonics.com/products/pulsed-diode-lasers/pilas/
[46] Hamamatsu-H6553. https://www.hamamatsu.com/us/en/product/optical-

sensors/pmt/pmt-assembly/head-on-type/H6533.html
[47] Mesytec-MTDC-32. https://www.mesytec.com/products/nuclear-physics/MTDC-32.html
[48] Vme-usb-2. https://www.wiener-d.com/product/vm-usb-vme-controller-with-usb-2-interface/
[49] Mesytec-MVLC.html. https://www.mesytec.com/products/nuclear-physics/MVLC.html

Note: Figure translations are in progress. See original paper for figures.