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Radiation-Hardened DC-DC Converter Design: Systematic Analysis of Single-Event Transient Effects and Voltage Clamping Mitigation Strategy

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Abstract

This paper investigates the single-event transient (SET) effects induced by high-energy particle radiation on the error amplifier (EA) within the loop of a DC-DC Boost converter using circuit-level simulation methods. Through the analysis of SET propagation within the loop and simulation verification, the relationship between SET impact on the DC-DC output voltage and load current is derived. A SET mitigation approach based on voltage clamping technology is proposed for SETs occurring at the EA output. By sampling and comparing the EA output voltage, SET detection is achieved. Upon detection of an SET, the EA output voltage is clamped, effectively isolating the SET propagation within the loop and ensuring the stability of the DC-DC output voltage, thereby endowing the DC-DC converter with a certain level of radiation hardness. The proposed method is verified using a 180nm commercial BCD process. Experimental results show that under a high-energy particle linear energy transfer (LET) of 100 MeV · cm2/mg, the output voltage variations in the DC-DC converter caused by negative and positive SETs are less than 0.6 mV and 1.7 mV, respectively. The SET mitigation capabilities are 96.1% and 87.1%, respectively. Moreover, for the hardened EA, SETs occurring at the output node have a 95.5% probability of not affecting the DC-DC converter' s output voltage.

Full Text

Preamble

Radiation-Hardened DC-DC Converter Design: Systematic Analysis of Single-Event Transient Effects and Voltage Clamping Mitigation Strategy

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This paper investigates the single-event transient (SET) effects induced by high-energy particle radiation on the error amplifier (EA) within the loop of a DC-DC Boost converter using circuit-level simulation methods. Through analysis of SET propagation within the loop and simulation verification, the relationship between SET impact on the DC-DC output voltage and load current is derived. A SET mitigation approach based on voltage clamping technology is proposed for SETs occurring at the EA output. By sampling and comparing the EA output voltage, SET detection is achieved. Upon detection of an SET, the EA output voltage is clamped, effectively isolating the SET propagation within the loop and ensuring the stability of the DC-DC output voltage, thereby endowing the DC-DC converter with a certain level of radiation hardness. The proposed method is verified using a 180nm commercial BCD process. Experimental results show that under a high-energy particle linear energy transfer (LET) of 100 $MeV \cdot cm^2/mg$, the output voltage variations in the DC-DC converter caused by negative and positive SETs are less than 0.6 mV and 1.7 mV, respectively. The SET mitigation capabilities are 96.1% and 87.1%, respectively. Moreover, for the hardened EA, SETs occurring at the output node have a 95.5% probability of not affecting the DC-DC converter' s output voltage.

Keywords: DC-DC converter, Single event transient (SET), Voltage clamping, Radiation hardened by design (RHBD)

Introduction

The space environment contains numerous radiation sources that, through different mechanisms, cause interruptions and damage to various spacecraft with integrated circuits as their core. Common radiation effects include the single-event transient effect (SET) and the total ionizing dose effect (TID) [1–3]. As an important component of power management chips, DC-DC converters are present in various industrial fields [4, 5]. In the space field, due to the harsh operating environment, the stability of DC-DC converters is not guaranteed, which limits their application [6–8]. When high-energy particles strike the reverse-biased PN junction in an integrated circuit, a large number of charged ions are ionized and immediately collected by sensitive nodes, causing changes in the transient current and voltage at the nodes—this is known as the SET [9–13]. The SET generated when high-energy particles enter the DC-DC converter poses a threat to system stability.

Given the importance of DC-DC converters in electronic devices, several studies have reported on SET phenomena and radiation hardening techniques related to DC-DC converters. Reference [14] identified through particle bombardment experiments that bandgap reference circuits are sensitive to SET, which could lead

to a reset of the DC-DC system. Reference [15] discovered that SET can affect the output voltage VOUT of DC-DC converters through high-energy particle injection experiments. Reference [16] conducted high-energy particle injection experiments on the voltage-controlled oscillator and comparator within PWM controllers, observing variations in the loop duty cycle that ultimately resulted in VOUT jumps, indicating that PWM controllers are among the SET-sensitive components in DC-DC converters.

Reference [17] proposed a method of adding resistors in series at the front end of the DC-DC converter to facilitate CMOS devices exiting Single Event Latch-up (SEL), but this approach only targets the digital circuit portions. In reference [18], a radiation-hardened process was used to harden a DC-DC converter based on switch capacitors, and redundant hardening design was also applied to the current reference circuit. However, this particular process is expensive and not universally applicable. Therefore, circuit-level hardening design has become increasingly attractive as an alternative approach. Reference [19] performed hardening on oscillators within the DC-DC converter, enabling them to withstand certain energy levels from particle strikes, but this was essentially a redundancy design for the internal RS latches and other digital circuits of the oscillator.

Redundancy hardening methods are commonly used in design hardening, but they primarily apply to digital circuits [20, 21]. The error amplifier (EA), as a core analog circuit within PWM controllers, is particularly susceptible to SET effects [22]. For the hardening of analog integrated circuits, Reference [23] proposed an RC filtering approach specifically for bandgap reference circuits, which involves connecting high-value resistors and capacitors at the output terminal of the reference to filter out voltage ripple. While this method can reduce the amplitude of reference voltage transients, it also prolongs the recovery time of the reference voltage and significantly increases chip area. Reference [24] performed SET analysis on the charge pump (CP) in phase-locked loops (PLLs). By directly adding a digital control circuit between the CP and the low-pass filter (LPF), the transmission of SET currents was interrupted, and a charge release circuit was utilized to dissipate the charges generated by SET effects. Although this digital circuit resembles a latch unit with strong resistance against SET, it still suffers from false triggering and occurrences of SET during port switching. Reference [25] introduced a symmetrical multi-path-splitting (SMPS) method, which splits SET-sensitive nodes in low-dropout regulators (LDOs) and adds resistors between adjacent nodes for isolation. This approach significantly reduces the impact of SET; however, the circuit structure must be replicated multiple times for effective SET mitigation, complicating the circuit layout. Reference [26] incorporated two NMOS transistors into a voltage-controlled oscillator (VCO), ingeniously cross-connecting them with the existing two PMOS transistors to form positive feedback and accelerate the SET recovery process. However, the universality of this hardening technique is relatively poor.

This paper is based on a DC-DC Boost converter integrated on a single chip using a commercially available 180nm BCD process. The study focuses on the

SET in the EA of the PWM control unit and proposes a SET mitigation method based on voltage clamping. The remaining sections of this paper are organized as follows: Section II introduces the impact of SET in the EA on the DC-DC loop. Section III presents the proposed DC-DC hardening method based on voltage clamping technology. Section IV provides experimental results and analysis. Finally, Section V concludes the paper.

II. The Effect of SET on the DC-DC Loop

A. SET Simulation

The simulation region can extend downward in a funnel shape along the particle trajectory, and this phenomenon is known as the "funnel effect." The funnel effect significantly increases the carrier collection region. With the absorption of electrons and holes by the depletion region formed between the drain and the substrate, a transient current ISET will be formed. Specifically, the NMOS extracts ISET from the drain, discharging the parasitic capacitance at the drain and generating a negative SET pulse. Conversely, the PMOS injects ISET into the drain, charging the parasitic capacitance and producing a positive SET pulse.

The relationship between the charge collected Q at the drain after high-energy particle bombardment of sensitive nodes and the Linear Energy Transfer (LET) of the particles can be expressed as follows:

$$Q = e \cdot \rho \cdot d \cdot LET/E_{eh}$$

where e represents the elementary charge of an electron,   is the volume density of silicon, d denotes the penetration depth of high-energy particles, and Eeh is the minimum energy required to ionize an electron-hole pair in the target material. To simulate the transient current ISET induced by particle bombardment, a double-exponential instantaneous pulse model is used for modeling ISET [27, 28]. The expression is given as follows:

$$I_{SET} = \frac{Q}{\tau_f - \tau_r} \left(\exp(-t/\tau_f) - \exp(-t/\tau_r) \right)$$

In analog integrated circuits, different MOS devices have distinct electrical parameters, which lead to different responses at the circuit nodes. [Figure 1: see original paper] illustrates the mechanism diagram of SET generation when high-energy particles enter bulk silicon MOS devices, where τr is the rise time constant of the current pulse and τf is the fall time constant. Here, τr is set to 50ps and τf is set to 450ps. [Figure 2: see original paper] illustrates the ISET generated by different LET values.

When high-energy particles enter the sensitive region of a MOS device, they ionize a large number of electron-hole pairs from extranuclear electrons along

the incident trajectory. The depletion region formed by the reverse-biased PN junction, due to its strong electric field, becomes a sensitive region for carrier collection. Since the ionized carriers with high concentration along the particle trajectory can be approximated as a conductor, the electric field in the depletion region can extend deeper into the substrate. The LET values selected in this paper are within the expected test range for CMOS technology [29]. In the subsequent SET impact analysis and hardening effect tests of the DC-DC converter presented in this paper, this current source model is employed.

B. DC-DC Converter Structure and SET Sensitive Node Analysis

The DC-DC converter must be combined with a controller to form a negative feedback loop in order to provide a controllable and stable VOUT. [Figure 3: see original paper] illustrates the overall architecture of a peak current mode-controlled DC-DC boost converter. The reference voltage VCT output from the DAC and the feedback voltage VFB from the DC-DC output jointly act on the EA to regulate the loop and stabilize VOUT.

In steady state, the relationship between the input voltage VIN and the VOUT of a Boost converter can be expressed as:

$$V_{OUT} = \frac{V_{IN}}{1 - D}$$

where the duty cycle D is defined as the ratio of the time the control signal VNG for transistor M1 is high to the clock period T. High-energy particle strikes on the DC-DC loop may affect D, leading to variations in the inductor current IL. If this influence persists for a longer duration and affects multiple control cycles of the loop, it can impact VOUT.

To enhance the low-frequency gain of the loop and suppress high-frequency noise, a PI compensation method is employed for the control loop. Compensation resistor R1 and compensation capacitors C1 and C2 are connected at the output of the EA. The values of the compensation resistors and capacitors must be determined in conjunction with the parameters of the loop. In this application, R1 is set to 2.3MΩ, C1 is 10pF, and C2 is 200fF.

Since DC-DC converters operate based on switching cycle control, the duration of SET occurring at most nodes within the loop is relatively short, generally ranging from a few nanoseconds to several tens of nanoseconds. The switching frequency of common non-isolated chip-level DC-DC converters typically lies in the range of several kilohertz (kHz) to several megahertz (MHz). Taking the switching frequency of 1.5 MHz used in this paper as an example, one cycle is approximately 667 ns. Therefore, the unstable time caused by SET at most nodes accounts for only a small fraction of the entire switching cycle. Moreover, due to the presence of output capacitance at the converter' s output terminal, the influence on just one switching cycle will not lead to a significant change in

the output voltage. However, the SET occurring at the output terminal of the EA, influenced by the compensation network, will affect the duty cycle and the inductor current for a relatively long time. Therefore, this paper focuses on the study of SET at the output node of the EA and proposes a circuit design for mitigating SET at this node.

The circuit structure of the EA is shown in [Figure 4: see original paper]. VB1, VB2, and VB3 are bias voltages. High-energy particles striking the drain of M18 will trigger a negative SET pulse, causing VC to decrease, while impacts on the drain of M17 will result in a positive SET pulse, leading to an increase in VC. The signal VC is passed to VCM through a voltage conversion circuit, as shown in [Figure 5: see original paper]. Transistors M1 and M2 form a current mirror, which fixes the current in the branch containing M2. Therefore, the voltage VGS between the gate and source of M3 is a constant value. The relationship between VCM and VC is as follows:

$$V_{CM} = V_C - V_{GS}$$

The reason for level-shifting VC is twofold: it allows the common-mode voltage range of VC to vary within a higher range, enabling the compensation capacitor to operate in a strong response region and ensuring loop stability. Additionally, during the soft start phase, limiting VC restricts the magnitude of the inductor current. The PWM comparator compares VCM containing erroneous information and VSUM, resulting in changes in D and IL, thereby causing an offset in VOUT. [Figure 6: see original paper] illustrates the transmission diagram of SET effects on VC within the loop. The waveforms of VC and VCM have slight differences. In the process of signal propagation, the limitation of the loop bandwidth results in a certain mitigation of the transition speed and amplitude of VCM by the voltage conversion circuit. The shaded area A represents the amount of charge absorbed by the load capacitance, which will cause a decrease in the output voltage VOUT:

$$\Delta V_{OUT} = \frac{A}{C_{OUT}}$$

Reducing the shaded area A will help mitigate the effects caused by SET. [Figure 6: see original paper] illustrates the impact of a negative SET pulse; the mechanism of influence from a positive SET pulse is similar, except it will result in an increase in VOUT.

C. The Impact of SET on the Converter' s Output Voltage Under Different Load Conditions

From the previous analysis, it can be concluded that an SET occurring at the output of the EA will change the VCM of the loop, leading to variations in D and IL. The charge loss A at the system output causes VOUT to decrease, while

absorbing excess charge A results in an increase in VOUT. The magnitude of A is actually related to the load current IOUT. [Figure 7: see original paper] shows the waveforms at key nodes in the loop corresponding to negative SET at the EA output for different IOUT values. The simulation conditions are set to VIN = 3.7V, VOUT = 6.7V, and the particle LET value is set to 100 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$.

As IOUT decreases, the impact on VOUT becomes smaller. Although particle incidence may cause a significant jump in VC, VCM has a lower voltage limit that prevents further reduction of VCM. As IOUT decreases, VCM also decreases, leading to a corresponding reduction in the DC value of IL. Additionally, the drop in IL caused by SET will trigger zero-crossing detection, ensuring that the minimum value of IL is 0. Consequently, the variation in IL induced by negative SET is confined to a small range of change. Therefore, as IOUT decreases, the value of A becomes smaller, resulting in a reduced impact on VOUT.

In contrast to negative SET, positive SET causes an upward jump in VCM without any upper voltage limitation. Thus, the magnitude of the jump in VOUT due to positive SET is not significantly related to the load. The effects of positive SET on the key nodes of the loop are illustrated in [Figure 8: see original paper]. Under heavy load conditions, the impact of positive SET on the loop is minimized due to the setting of the minimum shutdown time in the system.

III. DC-DC Hardening Design Based on Voltage Clamping Technology

A. Hardening Circuit Design

The SET induced by particle incidence at the output of the EA causes a change in VC, which, when propagated through the loop, results in an offset in VOUT. To mitigate the impact of SET on the DC-DC converter, this paper proposes a voltage clamping technique-based SET mitigation method. This method involves detecting the occurrence of SET in the EA and clamping VC to the correct value. [Figure 9: see original paper] illustrates the proposed voltage clamping technique for SET mitigation.

The architecture consists of a sample-and-hold circuit, SET detection circuit, pulse widening circuit, and voltage clamping circuit. The sampling circuit is composed of an operational amplifier OP1 with unity gain negative feedback, a switch S1, and a capacitor C3. The purpose of the sampling circuit is to sample the output voltage VC of the EA. When the sampling switch S1 is closed, the voltage value VC is stored on C3. To mitigate the voltage drop caused by charge leakage from C3, every 200 DC-DC clock cycles, CLK1 is set low and S1 is closed once to refresh the value of C3, ensuring that Vsamp = VC.

The SET detection circuit is composed of two positive threshold comparators,

Com1 and Com2, and a NAND gate G1. When Vsamp = VC, meaning that the voltages at the non-inverting and inverting terminals of both comparators are equal, the presence of positive thresholds in the comparators results in high output levels Va and Vb from Com1 and Com2, respectively. Consequently, the output V1 from the NAND gate G1 will be low. When a particle incidence causes VC to experience a positive SET, the voltage VC jumps upward, exceeding the positive threshold of Com2, which causes Vb to flip to a low level. Conversely, if a negative SET occurs due to particle incidence causing VC to jump downward, VC falls below the positive threshold of Com1, resulting in Va flipping to a low level. The transition of either Va or Vb to a low level will produce a high level at V1. Thus, the SET detection circuit can convert both positive and negative SET triggered by particle incidence at the EA into a single high-level pulse.

The duration of V1 being in a high state is the time when VC exceeds (or falls below) the set threshold. This duration is relatively short. If it is directly used as the control signal for switch S2 in the voltage clamping circuit, it may not allow sufficient time for VC to fully recover. To address this issue, a pulse widening circuit is proposed here, as shown in [Figure 10: see original paper], which extends the effective level signal of V1 to obtain V2.

The pulse widening circuit consists of an SR latch, inverters G3 and G4, NMOS transistors M2 and M3, capacitor C4, and comparator Com3. V1 represents the output signal from the SET detection circuit, while V2 is the output signal from the pulse widening circuit. When V1 is high, the RS latch is reset, resulting in V2 being high and VQ being low. After passing through inverter G3, V4 becomes high, activating transistor M2 and turning off transistor M3, thus allowing current source I0 to charge capacitor C4. This continues until the voltage V5 across the capacitor exceeds VREF, at which point comparator Com3 outputs a low level for V6. After passing through inverter G4, the output V7 becomes high, leading to a high state at the S terminal of the RS latch, setting the latch and causing V2 to become low while VQ goes high. Therefore, the duration tw that V2 maintains a high state corresponds to the time required for I0 to charge capacitor C4 until the voltage V5 reaches VREF. The expression for tw can be given as:

$$t_w = \frac{V_{REF} \cdot C4}{I0}$$

The pulse high-level duration can be controlled by adjusting the charging current I0, the capacitance C4, and VREF. In summary, the pulse widening circuit expands the narrow pulse signal V1 output from the SET detection circuit into a wider pulse signal V2. The signal V2 is then inverted by inverter G2 to generate the control signal V3 for switch S2.

The voltage clamping circuit is composed of OP2, M1, R2, and S2. Due to the negative feedback characteristics of the voltage clamping circuit itself, VS = Vsamp, and this circuit structure can provide a large driving current. When a

particle impacts the output of the EA, it causes a jump in VC. Once detected by the detection circuit, V3 transitions from a high level to a low level, which opens S2 and clamps the jumping VC voltage to Vsamp, such that VC = Vsamp. This prevents erroneous signals from propagating to subsequent stages, thereby achieving hardening design for the DC-DC converter.

In addition, the proposed hardening circuit in this paper can achieve immunity to SET itself. If a particle incidence causes an erroneous flip in the output of G2, transitioning from a high level to a low level, this would lead to the closure of S2. However, since VC = Vsamp, the voltage clamping circuit does not affect VC, and therefore, the hardening circuit does not impact the DC-DC loop in such a scenario.

B. Distinguishing from Load Transients

It is important to note that if the output load of the DC-DC converter experiences significant changes within a short time, known as load transients, it will also cause jumps in VC to adjust D and IL for stabilizing VOUT. If SET cannot be distinguished from load transients, the SET mitigation circuit proposed in this paper may exhibit false triggering, preventing the loop from performing its normal regulation.

If the range of changes in VC can be determined and is significantly smaller than the range of jumps in VC caused by SET, then the two can be distinguished. The range of VC, denoted as VCRange, is actually determined by the maximum inductance current ILMax and the equivalent series resistance Ri = VCRange/ILMax. Reducing Ri will increase VCRange; however, a decrease in Ri will affect the sampling accuracy of the inductor current and diminish the effectiveness of the current loop, making it behave more like a voltage mode. Therefore, within the permissible conditions for VCRange, a larger Ri is preferable. Typically, when the load range is relatively small, VCRange can be set to around 1.5V. However, to account for fluctuations in Ri due to different processes, the variation in VC caused by load changes is usually set to be k times VCRange, with k generally taken as 0.5 to 0.7.

In this study, the maximum output current IOUT of the DC-DC converter is 150mA. The output current drops from 150mA to 10mA within 5µs. A simulation of VCRange was conducted, and the results are shown in [Figure 11: see original paper]. During load transients, the maximum variation in VC is 0.7V. By setting different particle LET values, simulations were conducted to analyze negative and positive SET occurring in VC. The results are depicted in [Figure 12: see original paper]. As the particle energy increases, the magnitude of the voltage jump in VC also increases. When LET = 20 $\mathrm{MeV \cdot cm^2/mg}$, both positive and negative SET cause a voltage jump in VC greater than 0.8V. Setting the forward threshold of comparators Com1 and Com2 in [Figure 9: see original paper] to 0.75V, corresponding to a particle LET of 15 $\mathrm{MeV \cdot cm^2/mg}$, results in the voltage jump in VOUT as shown in [Figure 13: see original paper]. With the

voltage jump in VOUT being within 2.1mV, setting the comparator threshold to 0.75V allows for the distinction between SETs and load transients.

IV. Experimental Results and Discussion

In this study, based on a commercial 180nm BCD process, the layout design and post-simulation verification of a DC-DC converter utilizing voltage clamping hardening technique were conducted. [Figure 14: see original paper] shows the overall layout of the DC-DC converter with dimensions of 1882µm × 1375µm. The area of the hardened circuit is 160µm × 97µm.

Under the conditions of VIN = 3.7V, VOUT = 6.7V, and IOUT = 100mA, the mitigation results of SET were verified by setting the particle energy LET to 100 $\text{MeV} \cdot \text{cm}^2/\text{mg}$. The waveforms of the key nodes in the loop are shown in [Figure 15: see original paper]. After hardening the DC-DC converter, neither negative SET nor positive SET affect the output voltage, nor do they alter D or IL. However, it is important to note that this is also related to the timing of particle incidence; if a particle strikes the circuit precisely when VSUM and VCM are in contact, there may still be a slight impact on the loop, affecting only one cycle.

As shown in [Figure 15: see original paper], the hardened circuit can almost completely eliminate the influence of negative SET on VCM. However, positive SET still cause a jump in VCM, with a pulse width of approximately 30 ns, which accounts for 4.5% of the entire clock cycle. This indicates that after hardening, the DC-DC converter has a 95.5% probability of being immune to SET impacts. Even when affected, the impact is minimal.

Under different load conditions, particles were set to strike the DC-DC converter when VSUM equals VCM. The comparison of VOUT before and after hardening is presented, with the mitigation results for negative SET shown in [Figure 16: see original paper]. Before hardening, the impact of negative SET on VOUT was greatest at IOUT = 150mA, with a voltage jump of 15.1mV. After hardening, this value decreased to 486µV, indicating that negative SET have little effect on the VOUT of the DC-DC converter.

The mitigation results for positive SET are shown in [Figure 17: see original paper]. The impact of positive SET on VOUT does not exhibit a direct correlation. The maximum voltage jump in VOUT was 12.8mV before hardening, which reduced to 1.4mV after hardening.

Comprehensive simulation validation of the SET mitigation effects for the hardened circuit was performed. The particles were set with a LET of 100 $\text{MeV} \cdot \text{cm}^2/\text{mg}$, and the mitigation effects of SET were thoroughly validated through PVT (Process, Voltage, Temperature) simulations. The validation results are shown in [Figure 18: see original paper]. Under different PVT conditions, the hardened circuit demonstrates effective mitigation performance. The maximum voltage jump in VOUT caused by negative SET was 15.4mV before hardening

and reduced to no more than 0.6mV after hardening, achieving a mitigation capability of 96.1% for negative SET. For positive SET, the maximum voltage jump in VOUT was 13.2mV before hardening, which decreased to no more than 1.7mV after hardening, resulting in a mitigation capability of 87.1% for positive SET.

During a load transient where IOUT drops from 150mA to 10mA, a simulation was conducted on the clamping switch control signal V3 as shown in [Figure 19: see original paper]. During a load transient, the voltage jump in VC did not trigger the threshold comparator to flip, and V3 remained at a high level, keeping switch S2 closed. The hardened circuit had no effect on the original circuit, effectively distinguishing between SETs and load transients.

To assess the stability of the loop after hardening, an AC modeling of the loop was performed. The power stage was modeled using an average switching model [30], while the control stage employed the small-signal modeling approach based on peak current mode proposed by Ridley. Based on the AC model, simulations were conducted in SPICE to validate the hardened circuit, as shown in [Figure 20: see original paper]. After hardening, the phase margin of the loop is minimized at 10mA, reaching 65°, which meets the stability requirements. The crossover frequency of the loop is above 70kHz in all cases.

A comparison of the parameters and hardening results from this study with references [23-26] is presented in .

V. Conclusion

In this DC-DC converter study, the impact of SET in the sensitive component —the PWM controller' s EA—was investigated. The analysis and simulation verification of SET propagation within the loop were carried out, leading to an understanding of the relationship between SET and load size on VOUT. To address the effects of SET, a radiation-hardened circuit based on voltage clamping technology was proposed for the EA. By setting appropriate thresholds, the differentiation between SETs and load transients was achieved. Additionally, pulse-width modulation techniques were employed to expedite the recovery of the sensitive node voltage, effectively maintaining the stability of the DC-DC converter' s VOUT. This research not only provides a foundation for future studies on SET in DC-DC converters but also offers a hardened circuit approach to mitigate their effects.

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