Development of an Innovative Real-Time Dosimetry Monitoring System for Heavy Ion Radiotherapy

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Abstract

Cancer is the second leading cause of mortality globally. As a critical technological approach in oncology treatment, radiation therapy is evolving from conventional radiotherapy to ultra-high dose rate radiotherapy (FLASH-RT). With the significant escalation in radiotherapy dose rates, real-time dosimetry monitoring faces the dual challenges of enhancing both response time and measurement precision. This work successfully developed a real-time dosimetry monitoring system for radiotherapy, designed to accommodate a broad range of dose rates. The system consists of a dual-gated integrator architecture front-end circuit and a high-speed data acquisition circuit, providing accurate detection of bipolar current pulse signals spanning from -190 μA to +200 μA, the minimum current measurement range is from -1 pA to 1 pA. Two significant technological advancements were accomplished: (1) The elimination of signal processing dead time resulted in a reduction of the single-event readout time to 5 μs; (2)The nonlinear error from -190 μA up to the maximum current is within 0.67%, with a linear correlation coefficient (R2)of 0.99992. The experiments were conducted using an ionization chamber detector at the Heavy Ion Research Facility in Lanzhou (HIRFL-TR4), this system, combined with a dose detector, achieves real-time dose measurement within the dose rate range of 65 Gy/min to 120 Gy/min. It demonstrates excellent real-time monitoring performance in the high-dose rate range of radiation therapy and shows potential for further application in dose monitoring for electron and proton beam radiotherapy.

Full Text

Preamble

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Cancer is the second leading cause of mortality globally. As a critical technological approach in oncology treatment, radiation therapy is evolving from conventional radiotherapy to ultra-high dose rate radiotherapy (FLASH-RT). With the significant escalation in radiotherapy dose rates, real-time dosimetry monitoring faces the dual challenges of enhancing both response time and measurement precision. This work successfully developed a real-time dosimetry monitoring system for radiotherapy, designed to accommodate a broad range of dose rates. The system consists of a dual-gated integrator architecture front-end circuit and a high-speed data acquisition circuit, providing accurate detection of bipolar current pulse signals spanning from -190 µA to +200 µA, with a minimum current measurement range from -1 pA to 1 pA. Two significant technological advancements were accomplished: first, the elimination of signal processing dead time resulted in a reduction of the single-event readout time to 5 µs; second, the nonlinear error from -190 µA up to the maximum current is within 0.67%, with a linear correlation coefficient (R^2) of 0.99992. The experiments were conducted using an ionization chamber detector at the Heavy Ion Research Facility in Lanzhou (HIRFL-TR4). This system, combined with a dose detector, achieves real-time dose measurement within the dose rate range of 65 Gy/min to 120 Gy/min. It demonstrates excellent real-time monitoring performance in the high-dose rate range of radiation therapy and shows potential for further application in dose monitoring for electron and proton beam radiotherapy.

Keywords: Real-time dosimetry monitoring, Heavy Ion Radiotherapy, Data acquisition circuit, Analog front-end circuit

Introduction

Malignant tumors represent a significant threat to human health, with radiation therapy being one of the most crucial treatment methods for cancer. Unlike traditional photon radiation, heavy ion beams exhibit a Bragg peak—a concentrated dose deposition whose depth can be finely adjusted by altering the beam energy [**?**]. This feature enhances protection for healthy tissues [**?**], making heavy ion therapy currently regarded as the most optimal form of radiation therapy in clinical practice [**?**, **?**]. Research indicates that while high-dose per fraction radiotherapy can suppress tumor-reactive immunity [**?**], ultra-high dose rate

radiotherapy (FLASH-RT) notably reduces radiation toxicity to normal cells surrounding tumor cells \cite{6–8}. Ion beam radiotherapy has evolved from conventional dose rate therapy to high dose rate and, more recently, to ultra-high dose rate therapies such as FLASH-RT. The effectiveness and quality of ion beam therapy are strongly correlated with the dose delivered to the patient, making beam monitoring essential for ensuring the precision and efficacy of ion therapy [**?**]. As dose rates increase, the demands for real-time dose monitoring in terms of difficulty, importance, and accuracy are progressively heightened.

Typically, ionization chambers are used as dose detectors at the end of heavy ion radiotherapy to measure the dose \cite{10–16}. The current signal produced by the ionization chamber is directly proportional to the dose delivered during beam radiation therapy. Dose ionization chamber detectors are characterized by their negligible dependence on particle energy and linear energy transfer, while exhibiting high reproducibility and accuracy. As a result, ionization chambers are regarded as the gold standard for monitoring radiation therapy doses [**?**].

Columns 2 and 3 of Table 1 present the range of current output from the ionization chamber for various radiation therapy devices under corresponding dose rate conditions. The output signal from the dose ionization chamber detector varies due to differences in beam intensity and the chamber' s actual gain. Therefore, dose monitoring readout electronics must be capable of measuring input signals in the range of pA to µA [**?**]. Columns 4 and 5 of Table 1 present the readout electronics systems for dose ionization chambers and their linearity relationships for different radiation therapy devices. As shown in the table, internationally, the measurement of current signals output by dose detection ionization chambers generally uses Very Large Scale Integration (VLSI) [**?**], Application-Specific Integrated Circuits (ASICs) [**?**], or discrete components \cite{26–28}. VLSI and ASIC devices are characterized by high integration, low power consumption, and exceptional stability; however, their development is complex, with long timelines, limited versatility, and slow technological advancements. In contrast, measurement circuits based on discrete components provide greater flexibility, lower cost, and faster technological updates, but they tend to occupy more circuit board space, have lower integration, and are more susceptible to noise interference.

Two commonly used readout schemes utilizing discrete components are as follows. The first scheme uses an integrator circuit combined with an Analog to Digital Converter (ADC) for sampling and output [**?**]. This approach directly integrates the current to obtain the charge, making it relatively simple and insensitive to AC noise. The measurement range can be adjusted by selecting an appropriate capacitance based on the beam intensity. The second scheme converts the current into a voltage, which is subsequently converted into a frequency output [**?**], with the charge measured via a count. This scheme is conducive to digital processing and provides high accuracy. Nevertheless, its linear range is limited, and when the current approaches the measurement threshold, the linearity may deviate, leading to measurement errors. As such, this approach is

not suitable for general-purpose designs.

To facilitate dose measurements compatible with both high dose rate and conventional dose rate radiotherapy—specifically covering current outputs ranging from hundreds of pA to hundreds of µA as typically provided by ionization chambers—we have developed an innovative real-time dose monitoring readout system. This system utilizes a dual-gated integrator architecture for the analog front-end (AFE) circuit to directly integrate the current. Coupled with a data acquisition (DAQ) circuit for sampling and readout, the system is capable of covering a wide bipolar dynamic current range of -190 µA to 210 µA, thus meeting the readout requirements of the majority of ionization chamber detectors used in particle therapy dose measurements. In conventional designs, current signals are acquired after passing through the AFE circuit. During the acquisition period, the AFE circuit must maintain the current voltage, rendering it incapable of responding to real-time input currents, thereby causing dead time. This dead time limits the detector' s ability to record all events, potentially compromising the completeness of data acquisition and subsequently affecting the precision and efficacy of the treatment process. Furthermore, the response capability to high-frequency events, which is directly related to the processing time of individual events, can impact the accuracy of real-time monitoring. To address these limitations, the proposed real-time dose monitoring readout system utilizes a dual-gated integrator architecture in the analog front-end processing circuit. By enabling two integrators to operate alternately, the system effectively eliminates dead time and reduces the individual event processing time to 5 µs.

System Structure

The schematic diagram of the innovative real-time dosimetry monitoring system is shown in Fig. 1 [Figure 1: see original paper]. The system consists of two primary components: an innovative analog front-end (AFE) circuit based on a dual-gated integrator architecture, and a data acquisition (DAQ) circuit. The AFE utilizes a dual-gated integrator to segment and process the weak current signals from the detector, converting them into voltage. This voltage signal is subsequently sampled and encoded by a pipeline-style analog-to-digital converter (ADC). The Field Programmable Gate Array (FPGA) on the DAQ circuit board is responsible for synchronizing and compressing the encoded data. Additionally, the FPGA logic control circuit manages the conversion process of the AFE circuit, ADC sampling, and other associated operations. Finally, the FPGA communicates with the host computer via USB, enabling command transmission and uploading of dose data. The host computer processes the transmitted data and displays it in real time.

AFE Circuit

As shown in Fig. 2 [Figure 2: see original paper], the AFE circuit consists of dual-gated integrators, a multiplexer, an optocoupler isolator, an attenuation

circuit, and a Complex Programmable Logic Device (CPLD). The current signal output from the ionization chamber alternately enters the two gated integrators, is converted into a voltage signal, and then selected and output controlled by the CPLD via the multiplexer. Upon receiving the external trigger signal TrigIn, the circuit is activated. Integrator A begins integrating during the high-level period, generating a voltage signal. Simultaneously, the CPLD controls the multiplexer to output the voltage from Integrator B, which is held for a certain duration to allow digitization by the DAQ circuit. Afterward, the voltage is discharged to complete initialization. When TrigIn transitions, Integrator B starts integrating and generating a voltage, while the CPLD switches the multiplexer to output the voltage from Integrator A. This voltage is similarly held for digitization and then discharged. The image of the AFE circuit is shown in Fig. 3 [Figure 3: see original paper]. As the AFE circuit is located near the beam area, a shielding enclosure is employed to enhance its radiation tolerance, effectively reducing external radiation interference and improving system stability.

Dual-Gated Integrator Architecture Circuit The dual-gated integrator architecture circuit is constructed using two integrators in conjunction with four high-speed switching gates, as shown in Fig. 4 [Figure 4: see original paper]. The dual-gated integrator architecture circuit begins operation after power-on reset. The alternating hardware operation states during its working period are illustrated in Fig. 5 [Figure 5: see original paper].

1. **State 1**: The input current is integrated by Integrator A, with its integration switch closed and discharge switch open. Integrator B remains with both switches open. The DAQ circuit samples the voltage from Integrator B.
2. **State 2**: After the voltage sampling from Integrator B is completed, the AFE circuit closes the discharge switch of Integrator B to discharge the voltage. Meanwhile, Integrator A continues integrating.
3. **State 3**: Upon completion of the discharge, Integrator B begins integration as its integration switch closes. Simultaneously, both switches of Integrator A are opened to halt integration. The DAQ circuit then samples the voltage from Integrator A.
4. **State 4**: After the DAQ circuit finishes sampling the voltage from Integrator A, the discharge switch of Integrator A is closed, and the AFE circuit discharges the voltage from Integrator A. Once the voltage from Integrator A is fully discharged, the cycle returns to State 1, where the integration and discharge switches of Integrator B are both opened, halting integration in Integrator B, and Integrator A starts the integration process again while the DAQ circuit samples the voltage from Integrator B. This process repeats continuously.

The integration switch is closed only when the discharge switch is open. During the short period that the integration switch is open (approximately 100 ns), any signal current produced by the ionization chamber will charge the ionization

chamber' s effective input capacitor. This charge is then transferred to the integrating capacitor when the integration switch is closed. As a result, no charge produced by the ionization chamber is lost and the input signal is continuously integrated. Even fast input pulses are accurately integrated.

To eliminate errors caused by baseline drift, the integration output voltage V_O is calculated by subtracting the baseline voltage $V_{baseline}$ from the measured voltage V, as defined in Eq. (1):

$$V_O = V - V_{baseline}$$

The functional relationship between the output charge Q of a single integration and the output voltage is given by Eq. (2):

$$Q = C_{INT} V_O = I_{IN} T_{IN}$$

Where I_{IN} is the input current and C_{INT} is the integration capacitor. To ensure the accuracy of the calculated results, the value of C_{INT} should be accurately calibrated in the laboratory to minimize deviations from theoretical values and ensure measurement accuracy.

Assuming the input current is integrated over a certain period, the total accumulated charge is given by Eq. (3):

$$\sum Q_i$$

Where Q_i is the output charge of the ith integration cycle.

Suppose the input current is 100 µA, each integration period is 5 µs, and the integration capacitance is calibrated to 100 pF, the output charge per cycle is calculated as follows in Eq. (4):

$$Q = I_{IN} T_{IN} = 500 \text{ pC}$$

If the input current is continuously integrated over 1 ms, corresponding to 200 events, the total accumulated charge is calculated by Eq. (5):

$$\sum Q_i = Q_1 + Q_2 + Q_3 + \cdots + Q_{200} = 100 \text{ nC}$$

The output current pulse signal range of the dose ionization chamber detector exhibits a large span. The gated integrator can adjust the gain to accommodate different input ranges. The circuit' s conversion gain is determined by both the integration time and the integration capacitance. Specifically, the output voltage is proportional to the integration time and inversely proportional to the integration capacitance. Higher gain can be obtained by increasing the integration time or reducing the integration capacitance. When the input signal is large, the integration time of the gated integrator is shortened, whereas when

the input signal is small, the integration time is increased. The gated integrator is highly flexible, capable not only of converting and amplifying current to voltage but also of effectively mitigating noise and interference signals that fluctuate around the baseline by integrating them out, resulting in a significant reduction of noise and interference. Furthermore, the gated integrator used in this circuit features on-chip integrated capacitors, which helps to minimize the impact of leakage voltage caused by dielectric losses in the integration capacitor.

The traditional single integrator architecture typically has a dead time between integration and discharge (a blank period during charge signal processing) which can result in increased measurement errors and reduced timeliness. In contrast, the dual-gated integrator architecture alternates between two integrators to complete integration and discharge, ensuring real-time and continuous processing of current signals and providing dead-time-free readout. This is especially critical for rapid response and high-accuracy dose measurements.

Attenuation Circuit As shown in Fig. 2, the attenuation circuit follows the multiplexer circuit at the backend. The voltage amplitude range of the output from the front-end multiplexer circuit is between -10 V and 10 V. To reduce the power consumption of the circuit and match the signal processing range of the data acquisition circuit in the subsequent stage, a voltage attenuation circuit is designed to attenuate the signal within the -10 V to 10 V range to between -1 V and 1 V. The attenuation is implemented using the T-attenuation circuit, as shown in Fig. 6 [Figure 6: see original paper]. The calculation method for the resistance of the circuit is given by Eq. (6), where R_c is the circuit impedance matching resistance of 50 Ω, and N is the attenuation factor.

$$R_1 = R_c \frac{N-1}{N+1}$$
$$R_2 = \frac{R_c}{2} \frac{N^2-1}{N}$$

From the above equation, the resistances in this circuit are calculated as $R_1 =$ 10 kΩ, $R_2 = 560$ Ω. The voltage signal amplitude after passing through the attenuation circuit is $±$1 V, which is then fed directly to the data acquisition circuit through a subsequent stage follower circuit.

DAQ Circuit Board

As shown in Fig. 7 [Figure 7: see original paper], the DAQ circuit primarily consists of the front-end preprocessing unit (Pre-Processing Unit, PPU) and the data processing unit (Data Processing Unit, DPU). The PPU amplifies and filters the raw voltage signals output by the AFE, shaping them before they are sampled by the on-board 14-bit ADC and converted into digital signals. These digital signals are then forwarded to the DPU for further signal processing and computation. The DPU handles data flow algorithm processing, transmission,

command reception and parsing, as well as clock control. An image of the DAQ circuit board is shown in Fig. 8 [Figure 8: see original paper].

PPU Unit The PPU (Pre-Processing Unit) consists of four main components: a matching and protection circuit, a gain amplification circuit, an anti-aliasing filter, and an ADC sampling circuit. To minimize signal reflection and enhance measurement accuracy, terminal matching is used at the input for proper impedance matching. The filter shaping circuit is used to eliminate high-frequency noise. To simplify the circuit structure while achieving optimal filtering performance and serving as the driver circuit for the ADC, the design adopts a second-order low-pass anti-aliasing filter characterized by low noise, low distortion, and wide bandwidth as the driving circuit.

DPU Unit The hardware structure of the DPU unit consists mainly of a Field-Programmable Gate Array (FPGA) and its peripheral circuits, providing the sampling clock for the ADC and supplying clock and synchronization signals for the internal data processing modules of the FPGA. The DPU also includes multiple interfaces to control the AFE circuit. The data transmission interface includes an optical fiber transmission interface and a Universal Serial Bus (USB) interface. The host computer sends instructions to the FPGA via USB. After receiving the instructions, the FPGA controls operations such as ADC sampling and FIFO caching, and then transmits the acquired signals to the host computer through the USB transmission circuit.

System Firmware Design

The system firmware design has two main parts: one controls the high-speed switches and signal reading of the gated integrator on the AFE board using a CPLD, while the other manages ADC sampling, data processing, packaging, uploading, and communication with the host computer.

AFE Circuit Firmware Design

Fig. 9 [Figure 9: see original paper] shows the diagram of the gated integrator, where different capacitors can be selected based on the input. Fig. 10 [Figure 10: see original paper] illustrates the complete integration cycle, consisting of four stages: discharge, wait, integration, and hold.

1. **Discharge**: SH is set to high and SR to low, grounding the capacitors in the gated integrator and starting the discharge.
2. **Wait**: Set both SH and SR to high to prepare for integration, disconnecting SR to prevent charge flow to the ground. The wait time should be at least 10 ps for stabilization.
3. **Integration**: SH is set to low and SR to high, activating SH and charging the capacitor.

4. **Hold**: Set both SH and SR to high, deactivating SH and halting the integrator' s operation.

The AFE firmware design involves the CPLD' s logic control of the dual-gated integrator, multiplexer, and other components. The timing diagram is shown in Fig. 11 [Figure 11: see original paper], where Clock is the system clock provided by an external crystal oscillator; TrigIn is the external trigger signal corresponding to the operating cycle. SHA and SHB are the integration switches for integrators A and B, respectively, while SRA and SRB are the discharge switches for integrators A and B, all of which are active low. Daqtrig is the acquisition trigger signal sent from the AFE circuit to the DAQ circuit, instructing the ADC when to sample data. OUTPUT refers to the output signals, where channel A corresponds to integrator A' s output, and channel B to integrator B' s output.

DAQ Circuit Firmware Design

The DAQ circuit firmware design mainly includes logic control for FPGA data framing and packaging, AFE triggering, USB commands, and data transmission.

AFE Triggering, USB Commands, and Data Transmission The AFE trigger signal, TrigIn, defines the circuit' s operation. The AFE operates based on the period of TrigIn, with integration duration and gain directly related to its period. The system diagram for AFE triggering, USB commands, and data transmission is shown in Fig. 12 [Figure 12: see original paper].

The host computer sends commands and integration duration via USB to the FPGA in the DAQ circuit. The FPGA parses the commands, restores the waveform, and generates a correct TrigIn signal, which controls the AFE' s operation time and cycle. Once the AFE is active, the output signal is sampled by the DAQ circuit, and the FPGA processes and packages the data, which is then uploaded to the host computer via USB. Fig. 13 [Figure 13: see original paper] illustrates the complete process of a read-write operation state transition between the FPGA and USB. The fifo empty and fifo full signals shown in the figure represent the FIFO status signals of the USB chip.

Reading Process: 1. **Idle state**: After reset, the system waits for the trigger condition in the IDLE state. 2. **Reading state**: If the read enable is active and the FIFO is not empty (Rd_{en} & !fifo_{empty}), the system enters the reading state, where the FPGA performs the read operation and increments the read counter. Otherwise, it returns to the IDLE state. 3. **Continue reading or waiting state**: After reading one data point, the system checks if the read enable is active and the FIFO is not empty (Rd_{en} & !fifo_{empty}). If valid, it continues reading data; otherwise, it transitions to the IDLE state waiting for the trigger condition.

Writing Process: 1. **Idle state**: After reset, the system waits for the trigger condition in the IDLE state. 2. **Writing state**: If the write enable is active and

the FIFO is not full (Wr_{en} & !fifo_{full}), the system enters the writing state, where the FPGA performs the write operation and increments the write counter. Otherwise, it returns to the IDLE state. 3. **Continue writing or waiting state**: After writing one data point, the system checks if the write enable is active and the FIFO is not full (Wr_{en} & !fifo_{full}). If valid, it continues writing data; otherwise, it transitions to the IDLE state waiting for the trigger condition.

Data Framing and Packaging After the ADC samples and quantizes the analog voltage signal, it outputs a 14-bit parallel data stream. The signal is framed in a specific data format for easy extraction and analysis. As shown in Fig. 14 [Figure 14: see original paper], each data set consists of 33 sampling points. The framed data is stored in an asynchronous FIFO (First In, First Out) buffer, from which the data packaging module packages and transmits the data. The header (55AA) and footer (5AA5) identify the packet, with the second bit indicating the channel (integrator A or B). Bits 3 to 6 are reserved for future use, while the remaining bits contain the 33 sampled data points.

Baseline Restoration The ADC sampled data is temporarily stored in the FIFO. When the data read condition is met, the FIFO read enable is triggered to retrieve the data, which serves as the basis for subsequent pulse baseline calculations. Since baseline drift may occur due to the detector and conditioning circuitry, baseline calibration is required. The FPGA controls the ADC to sample N points and compute the average, yielding the current baseline value, B_{AVG}, as shown in Eq. (7):

$$B_{AVG} = \sum V_i$$

Where V_i is the amplitude of the ith sampled waveform point.

After baseline calculation, the charge is determined by summing the data of M sampled points, as shown in Eq. (8):

$$\sum (V_i - B_{AVG}) \cdot \Delta t$$

Where K is the conversion gain of the conditioning circuit, and Δt is the sampling time for each sample.

Real-Time Host Computer Software Design The host computer software interface, shown in Fig. 15 [Figure 15: see original paper], allows for selecting the data format, setting the integration duration, and configuring the FPGA. The right side displays a plotting area where data is processed by two threads: one stores the data in a ".dat"file, while the other performs real-time analysis and plotting. During event analysis, 33 sampled points can reconstruct the complete waveform. However, since this work focuses on amplitude, the points from the

20th to the 30th, where the amplitude is stable, are selected for calculation. To minimize errors from baseline drift, the first five points of the 33 are used as baseline pre-samples. The accurate peak-to-peak amplitude is obtained by subtracting the baseline from the stable amplitude value. The AFE system uses a dual-gated integrator architecture, and to reduce errors introduced by the integrators, standard charge values are used in the host software to correct both integrators A and B.

Performance Test

Electronics Performance Test

Calibration of the Integration Capacitance In laboratory tests, a 100 pF on-chip integrating capacitor is used for integration. Fig. 16 [Figure 16: see original paper] shows the linearity characteristics between the integrator' s measured and theoretical charge outputs at different integration times (20 µs, 50 µs, 100 µs, 500 µs). The red squares represent the theoretical charge output, while the black (500 µs), gray (100 µs), blue (50 µs), and green (20 µs) squares represent the measured charge output for various conditions.

Significant deviations are observed, primarily due to the discrepancy between the actual and nominal values of the integrator capacitor. To reduce this error, the capacitance was calibrated, and the results were compensated using the corrected capacitance. After calibration, as shown in Fig. 17 [Figure 17: see original paper], the error between the measured and theoretical charge outputs is significantly reduced, with measurements closely matching the theoretical values. The maximum nonlinear error after correction is 0.62% (the linear correlation coefficient $R^2 = 0.99992$).

Nonlinear Error Test With the integrator capacitor fixed at 100 pF, the measurable current dynamic range varies with different integration times. Five integration times are selected as distinct ranges, and fitting is performed using Origin to calculate the nonlinear error over the entire range. The results are shown in Table 2 . When the integration time is 1 s and the capacitor is 0.5 pF, the laboratory-measured minimum current range is -1 pA to 1 pA.

Fig. 18 [Figure 18: see original paper] shows the linear fit curve for the entire measurement range. The nonlinear error of the range from -190 µA to 200 µA is 0.67% and the coefficient of determination is $R^2 = 0.99992$. The tests demonstrate that the system offers high accuracy, a wide dynamic range, good linearity, and excellent performance in ultra-low current measurements.

Beam Experiment

The beam experiment was conducted at the Heavy Ion Research Facility in Lanzhou (HIRFL-TR4), which supports research on heavy ion cancer therapy and clinical trials for treating superficial tumors in humans. The beam exper-

iment layout is shown in Fig. 19 [Figure 19: see original paper]. The carbon ion beam is extracted into the atmosphere, passing through a dose ionization chamber detector, which converts the ion signal into a current. This current is then input into the real-time dosimetry monitoring system. The host computer, located in the control room, remotely controls data acquisition via cables.

To verify the system's real-time monitoring capability at high dose rates, in April 2024, after the complete electronics system was finished, beam tests were performed with an ionization chamber detector at the TR4 terminal of the Heavy Ion Research Facility in Lanzhou (HIRFL). The TR4 terminal uses heavy ions with varying dose rates for fundamental research. In conventional and high dose rate radiotherapy, the dose rate is typically below 20 Gy/min. Monitoring at higher dose rates imposes stricter demands on the system' s dynamic range, response rate, stability, and accuracy. To evaluate the system' s real-time monitoring performance at higher dose rates, this experiment set the beam dose range between 65 Gy/min and 120 Gy/min. The terminal dose is updated every second, with the AFE circuit using a 10 pF capacitor and an integration time of 16 µs, corresponding to 62,500 events per second. After analyzing the sampled current signals, a linear fit curve of ionization chamber output current versus dose variation is shown in Fig. 21 [Figure 21: see original paper]. Each data point represents the current at different beam dose levels, and the coefficient of determination is $R^2 = 0.9998$. The results show that the system can stably operate at dose rates up to 120 Gy/min, meeting the real-time monitoring requirements for both conventional and high dose rate radiotherapy, and demonstrating potential for application in ultra-high dose rate radiotherapy (FLASH-RT).

The field image of the test is shown in Fig. 20 [Figure 20: see original paper], which includes the ionization chamber detector (a), which transmits the current signal to the AFE (b) for voltage conversion. The DAQ (c) samples and processes the signal, with results displayed on the host computer.

Discussion

In 2010, Furukawa and Torikoshi M from the National Institute of Radiological Sciences (NIRS), Japan, measured dosimetry for HIMAC with a range of 1 nA to 1000 nA, a nonlinear error of less than 1%, and a dose rate of approximately 1 Gy/min [**?**, **?**]. In 2017, Binqing Zhao from the Shanghai Institute of Applied Physics, Chinese Academy of Sciences, developed a proton therapy beam delivery system with a dosimetry range of -400 nA to -60 nA, a dose rate of about 2 Gy/min, and a maximum linear error of $\pm 0.04 nA$[**?**]. $In 2020, Eric S. Diffender fer's team at the University of Pennsylvania designed a proton FLASH-RT system with a dose rate of 60-100 Gy/s and a maximum beam current of 300 nA, showing a linear relationship be$ = 0.9952$) [**?**]. In 2024, Yagi M and colleagues developed dosimetry electronics for HIMAC' s UHDR carbon ion beam with a range of -0.5 µA to -50 µA, dose rates up to 102.54-115.38 Gy/s, and a linear relationship between ion chamber current and electronics output frequency within $\pm$1% [**?**].

Compared to existing dosimetry electronics systems, this system offers a measurement range of $±$1 pA to $±200A, capable of reading both positive and negative signals, with a nonlinear erro 0.62R^2 = 0.99992$). It meets the ionization chamber current monitoring needs of most conventional and FLASH-RT dose detectors. Owing to the fact that domestic FLASH radiotherapy terminals are still in development, this system has not yet been validated with FLASH beams. Nonetheless, its wide dynamic range, high linearity, and dead-time-free features demonstrate significant potential for future FLASH-RT research and clinical applications.

Conclusion

This work demonstrates an innovative real-time dosimetry monitoring system for heavy ion radiotherapy, validated experimentally on the TR4 terminal. The system detects bipolar currents within a range of -190 µA to 210 µA, maintains a nonlinear error below 0.67%, and offers a single-event processing time as fast as 5 µs. The system achieved high-accuracy real-time monitoring within a dose rate range of 65-120 Gy/min in beam experiments. Compared to existing radiotherapy dosimetry systems, it eliminates signal processing dead time in the front-end circuit, ensuring continuous and accurate dose measurements. The system' s current measurement range spans eight orders of magnitude ($±$1 pA to $±$190 µA), greatly enhancing its versatility across different applications. This system is optimized for high-precision monitoring of ionization chamber output currents and is compatible with various radiotherapy modes. It is suitable for real-time dose measurement in heavy ion radiotherapy and can be extended to electron, proton, and other high-energy particle radiotherapies, demonstrating broad application potential.

To meet the growing demand for higher dose rates and support cutting-edge applications like FLASH-RT, we are developing a new generation of ultra-fast front-end processing circuits and data acquisition systems. This system will offer a sampling rate up to 250 MHz, data transmission speeds over 10 GHz, and a wider input dynamic range, enhancing real-time monitoring capabilities in high dose rate environments. These improvements will not only expand the system' s applicability in high dose rate radiotherapy but also provide a more reliable real-time dosimetry solution for accurate radiotherapy.

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