Design and Implementation of the Resistive Micromegas Tracker Electronics Prototype

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Abstract

The large-scale detector spectrometer for the SuperTau-Charm Facility (STCF) will provide a unique platform for frontier research in particle physics. The cylindrical resistive micro-well inner tracker (Inner Tracker, ITK), positioned at the center, is one of the key components for low-momentum particle track reconstruction due to its low material budget, high counting rate, and high spatial resolution capability. This paper addresses the physical requirements of the resistive micro-well detector, conducts key technology research on high charge-resolution readout electronics, and develops a 1024-channel highly integrated, high-performance readout electronics prototype. The system comprises ASIC readout units, front-end electronics boards, data aggregation boards, and other circuits, featuring a reasonable structure and easy expandability. Laboratory simulations and board-level testing results indicate that the system functions as expected, with metrics such as charge resolution and integral nonlinearity meeting the requirements, thus providing solid technical support for subsequent engineering implementation.

Full Text

2 System Design

The Super Tau-Charm Facility (STCF) is a next-generation electron-positron collider being planned in China, operating in the tau-charm energy region with a center-of-mass energy range of 2-7 GeV and a peak luminosity exceeding 0.5$×10^{35}$ cm^{-2} s^{-1}. It provides a unique platform for research in quantum chromodynamics (QCD) confinement and nucleon structure, electroweak (EW) unification and CP symmetry violation, and new physics searches, with the potential for major breakthroughs. In addition to linear and circular accelerators, the STCF main complex includes a large integrated particle detection spectrometer at the collision point, comprising subsystems such as the Inner

Tracker (ITK), Main Drift Chamber (MDC), Particle Identification detector (PID), Muon Detector (MUD), Electromagnetic Calorimeter (EMC), and a large superconducting magnet [1]. The system must achieve precise measurement of final-state particle energy and momentum, high detection efficiency, and particle identification capability under extreme conditions. The ITK, located at the innermost layer of the spectrometer, must provide charged particle track position measurements with hundred-micron precision under high background, high counting rate, and high radiation conditions. The resistive micro-well detector, with its low material budget, high counting rate capability, and excellent position resolution, represents an important candidate for the STCF-ITK. This paper addresses the physical objectives of the resistive micro-well detector by conducting research on critical technologies for high-timing, high-charge-precision readout electronics and developing a prototype system to prepare for future engineering implementation.

According to the development plan, the ITK subsystem consists of three coaxial gas detector layers based on R-WELL microstructures, with active diameters of 131 mm, 229 mm, and 328 mm, and lengths of 380 mm, 650 mm, and 920 mm, respectively. To facilitate routing, all readout units will be installed at one end of the cylindrical detector, with the total number of readout channels expected to reach tens of thousands [2]. Given the large scale of the readout electronics, a 1024-channel prototype was developed in the initial project phase to reduce costs while fully verifying the technical feasibility. To ensure precise particle energy measurement in high-luminosity collision experiments, the prototype readout electronics system must meet requirements for high precision, low noise, high integration, and scalability. Specific performance targets include: 1024 total readout channels, charge resolution better than 5 fC RMS, equivalent noise charge better than 1.3 fC RMS, integral nonlinearity better than 2%, and a dynamic range of 0–20 fC.

Traditional discrete-component readout methods cannot meet these channel density requirements. Adopting an appropriate ASIC to read the analog signals from the ITK detector significantly improves system integration and reduces power consumption. To satisfy scalability requirements, the prototype readout electronics system employs a three-tier architecture, as illustrated in Figure 1 [Figure 1: see original paper]. The architecture comprises the ASIC Readout Unit (ARU), Front-end Electronics Board (FEB), and Data Collection Board (DCB). The first-tier ARU directly reads detector signals and must be mounted close to the detector for optimal signal-to-noise ratio. The second-tier FEB receives the sampled and amplified detector signals from the ARU, performs digitization and primary data aggregation, and transmits the data via optical fiber to the corresponding DCB for secondary data selection and aggregation. The final-tier DCB reads all front-end data and delivers it to the DAQ subsystem server for storage through a higher-bandwidth communication interface.

2.1 ASIC Readout Unit

The APV25 is a mixed-signal ASIC fabricated in 250 nm CMOS technology, originally designed for the silicon strip detector readout system of the CMS experiment. With a power consumption of approximately 2.31 mW per channel at a 128 A reference current under nominal settings, an equivalent noise charge as low as 0.043 fC, and support for counting rates up to 285 kHz, the APV25 was selected as the front-end readout ASIC [3].

The APV25 front-end board measures 5 cm × 7.5 cm and utilizes mature circuit technology to facilitate design verification and risk reduction for subsequent circuits; it can later be replaced by a functionally equivalent in-house ASIC after technical validation. The board core is an APV25 chip mounted on a PCB using chip-on-board (COB) technology, providing 128 analog input channels. Each channel includes an independent charge-sensitive preamplifier, CR-RC shaping filter, 192-cell analog pipeline, and gain control circuit. Under a maximum clock frequency of 40 MHz, all channel input signals are simultaneously amplified, shaped, sampled, and stored. Upon receiving an external trigger, the APV25' s internal DSP is activated to read the pipeline signals, construct analog signal frames, and output them time-division multiplexed through a single LVDS interface. The APV25 supports three operating modes—Peak, Deconvolution, and Multi-mode—configurable via a standard I2C interface. Peak mode suits moderate event rates with insignificant pile-up and requires high signal-to-noise ratio. Deconvolution mode handles high event rates with significant pile-up. Multi-mode, which enables continuous sampling of all sample points, is ideal for calibrating input pulse signals at low event rates. For engineering applications, the APV25 operates in Peak mode to maximize signal-to-noise ratio, while laboratory testing employs Multi-mode with 30 consecutive samples per event for comprehensive waveform observation. All three modes share a unified output frame format consisting of a frame header, address, error flags, and an analog signal segment containing one sample point from all 128 channels.

To simplify interfacing and wiring, each ARU integrates two APV25 front-end boards cascaded via a backplane using two Molex 547220304 connectors [4]. Each APV25 front-end board interfaces with the detector through an Fx10a-140 high-density connector. The backplane also features a 19-pin universal HDMI interface that connects to the downstream FEB using a single HDMI Type-A cable, offering the significant advantage of integrating power, clock, trigger, and I2C slow-control interfaces to greatly enhance system integration [5].

2.2 Front-end Electronics Board Hardware

The FEB serves as the core circuit of the second-tier node, comprising a high-performance FPGA, ADC digitization circuit, front-end operational amplifiers, clock and trigger circuits, and associated interfaces, as shown in Figure 2 [Figure 2: see original paper]. Each FEB provides four HDMI interfaces to connect four ARUs. During operation, global clock and trigger signals are input through

dedicated interfaces, synchronized and fanned out to all HDMI interfaces by an on-board Xilinx Kintex-7 series FPGA, then transmitted via cable to the APV25 front-end boards in the ARUs. Simultaneously, the differential current signal frames from the APV25s return through the same HDMI interface to the FEB, where they undergo current-to-voltage conversion before being fed to a differential analog signal buffer that amplifies them to match the ADC' s dynamic range.

Given that the APV25' s sample switching time is 25 ns under a 40 MHz clock, the buffer' s 3 dB bandwidth must exceed 140 MHz when calculated using 10% of the switching time as the rise/fall time for the output analog signal. The AD8138 from Analog Devices, offering a 3 dB bandwidth of 320 MHz at unity gain, satisfies this requirement and was selected as the differential analog signal buffer. Considering that the quantization error of a 12-bit ADC is 0.122%, the corresponding noise is approximately 0.00244 fC under the APV25' s 20 fC dynamic range, meeting system requirements. Accounting for the APV25' s sample switching time, the ADS52J90 from Texas Instruments was chosen as the analog-to-digital converter, configured to operate at 12-bit resolution and 40 Msps sampling rate. After digitization by the ADS52J90, data from eight APV25 signal frames are input to the FPGA for discrimination, framing, and primary aggregation, then transmitted through a high-speed optical fiber interface to the downstream DCB for secondary aggregation. For convenient standalone debugging, the FEB also includes a USB 3.0 interface that enables direct data transfer to a host computer without requiring the third-tier DCB [6].

2.3 Front-end Electronics Board Firmware

The FEB' s on-chip FPGA must not only manage trigger and clock synchronization, read signals from upstream ARUs, perform digitization and data processing, and handle system configuration, but also implement high-speed communication of data streams, status streams, and command streams with the downstream DCB. Accordingly, the FEB firmware is primarily divided into a control unit, data processing unit, transceiver unit, and clock/reset unit, as illustrated in Figure 3 [Figure 3: see original paper]. The control unit comprises a command/status transceiver, ADC driver, APV25 driver, and status monitoring ADC driver modules. The data processing unit includes synchronization and deserialization, frame decoding, baseline calculation, data sorting, data compression, data framing, and data frame scheduling modules. The transceiver unit contains GTX transceiver and USB transceiver modules. The clock/reset unit encompasses clock fanout, trigger fanout, and global reset modules.

2.3.1 Overall Logic Design From power-on to normal operation, the FEB undergoes two phases: initialization/configuration and regular acquisition. In the first phase, the FPGA receives reset and configuration command sets forwarded by the DCB from the host computer via external communication in-

terfaces, parses and executes them through an internal status transceiver to complete reset initialization of all logic functional modules, associated circuits, and operating modes. To minimize configuration time, the FEB synchronously configures all eight APV25 front-end boards using broadcast mode and reads back the status of individual boards via unicast communication. Upon completion of this phase, the system enters a standby state. When a particle event occurs, the system automatically transitions to the second phase, where the FPGA generates corresponding trigger sequences under external trigger excitation and fans them out to the eight APV25 front-end boards. The APV25 boards activate and return signal frames to the FEB, which are digitized by the on-board ADC and input to the FPGA' s internal data processing unit. The data processing unit sequentially performs synchronization and deserialization, frame decoding, baseline calculation, data sorting, and data compression on the ADC parallel data frames. The processed data is then input to corresponding framing modules for encapsulation and subsequently written to eight first-level FIFOs for one-to-one caching. Concurrently, the data frame scheduling module continuously polls the status flags of all first-level FIFOs; when a non-empty FIFO is detected, indicating a particle event, the round-robin arbiter within the module sequentially empties all FIFOs and transfers the aggregated data to a large-capacity second-level FIFO. Finally, the transceiver unit reads the data and transmits it to the DCB via the GTX module over the fiber link. Considering that a single APV25 generates a maximum data bandwidth of 480 Mbps, eight APV25s reach 3.84 Gbps. After framing by the raw data framing module with additional fields, the bandwidth requirement becomes 5.01 Gbps, and with 8B/10B encoding, the data bandwidth demand reaches 6.26 Gbps. Therefore, configuring the GTX hard core' s data link bandwidth to 10 Gbps is more appropriate.

2.3.2 Data Processing Core Logic Design The data processing sub-unit framework is shown in Figure 4 [Figure 4: see original paper]. The firmware operating modes are divided into raw mode and compression mode based on the processing level applied to APV25 output data. In raw mode, all channel data enters the raw mode framing module for direct encapsulation, resulting in large data volumes and high transmission bandwidth requirements. In compression mode, all channel data undergoes data sorting and compression processing before encapsulation by the compression mode framing module. Consequently, baseline calculation, data sorting, and data compression constitute the core logic of the APV25 data processing sub-unit.

To achieve channel consistency and eliminate temperature drift effects, baseline calibration must be performed before acquiring detector signals. The baseline calculation module employs an averaging method to continuously compute the mean of a given number of baseline samples and uses the Cordic IP core in the FPGA to calculate the root-mean-square (RMS) value. The computed baseline mean and RMS values for all 128 channels are stored in two dual-port RAMs for access by the data compression module. Since the APV25 data frame employs

a time-division multiplexing format, the data must first be input to the data sorting module for demultiplexing to facilitate subsequent compression processing. The sorting module first completely caches N APV25 data frames, then extracts data from each time slot according to the APV25 frame format and distributes it to the corresponding channels, finally restoring the 128-channel raw waveform data for serial input to the data compression module.

The data compression module provides baseline subtraction, valid channel selection, and charge/time data extraction, significantly reducing invalid data transmission and alleviating downstream storage pressure. The module first subtracts the corresponding baseline mean from each channel' s raw waveform data to obtain baseline-corrected waveform data. It then accumulates the data across 0–N−1 sample points, takes the absolute value as the waveform area, and uses a threshold derived from the baseline RMS multiplied by a coefficient α and the number of sample points N. This threshold is compared with the waveform area to screen valid channels, as expressed in Equation (1). Compared with thresholding based on individual sample values of baseline-subtracted waveforms, this area-based method effectively avoids excessive crosstalk and noise effects, thereby improving screening stability. Simultaneously, a peak-finding module determines the peak amplitude and sample point of the baseline-subtracted waveform as the charge and time data. When valid channels are identified, their channel numbers, charge data, and time data are temporarily stored in an array. Finally, the compressed data framing module outputs data in the variable-length frame format shown in Figure 5 [Figure 5: see original paper], where the data segment can optionally include zero-suppressed data or further charge/time extraction data.

[*{i=0}^{N-1}(P_i - B*{mean}) > N B_{rms}]

where (N) is the number of sample points, (P_i) is the amplitude of each sample point, (B_{mean}) is the baseline mean, (B_{rms}) is the baseline RMS value, and ( ) is a given coefficient.

2.4 Data Collection Board

The DCB is existing hardware within the group that primarily handles secondary aggregation, buffering, and transmission of FEB output data, as well as reception and forwarding of host computer commands. The DCB board integrates a high-performance FPGA chip, DDR4 memory chips, QSFP+ optical interface circuits, and PCIe interface circuits. The FPGA employs Xilinx' s Kintex Ultrascale series, which incorporates GTH high-speed transceiver hard cores and PCIe hard cores, providing robust hardware support for data transmission. For data transfer, the DCB communicates with up to four FEBs via four full-duplex optical links (each up to 10 Gbps), implemented through the GTH transceiver hard cores and QSFP+ optical modules. Additionally, the DCB supports interaction with the host computer via eight PCIe Gen3 links (each at 8 Gbps), leveraging the integrated PCIe hard core in the Kintex Ultra-

scale FPGA. Furthermore, the DCB is equipped with four DDR4 SDRAMs for the FPGA, offering a total capacity of 16 Gbits and a maximum data rate of 2400 Mbps to support data processing and buffering [7-8].

3.1 Firmware Simulation

To verify the functionality of the FEB firmware—the core component of the readout system—and provide more direct feedback, simulation testing of the firmware system was conducted using the Vivado platform.

3.1.1 Baseline Calculation Function Simulation

In this simulation, a Testbench was used to generate digitized APV25 output baselines with ADC code values in the range of 700–730. The results are shown in Figure 6 [Figure 6: see original paper]. The baseline calculation module obtained channel-specific baseline means of 714–715 codes and computed an RMS value of 9 codes using the Cordic IP core, confirming that the results meet expectations.

3.1.2 Data Compression Function Simulation

This simulation modeled the processing of APV25 waveform data from one channel through the data compression module. The results are presented in Figure 7 [Figure 7: see original paper], where the raw waveform peak occurs at sample point 5 with an absolute amplitude of approximately 1000 codes. The compression module' s comparison logic first subtracts the baseline mean from the raw waveform to obtain baseline-corrected data, then calculates the waveform area using the area method. Simultaneously, it compares against the compression threshold to generate a valid waveform flag and invokes peak-finding logic to obtain the peak time and amplitude. The results correctly identify the peak time as 5 with an absolute amplitude near 1000 codes, consistent with peak-finding expectations.

3.1.3 Dead Time and Data Volume Simulation

To characterize the firmware system' s processing dead time and data volume, a simulation test was performed. The simulation modeled periodic signal frames output by the APV25 under continuous sampling of 30 sample points or a single sample point, with the firmware configured in either raw or compression mode. The resulting dead times and per-event data volumes are listed in Table 1 . The APV25 signal frame duration is 3500 ns, during which the APV25 cannot sample another input signal, yielding a processing dead time of 105,000 ns for continuous 30-sample acquisition. The table shows that in compression mode with 30 samples, the firmware processing dead time slightly exceeds the APV25 processing dead time, but compared to raw mode with 30 samples, the data volume is dramatically reduced with a compression efficiency approaching

98%. Thus, when continuously acquiring multiple samples, the compression-mode firmware system significantly reduces data volume at the cost of only a modest increase in dead time.

3.2 Laboratory Testing

To evaluate the charge measurement performance of the prototype system, relevant board-level verification tests were conducted in the laboratory, as shown in Figure 8 [Figure 8: see original paper]. A signal generator provided both trigger and test signals: a digital signal generator supplied periodic exponentially decaying calibration signals and system trigger signals through two channels, with amplitude adjusted by an attenuator and finally distributed to all APV25 analog input channels via a custom charge injection board [9].

3.2.1 Noise Test

To obtain accurate baseline data, all APV25 boards were configured in multi-peak mode with their analog inputs left floating, and the system was activated. Data from 1000 events were histogrammed and fitted with a Gaussian distribution, yielding the results shown in Figure 9 [Figure 9: see original paper]. The signal waveform mean was 728.8 codes with a root-mean-square (sigma) of approximately 8 codes. Based on the conversion factor of 0.02 fC per ADC code, the system' s equivalent noise charge is 0.16 fC, satisfying the prototype electronics requirement of better than 1.3 fC.

3.2.2 Signal Waveform Test

When a signal is present at the analog input, the APV25 board should output a quasi-Gaussian response waveform. This was verified by configuring the APV25 in multi-peak mode and injecting a full-scale charge of 20 fC. The APV25' s internal shaping circuit has a 50 ns shaping time with 25 ns sample intervals. Offline analysis yielded the reconstructed waveform shown in Figure 10 [Figure 10: see original paper]. At a 20 fC input, the amplitude ranges from 750 to -450 codes, and the rising edge spans two sample points (50 ns), consistent with chip specifications.

3.2.3 Charge Resolution Test

Charge resolution is the most critical metric for the ITK detector, as it indirectly reflects particle identification capability. To measure this, the APV25 was configured in multi-peak mode and injected with a typical charge of 12 fC. Data from 1000 events were histogrammed and fitted with a Gaussian distribution, producing the charge resolution spectrum shown in Figure 11 [Figure 11: see original paper]. Analysis reveals a charge resolution of approximately 0.13 fC, far exceeding the prototype electronics requirement of better than 5 fC.

3.2.4 Integral Nonlinearity Test

To characterize the system' s linear operating region, input charges from 2–20 fC in 2 fC steps were applied, and integral nonlinearity was tested in both multi-peak and single-peak modes. The results are shown in Figure 12 [Figure 12: see original paper]. Linear fitting indicates that single-peak mode achieves better integral nonlinearity (1.9%) than multi-peak mode across the full dynamic range. However, due to the chip' s inherent design, the linearity exhibits clear segmentation: the 0–12 fC region shows excellent linearity with results better than 0.26%, while the 12–20 fC region suffers from significant signal amplification distortion and degraded performance, as documented in related literature [10]. Since the ITK detector prioritizes charge resolution and the detector gain can be adjusted to match the APV25' s optimal linear region, the linearity test results remain acceptable.

3.2.5 Channel Consistency Test

To evaluate channel consistency within a single APV25, baseline signals were acquired from all channels without signal input. The baseline data were analyzed to obtain and store the mean values for each channel. When new signals were acquired, the stored baseline means were subtracted. The channel consistency results are shown in Figure 13 [Figure 13: see original paper]. Before baseline subtraction, the dispersion of the 128-channel means was 28.16 codes; after subtraction, this reduced to 0.71 codes. Baseline subtraction thus significantly improves channel consistency, thereby enhancing charge resolution.

3.2.6 Fiber Transmission Test

To evaluate fiber transmission performance, an eye diagram test was conducted. The eye scan results are presented in Figure 14 [Figure 14: see original paper]. With the fiber link bandwidth set to 10 Gbps, the eye opening ratio is 55% and the bit error rate (BER) is 2.486$×10^{-14}$. Both metrics demonstrate that the FEB' s fiber hardware interface design is robust and meets the data transmission bandwidth requirements for raw mode operation.

4 Conclusion and Outlook

This paper presents the development of a 1024-channel, highly integrated, high-performance APV25 readout electronics prototype for the ITK detector in the context of the STCF major scientific project. The system consists of ASIC readout units, front-end electronics boards, and data collection boards. Except for the APV25 boards, which were imported through international collaboration, all other components were independently developed. Through flexible firmware design, the system can operate in multiple modes and run stably, providing a solid technical foundation for the ITK subsystem engineering implementation. Future development will focus on replacing the front-end readout circuit with

an in-house ASIC to further enhance independent intellectual property rights and facilitate subsequent maintenance and upgrades.

Design and Implementation of Electronic Prototype for Micro-Resistive Well Detector

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Abstract: The large-scale detector spectrometer to be employed in the Super Tau-Charm Facility (STCF) will provide a unique platform for cutting-edge particle physics research. Among its components, the cylindrical Resistive Micro-Well Inner Tracker (ITK), located at the core, is one of the key detectors for low-momentum particle trajectory reconstruction due to its low material budget, high counting rate, and excellent spatial resolution. This paper focuses on the physical requirements of the resistive micro-well detector and conducts research on critical technologies for readout electronics with high charge resolution. A highly integrated, high-performance 1024-channel readout electronics prototype has been developed. The system consists of ASIC readout units, front-end electronics boards, and data aggregation boards, featuring a rational and scalable architecture. Laboratory simulations and board-level tests demonstrate that the system functions as expected, with charge resolution and integral nonlinearity meeting specifications. These results provide strong technical support for further engineering development.

Keywords: Super Tau-Charm Facility; micro-Resistive WELL detector; Field-Programmable Gate Array; Data Compression; Charge Measurement

Note: Figure translations are in progress. See original paper for figures.