Dependence of Single-Event Upset Susceptibility on Back-Gate Bias and Supply Voltage in 6T CSOI SRAM

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Abstract

This paper explores the impact of back-gate bias (Vsoi) and supply voltage (VDD) on the single-event upset (SEU) cross section of 0.18 µm configurable silicon-on-insulator (CSOI) static random-access memory (SRAM) under high linear energy transfer (LET) heavy-ion experimentation. The experimental findings demonstrate that applying a negative back-gate bias to NMOS and a positive back-gate bias to PMOS enhances the SEU resistance of SRAM. Specifically, as the back-gate bias for N-type transistors (Vnsoi) decreases from 0 to −10 V, the SEU cross section decreases by 93.23%, whereas an increase in the back-gate bias for P-type transistors (Vpsoi) from 0 V to 10 V correlates with an 83.7% reduction in SEU cross section. Furthermore, a significant increase in the SEU cross section was observed with increasing supply voltage, as evidenced by a 159% surge at VDD = 1.98 V compared with the nominal voltage of 1.8 V. To explore the physical mechanisms underlying these experimental data, we analyzed the dependence of the critical charge of the circuit and the collected charge on the bias voltage by simulating SEUs using technology computer-aided design (TCAD).

Full Text

Preamble

Back-Gate Bias and Supply Voltage Dependency on the Single-Event Upset Susceptibility of 6T CSOI SRAM

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This paper investigates the impact of back-gate bias (Vsoi) and supply voltage (VDD) on the single-event upset (SEU) cross-section of 0.18 μm configurable silicon-on-insulator (CSOI) static random-access memory (SRAM) under high linear energy transfer (LET) heavy-ion irradiation. Experimental results demonstrate that applying a negative back-gate bias to NMOS transistors and a positive back-gate bias to PMOS transistors significantly enhances SEU resistance. Specifically, as the back-gate bias for N-type transistors (Vnsoi) decreases from 0 to −10 V, the SEU cross-section decreases by 93.23%, while increasing the back-gate bias for P-type transistors (Vpsoi) from 0 V to 10 V yields an 83.7% reduction in SEU cross-section. Furthermore, the SEU cross-section increases substantially with rising supply voltage, showing a 159% surge at VDD = 1.98 V compared to the nominal voltage of 1.8 V. To elucidate the physical mechanisms underlying these experimental observations, we analyzed the dependence of critical charge and collected charge on bias voltage through technology computer-aided design (TCAD) simulations of SEUs.

Keywords: Single-event upset (SEU); Static random-access memory (SRAM); Back-gate voltage; Supply voltage

Introduction

With advancements in space science and technology, numerous spacecraft have been deployed to perform various functions in space. However, integrated circuits in these spacecraft are vulnerable to cosmic rays, which cause single-event effects (SEEs) and total ionizing dose (TID) effects [1]. Previous studies have shown that the SEU cross-section of static random-access memory (SRAM) cells increases as process nodes shrink [2, 3].

To mitigate the growing severity of SEEs, researchers have proposed radiation-hardened designs such as the dual interlocked storage cell (DICE), which significantly reduces device SEU cross-section [4–7]. Nevertheless, circuit-level hardening typically introduces adverse consequences, including increased power consumption, performance degradation, and larger footprint [8, 9]. Silicon-on-insulator (SOI) technology has been introduced to reduce circuit area and power

consumption while simultaneously decreasing integrated circuit sensitivity to SEEs. This technology incorporates a buried oxide (BOX) layer between the silicon film and substrate, which mitigates parasitic capacitance and short-channel effects while achieving complete dielectric isolation of electronic components [10–13].

Although SOI technology can substantially reduce the cross-section of transient radiation effects such as single-event transients (SETs), single-event latch-ups (SELs), and SEUs [14, 15], SOI devices exhibit reduced TID resistance due to the introduction of the BOX layer [16–19]. Cosmic rays can introduce trapped charges in the gate oxide, isolation oxide, and BOX layers, causing device parameter drift and degradation of electrical performance [20]. As technology nodes scale down, the fully depleted silicon-on-insulator (FDSOI) process enhances SEE susceptibility and gate-control capability by thinning the gate oxide and BOX layers [21]. However, the presence of a dopant trap region beneath the BOX layer constrains FDSOI back-gate bias range and reduces circuit design flexibility. Furthermore, the shallow trench isolation and BOX layer of FDSOI are highly susceptible to TID effects, leading to the formation of source-drain parasitic paths and reduction in effective channel width [22, 23].

Previous studies have demonstrated that a novel configurable silicon-on-insulator (CSOI) structure can effectively mitigate TID-induced damage and extend the back-gate bias range of devices [24, 25]. The CSOI process introduces two silicon layers: the top silicon film (SOI1) and an underlying SOI2 layer positioned beneath the conventional BOX layer. In CSOI devices, back-gate biasing is achieved using independent electrodes. This approach not only prevents back-channel formation during irradiation, reduces threshold voltage drift, and minimizes leakage current [26, 27] but also efficiently regulates the electric field within the BOX layer. By reducing threshold voltage drift and leakage current while effectively controlling the internal electric field of the BOX layer, independent dynamic compensation of TID effects is achieved [28]. CSOI implementation can regulate the drain region potential, thereby suppressing SEEs.

While experimental validation and simulation analysis of TID mitigation through CSOI back-gate bias have been comprehensive, studies examining the dependence of CSOI-SRAM SEUs on bias voltage under high-LET heavy-ion irradiation are lacking. This work investigates the influence of back-gate bias and supply voltage on SEU in CSOI SRAM through a combination of experiments and technology computer-aided design (TCAD) simulations. Additionally, we propose a physical mechanism wherein the trend of SEU cross-section variation with supply voltage exhibits opposite behavior at high and low LET values. This exploration has significant implications for understanding and hardening CSOI SRAM against SEUs.

Sections II and III describe the experimental setup and discuss the experimental results, respectively. Section IV presents the selection of physical models for TCAD simulation and configuration of simulation variables. We conducted

qualitative analysis to identify the sensitive state and sensitive region of the CSOI transistor, followed by simulations to explore the effects of back-gate bias and supply voltage on SEU sensitivity of the CSOI SRAM. Through simulations capturing variations in physical quantities such as transient pulse, potential, and collected charge of the SRAM off-state transistor under experimental parameters, we scrutinize and derive the physical mechanism underlying the influence of back-gate bias and supply voltage on SEU cross-section. This analysis explains and validates the experimental findings. Finally, Section V presents concluding remarks.

II. Experimental Setup

A. Experimental Device Description

The CSOI devices used in the experiments were fabricated using a 0.18 µm FDSOI process, with primary parameters and transistor sizes listed in Table 1 . The overall structure comprised two silicon layers (SOI1 and SOI2) and two buried oxide layers (BOX1 and BOX2). Electronic components were fabricated on the top silicon film, while the intermediate silicon layer (SOI2) was positioned between the two buried oxide layers to serve as a back-gate electrode. This electrode enabled adjustment of electrical performance and SEU resistance by modifying the voltage applied to SOI2. Consequently, both device electrical characteristics and SEU resistance could be tailored by varying the SOI2 voltage. The presence of the BOX layer mitigated the parasitic bipolar amplification effect and reduced leakage currents.

A 4k-bit 6T-SRAM provided by the Institute of Microelectronics of the Chinese Academy of Sciences (IMCAS) was employed to investigate the SEU resistance of SRAM fabricated using the CSOI process under varying back-gate biases. The chip package housed a 64 × 64-bit memory array with dimensions of approximately 1.45 mm × 1.45 mm, featuring a bit cell footprint of 10 µm × 8 µm. Within each memory cell, N-type transistors share an NSOI electrode (denoted Vnsoi), while P-type transistors share a PSOI electrode (denoted Vpsoi). The back-gate bias range of the SRAM extends from −10 to 10 V. The circuits were encapsulated in DIP-28 packages. Given the use of high-LET heavy ions in the experiment, the devices were decapped to ensure adequate penetration of the heavy ions.

B. Experimental Setup for Heavy-Ion Irradiation

For the experiments, Ta ions were selected from the TR5 terminal at the Heavy Ion Research Facility in Lanzhou (HIRFL) and the High Energy Heavy Ion Radiation Terminal (HERT) at the Space Environment Simulation and Research Infrastructure (SESRI) at Harbin Institute of Technology. The ion parameters are listed in Table 2 , with the fluence set to 5×10^6 ions/cm^2 for each experimental group. To achieve uniform heavy-ion beam distribution within the irradiated area, we adjusted the scanning current and frequency while precisely

controlling the irradiated area by manipulating the slit size.

Ta-ion irradiation was conducted in air, facilitated by the ability of the heavy-ion beam to reach the device' s sensitive region even after passing through a Ti window and traveling several microns in the atmosphere. The heavy ions traversed a vacuum/air transition foil before impinging on the device. To detect beam injection, we positioned an injection detector along the beam trajectory before the device under test. The LET of the ions from the device surface to the detector was adjusted by either inserting an energy attenuator (aluminum foil) into the heavy-ion incidence trajectory or employing angled ion impingement.

Experiments were conducted to investigate the impact of NSOI and PSOI electrodes, as well as power supply voltage, on SRAM SEUs. Before irradiation, 55+AA-type data were pre-written into the SRAM memory cells, with dynamic reading of the SRAM memory content performed during irradiation. Any discrepancies between read and write results were recorded by the test system as either 0$\rightarrow$1or1$\rightarrow$0$upsets, $dependingontheupsettypeobserved.Theseexperimentswereperformedatroomtemper
s to negate flux effects. A nominal supply voltage of 1.8 V was applied to the test system to simulate normal device operating conditions. Back-gate biases were uniformly set to zero to assess the effect of supply voltage on SRAM SEU. Six supply voltage biases were selected: pull-down 20% (1.44 V), pull-down 10% (1.62 V), pull-down 5% (1.71 V), nominal voltage (1.80 V), pull-up 10% (1.98 V), and pull-up 20% (2.16 V).

The SEU cross-section is calculated as:

$$\sigma_{seu} = \frac{N_{event}}{fluence \times N_{bit}}$$

where N_{event} is the total number of SEUs, and N_{bit} and fluence represent the SRAM memory cell capacity and experimental ion injection, respectively [29].

III. Discussion of Experimental Results

Analysis revealed that the total number of SEEs observed in this experiment consisted solely of single-bit upsets, with no occurrences of multiple-bit upsets or single-event functional interrupts. Figure 1 Figure 1: see original paper depicts the dependence of SEU cross-section on Vnsoi at LET = 86.1 MeV·cm^2/mg, with Vpsoi set to zero for all experiments. Notably, the SEU cross-section decreased by 47.31%, 87.82%, and 93.23% at Vnsoi = −2, −6, and −10 V, respectively, compared to the zero back-gate bias scenario. Conversely, Figure 1(b) shows the dependency of SEU cross-section on Vpsoi under the same LET conditions, with Vnsoi set to zero across all experiments. Here, the SEU cross-section decreased by 40.50%, 78.79%, and 83.77% at Vpsoi = 2, 6, and 10 V, respectively, compared to the zero back-gate bias case.

Table 3 presents the impact of various back-gate bias combinations on the SEU cross-section for LET = 87.3 MeV·cm^2/mg. The results demonstrate that apply-

ing negative Vnsoi and positive Vpsoi effectively mitigates the SEU cross-section. Notably, when the sum of absolute values of back-gate bias applied to N-type and P-type transistors was equal, a larger ratio of |Vnsoi|/|Vpsoi| resulted in lower SRAM sensitivity to SEU. Moreover, under identical magnitudes of back-gate bias, the negative bias applied to the NSOI electrode of N-type transistors exhibited superior effectiveness against SEU compared to the positive bias applied to the PSOI electrode of P-type transistors.

Figure 2 Figure 2: see original paper shows the relationship between SEU cross-section and supply voltage at LET = 86.1 MeV · cm^2/mg. At the nominal circuit voltage of 1.8 V, 61 single-bit upsets were recorded, whereas only one single-bit upset occurred at VDD = 1.62 V, and 158 single-bit upsets were observed at VDD = 1.98 V. A 10% increase in supply voltage resulted in a significant 161.67% increase in SEU cross-section. This observation suggests that variation in drain depletion region thickness with changing VDD contributed to the escalation of SEU cross-section. Further detailed analysis of this mechanism is provided in Section IV.

Figure 2(b) depicts the relationship between SEU cross-section and supply voltage at LET = 87.3 MeV · cm^2/mg. Compared to the SEU cross-section of 3.3×10^{-10} cm^2/bit at nominal voltage, the SEU cross-section decreased by 95.40% and 96.30% for pull-down VDD of 10% and 20%, respectively, and increased by 125.93% and 165.74% for pull-up VDD of 10% and 20%, respectively.

When VDD was below 1.62 V, the resulting drain voltage did not enable the CSOI to establish an effective drain depletion region capable of efficiently collecting charge excited by heavy ions. Consequently, the SEU cross-section exhibited minimal variation with supply voltage and remained significantly lower than that observed at nominal voltage. For VDD exceeding 1.71 V, the SEU cross-section experienced rapid escalation with increasing supply voltage, reaching a plateau after a 10% pull-up. We posit that the supply voltage range from 5% pull-down to 10% pull-up constitutes the interval in which space-charge region width undergoes significant variation in response to voltage changes. Within this range, any alteration in supply voltage substantially affects the device' s capability to collect unbalanced carriers. However, when VDD surpassed 1.98 V, the width of the space-charge region ceased to vary significantly, attributed to the power-function relationship governing space-charge region width with reverse bias voltage.

IV. SEU Simulation and Discussion

A. TCAD Physical Model Setting

To achieve comprehensive understanding of the mechanisms driving the observed experimental phenomena, we employed TCAD semiconductor device simulation software to develop a CSOI model. After parameter calibration, we utilized SDEVICE to construct a 6T-SRAM for the CSOI process. This section investigates the relationship between SEEs and parameters such as heavy-ion incidence posi-

tion, back-gate voltage, and supply voltage to elucidate the phenomena detailed in Section III.

Figure 3 [Figure 3: see original paper] depicts the CSOI device model developed for this simulation. The SRAM core memory cell comprised two pairs of input and output cross-coupled inverters (N1, P1; N2, P2). In the stable storage state, the word line was maintained at a low level, causing transmission transistors N3 and N4 to be in the off state. Consequently, the n0 node stored data "1," while the n1 node stored data "0." Heavy-ion incidence was modeled by incorporating lateral diffusion via a Gaussian distribution with a trajectory radius of 0.015 μm. Given the significant carrier generation due to SEEs, mechanisms including Fermi–Dirac statistics [30] as well as Shockley–Read–Hall (SRH) and Auger recombinations [31] (indirect and Russo–Cherese composites) were incorporated into the simulation.

Carrier transport was resolved through application of a hydrodynamic model, which entails concurrent coupling of electron and hole temperature equations. The Philips unified model (PhuMob) was employed to consider the collective influence of phonon scattering, inter-carrier scattering, and ionizing impurity scattering on mobility [32]. The Enormal model incorporates the impact of electric field perpendicular to the interface on mobility. The high-field velocity saturation mobility model (HighFieldSaturation model) integrates the correlation between mobility and electric field force along with saturation velocity [33]. Moreover, a resistive contact model was implemented at source and drain terminals. By introducing a distributed resistor (DistResist) between the contact and silicon surface of the device body, external voltage induced a voltage drop across the resistive contact, thereby enhancing device model realism.

B. Susceptibility of SEUs to Heavy-Ion Incidence Position

Simulation results indicated that the off-state transistor exhibited the highest sensitivity to SEUs, as shown in Fig. 4 [Figure 4: see original paper]. In this state, electrons generated by heavy ions within the off-state NMOS channel swiftly migrated toward the drain due to the carrier-collecting effect and bipolar amplification facilitated by drain PN junctions, resulting in maximum peak SET current magnitude. Conversely, in the transmission state, source and drain terminals were biased, preventing establishment of a potential difference for carrier drift. Consequently, only minimal carriers migrated to source and drain terminals concurrently through diffusion motion, yielding significantly reduced SET current compared to the off state. In the open state, the electric potential difference between source and drain was zero, impeding efficient collection of electron-hole pairs generated in the channel. Hence, the on-state NMOS transistor exhibited the lowest SEU sensitivity.

Figure 5 Figure 5: see original paper depicts charge collected at the drain when heavy ions impinged vertically on off-state NMOS and PMOS transistors of the SRAM at various positions. The findings indicated that the SRAM sensitive re-

gion was located at the drain–gate PN (D-G) junction of the off-state transistor. Given the similarity in physical mechanisms triggering SEEs for both off-state transistor types, this study exclusively analyzed the NMOS transistor.

As depicted in Fig. 5(b), compared to other regions within the body area, the depletion region of the D-G junction in the off-state MOS exhibited the highest electric field strength. Consequently, the device achieved maximum efficiency in collecting carriers generated by heavy ions incident on the D-G junction, resulting in current pulses with the shortest peaking time and maximum charge accumulation. Conversely, when the incident position lay within the source region, carrier drift motion was required to overcome potential barriers of both source–gate (S-G) and D-G junctions for collection by the drain electrode. Consequently, the source electrode exhibited the lowest SEE sensitivity, with only a fraction of carriers generated by heavy-ion ionization undergoing drift motion while the majority contributed to a diffusion current driven by concentration gradients, characterized by SET pulse current featuring a small peak but significant tail current.

Owing to higher electron mobility compared to holes, electrons are more readily collected by the drain, resulting in pulse current generation. Consequently, the SEE sensitivity of NMOS, in which electrons constitute majority carriers in the source–drain, surpasses that of PMOS. This discrepancy is evident in Fig. 5(a), where the peak charge collected by NMOS exceeded that collected by PMOS.

Furthermore, as depicted in Fig. 6 Figure 6: see original paper, to elucidate the mechanism of heavy-ion impact at the transistor level and subsequently analyze the effect of back-gate voltage on SEU cross-section, we simulated the electrostatic potential of devices at three distinct moments: before (T1), during (T2), and after (T3) heavy-ion incidence. Figure 6(b) shows that heavy ions with sufficient LET striking the sensitive region of an NMOS transistor generated significant carriers within the device. Electrons were predominantly collected by the drain, reducing drain potential, while hole accumulation after electron excitation increased body potential. This reduction in potential barrier between body and source–drain induced zero or even positive bias in the base-emitter junction of the parasitic bipolar transistor, thereby instigating bipolar amplification that augmented pulse current.

C. Relationship between SEU Occurrence and Back-Gate Bias

Figure 7 Figure 7: see original paper and (b) illustrate variations in cross-sectional potential distributions with back-gate bias for NMOS and PMOS transistors after heavy-ion incidence, respectively. As |Vnsoi| and |Vpsoi| increased, drain barrier height increased, making it more challenging for electrons to traverse the D-G barrier and reach the drain. Consequently, fewer carriers were collected at the drain of the off-state MOS, attenuating the parasitic bipolar amplification effect and decreasing SEE sensitivity. This augmented the SRAM self-recovery capability and elevated the LET threshold.

Figure 8 shows the relationship between collected charge and back-gate bias. As |Vsoi| increased from 0 to 10 V, NMOS collected charge decreased by 2.22% while experimental SEU count decreased by 94.24%. PMOS collected charge decreased by 0.43% while experimental SEU count decreased by 83.78%. This observation supports the experimental finding that SEU inhibition was more pronounced with Vnsoi than with Vpsoi.

Additionally, when analyzing experimental data, we observed that the device exhibited the most significant charge reduction when the absolute value of |Vsoi| increased from 0 to 2 V. The slopes of the curves in Fig. 8(a) and (b) are 5.24×10^{-11} cm^2/bit$\cdot$V and 4.48×10^{-11} cm^2/bit$\cdot$V, respectively—the highest among all ranges. This suggests that this voltage level offered the highest rejection efficiency for SEU occurrences. Considering both circuit power and SEU cross-section, the back-gate bias combination of Vnsoi = -2 V and Vpsoi = 2 V was deemed most suitable.

D. Impact of Supply Voltage on SEUs

Since semiconductor power consumption is directly proportional to the square of supply voltage, a viable strategy for minimizing power involves lowering VDD. However, SRAM susceptibility to SEUs is influenced by supply voltage. Consequently, comprehensive examination of SEU sensitivity across various supply voltage levels is essential. The SRAM soft error rate is described by the following model [34]:

$$SER \propto F \times A \times \exp\left(-\frac{Q_{crit}}{Q_{Coll}}\right)$$

where F is particle fluence in particles/(cm$^2 \cdot$ s), A is the area of the sensitive region in cm^2, and Q_{crit} and Q_{Coll} are the critical and collected charges in fC, respectively [35–37].

According to the formula $Q_{crit} \approx C_n V_{DD}$ referenced in [38], critical charge depends on specific circuit and device attributes, primarily influenced by node capacitance and supply voltage. The minimum charge necessary for SEUs increases with higher supply voltages, reducing transistor-sensitive volume due to augmented critical charge. This phenomenon, where increased supply voltage decreases SEU cross-section by elevating critical charge, is denoted as Mechanism I in this paper.

In contrast, collected charge (Q_{Coll}) is a strong function of particle LET value and supply voltage, characterizing the number of carriers collected at the drain during heavy-ion incidence [39]. For MOSFET devices, depletion-region thickness can be calculated using:

$$W = \sqrt{\frac{2K_s\varepsilon_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} + V_A)}$$

where K_s denotes semiconductor dielectric constant, ε_0 denotes vacuum dielectric constant, q denotes electronic charge, N_A and N_D denote acceptor and donor doping concentrations, respectively, and V_{bi} and V_A denote semiconductor built-in and applied voltages at the drain junction, respectively. V_{bi} is calculated as:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Depletion region thickness is directly proportional to supply voltage, implying that as VDD increases, both electric field density within the transistor and depletion volume increase. Consequently, charge collected by nodes increases. Figure 9 [Figure 9: see original paper] presents current density in the NMOS drain region at various bias voltages. Supply voltage plays a significant role in shaping PN junction depletion layer characteristics. Specifically, higher voltage bias in the off-state NMOS drain produces a more pronounced electric field within the depletion region, enhancing the drain' s ability to collect drifting carriers. Peak node pulse current is primarily determined by carrier drift; therefore, increased supply voltage intensifies drift motion, resulting in higher peak pulse current.

In the low core voltage state, the limited number of holes generated in the body region by low-LET heavy ions fails to effectively diminish the source-body potential barrier. Consequently, these holes cannot traverse the depletion region between source and body and are released through ground. Hole accumulation in the body region elevates electric potential, prompting significant electron flow to be collected by the drain through the depletion region between drain and body. Conversely, high-LET heavy ions generate substantial carriers that significantly reduce potential barriers between source and body. Thus, most holes generated in the body region by these heavy ions cross the depletion region between source and body and release to ground, lowering body region electric potential, suppressing bipolar amplification, and resulting in partial electron collection by the drain. Therefore, in the low-voltage state, current density produced by high-LET heavy ions is lower than that produced by low-LET heavy ions.

In the high core voltage state, the drain depletion region extends sufficiently to collect almost all electrons generated by low-LET heavy ions, causing current density from these ions to saturate after core voltage increases to 1.0 V. As core voltage increases further, drain-body depletion region width expands, enhancing drain electron collection efficiency. Simultaneously, elevated drain voltage increased body region electric potential, thereby strengthening the bipolar amplification effect. Consequently, current density from high-LET heavy ions increases rapidly with core voltage. In the high-voltage state, current density from high-LET heavy ions surpasses that from low-LET heavy ions.

The physical process of drain-junction depletion region widening due to increased supply voltage, as discussed in [40], results in SEU cross-section enlargement. This phenomenon is referred to as Mechanism II in this paper.

Figure 10 [Figure 10: see original paper] shows that for low-LET heavy-ion incidence, both Q_{crit} and Q_{Coll} increased with supply voltage. However, the number of carriers generated by heavy ions of a specific LET value remained constant and unaffected by VDD variations. The depletion region expanded sufficiently to capture excited carriers when supply voltage exceeded 1 V. Therefore, when VDD increase allowed the drain-depletion region to gather the majority of carriers, the magnitude of change in Q_{crit} and Q_{Coll} with respect to VDD resulted in notable disparity, evidenced by the increase in Q_{crit} surpassing that in Q_{Coll}. During this phase, Mechanism I prevailed, resulting in decreased SEU cross-section with increasing supply voltage.

However, for high-LET heavy-ion incidence, as shown in Fig. 10, the capacity to deposit greater energy in the device sensitive region meant that excited carriers were not entirely collected by the depletion layer even at VDD = 1.98 V. Collected charge increased rapidly with VDD. At this juncture, Mechanism II dominated.

During competition between these two mechanisms, the notable increase in CSOI SRAM SEU cross-section under Ta-ion irradiation with increasing supply voltage can be attributed to increased depletion layer thickness and parasitic bipolar current induced by rising VDD. Although Mechanism II prevailed in this 0.18 μm node test and simulation, the conflicting influences of Mechanisms I and II in small-node technology and low-core voltage scenarios merit further comprehensive investigation.

V. Conclusion

Experimental results demonstrated that both negative N-type and positive P-type transistor back-gate biases can effectively enhance SRAM memory cell SEU resistance. Moreover, we observed that the impact of Vnsoi is superior to that of Vpsoi when subjected to the same bias voltage magnitude. Maintaining the absolute value of |Vsoi| between 2 V and 6 V not only ensures low circuit power consumption but also aids in suppressing SEU occurrences.

Through TCAD simulations, this study investigated the sensitive location of CSOI SRAM and explored the influence of back-gate bias and supply voltage on SRAM SEE sensitivity. For a specific range and LET value of heavy-ion incidence, we observed that the drain-body potential difference of the NMOS device increased with back-gate bias. This increase raises the barrier height between body and source–drain, consequently suppressing parasitic bipolar amplification and reducing CSOI SRAM SEU cross-section.

In the context of SRAM, we observed that two competing mechanisms exist for SEU occurrence. First, increased supply voltage escalates critical charge and reduces circuit-sensitive volume. Second, increased supply voltage widens the depletion region, augmenting device collected charge and sensitive volume. In most cases, these mechanisms coexist and compete, potentially yielding varying competitive outcomes. Specific process nodes and LET values play crucial roles

in determining the nature of this competition. Thoroughly evaluating SEU cross-section at various LET values and core voltages and conducting bias experiments to determine worst-case scenarios for SRAM performance during ground testing are essential. Neglecting these factors may result in underestimation of circuit SEU cross-section.

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Note: Figure translations are in progress. See original paper for figures.