An 8-Channel, 46-ps-Precision TDC ASIC with Improved Vernier Delay Loop for STCF EMC

Authors: Mr. Ziwei Zhao, Zheng, Dr. Ran, Liu, Dr. Chao, Prof. Jia Wang, Wei, Dr. Xiaomin, Dr. Feifei Xue, Dr. Ruiguang Zhao, Hu, Dr. Yongcai, Zheng, Dr. Ran

Date: 2025-03-03T00:00:00+00:00

Abstract

An 8-channel Time-to-Digital Converter (TDC) with high precision and high linearity for the electromagnetic calorimeter (EMC) in the super tau-charm facility (STCF) is presented. The 3-level quantization structure is employed in the proposed TDC to achieve high time resolution and wide dynamic range simultaneously. A double triggered counter characterized with metastability eliminating is used as the first level. The second and third level are implemented with a polyphase clock sampler and a modified Vernier Delay Loop (VDL) with automatic reset mechanism, respectively. Two low-jitter Delay Locked Loops (DLLs) with different length are utilized to assist in vernier measurement and the polyphase clocks are also provided by the longer DLL. Theoretical analysis with respect to the optimal combination of DLL length and reference clock frequency has been presented. The proposed 8-channel TDC is implemented using 180-nm standard CMOS process with 1.8-V power supply. Under the reference clock frequency of 100-MHz, the TDC is realized with a resolution of 41.7-ps and a dynamic range of 2560-ns. According to testing results, the best single-shoot precision is 46-ps and good consistency among all channels can be observed. The effect of sliding scaled technique on improving conversion linearity is also proved with experiment results. In asynchronous measurements, the maximum differential nonlinearity (DNL) and the integral nonlinearity (INL) are less than 0.4-LSB and 0.5-LSB respectively.

Full Text

Preamble

An 8-Channel, 46-ps-Precision TDC ASIC with Improved Vernier Delay Loop for STCF EMC

Zi-Wei Zhao[1], Ran Zheng[1],[2],†, Chao Liu[1], Jia Wang[1], Xiao-Min Wei[1], Fei-Fei Xue[1], Rui-Guang Zhao[1], and Yann Hu[1]
[1]School of Computer Science and Technology, Northwestern Polytechnical University, No. 1, Dongxiang Road, Chang' an District, Xi' an, 710029 Shaanxi, China
[2]Research & Development Institute of Northwestern Polytechnical University in Shenzhen, No. 45, Gaoxin South 9th Road, Nanshan District, Shenzhen, 518063 Guangdong, China

This paper presents an 8-channel Time-to-Digital Converter (TDC) featuring high precision and high linearity for the electromagnetic calorimeter (EMC) of the super tau-charm facility (STCF). The proposed TDC employs a 3-level quantization structure to simultaneously achieve high time resolution and wide dynamic range. The first level utilizes a double-edge-triggered counter with metastability elimination, while the second and third levels are implemented using a polyphase clock sampler and a modified Vernier Delay Loop (VDL) with automatic reset mechanism, respectively. Two low-jitter Delay Locked Loops (DLLs) with different lengths assist in vernier measurement, with the polyphase clocks provided by one of the DLLs.

Theoretical analysis regarding the optimal combination of DLL length and reference clock frequency is presented. The proposed 8-channel TDC is fabricated using a 180-nm standard CMOS process with 1.8-V power supply. Under a 100-MHz reference clock frequency, the TDC achieves a resolution of 41.7 ps and a dynamic range of 2560 ns. Testing results demonstrate a best single-shot precision of 46 ps with good consistency across all channels. Experimental results also verify the effectiveness of the sliding scale technique in improving conversion linearity. In asynchronous measurements, the maximum differential nonlinearity (DNL) and integral nonlinearity (INL) are less than 0.4 LSB and 0.5 LSB, respectively.

Keywords: STCF, TDC, Vernier, sliding scale technique, high linearity

Introduction

As a key component of time measurement electronics, Time-to-Digital Converter (TDC) has become a research hotspot in nuclear detection [**?**, **?**] and medical imaging [**?**]. The super tau-charm facility (STCF), currently under construction in China, is a new accelerator-based experimental facility with ultra-high luminosity for particle physics [**?**]. The STCF facility is equipped with multiple detectors, including the electromagnetic calorimeter (EMC) which measures photon and electron energy with high efficiency and resolution. Additionally, good time resolution is required for the STCF EMC for background suppression, gamma-neutron discrimination, and event identification [**?**].

The STCF EMC adopts pure CsI (pCsI) crystal scintillators with avalanche photodiode (APD) readout, where time stamps are acquired through a front-end readout circuit (ROC) with leading edge discrimination (LED) and digitized by

TDC [?]. The full response time resolution is expected to be better than 300 ps for 1 GeV energy deposits, including optical processes and APD/electronics response [?]. However, the pCsI decay time used in this experiment can be as large as 30 ns [?], and the large capacitance (270 pF) of the adopted APD detector (Hamamatsu S8664-1010) introduces significant input noise to the front-end circuit [?]. Both factors make achieving ultra-high time precision in the ROC challenging; for example, our team has implemented an APD ROC with 270-ps time precision [?]. To achieve the target electronics time resolution of 300 ps, the TDC is expected to reach 100-ps resolution. Due to the large number of readout channels (6732 for the barrel and 1938 for the end-cap [?]), the ROC and TDC have been monolithically integrated on an ASIC for high operational efficiency. This paper investigates a TDC ASIC suitable for multi-channel integration, with resolution of 100 ps or better and high linearity.

Numerous time-to-digital conversion algorithms and architectures have been proposed over recent decades. ASIC-based TDCs can be divided into three categories [?]: sampling TDC, noise-shaping TDC, and stochastic TDC. Due to requirements for real-time measurement and high counting rate in STCF ECAL, noise-shaping TDCs requiring multiple samples for high resolution are not applicable. Stochastic TDCs are also unsuitable due to their large die area [?]. Counter-based TDC is the simplest sampling TDC structure with scalable dynamic range, but requires a high-frequency oscillator for high resolution (e.g., an 8-phase 3.125-GHz oscillator was used to achieve 40-ps resolution in [?]). The tapped delay line is a popular and easily implemented TDC whose resolution is typically limited by transistor channel length. The unit delay can be relatively fixed using delay locked loop (DLL) [?] or phase locked loop (PLL) [?] to overcome process, voltage, and temperature (PVT) variations. The front-end circuit is implemented in 180-nm CMOS process with 3.3-V power supply for better dynamic range and noise performance. Consequently, when manufactured with the same process, achieving controlled gate propagation delay below 100 ps is difficult, making sole use of counter or delay line insufficient for our design goals. Pulse shrinking [?] and time amplifying [?] are sampling TDC structures with sub-gate-delay resolution, both operating using propagation delay differences between leading and trailing edges of input pulses. However, unavoidable mismatch in delay cells typically leads to poor consistency across multiple channels. Successive-approximation TDC [?] is an alternative for high-resolution TDC, but suffers from long conversion time as a primary drawback.

Considering its high resolution, high counting rate, and superior multi-channel consistency, the vernier TDC [?] appears more suitable for real-time measurements. Compared with vernier delay line TDC, cyclic vernier TDC offers advantages in area occupation and conversion linearity while lagging in conversion speed [?]. Nonetheless, cyclic vernier TDC can still achieve relatively high speed (e.g., 6.67-MS/s conversion rate in [?]).

To simultaneously achieve high resolution (100 ps) and large dynamic range (2 µs), the Nutt method [?] was proposed using a counter and two fine time-

interpolators. The counter measures the number of clock cycles between Start and Stop, while start and stop interpolators measure the interval between Start/Stop signals and their subsequent first clock rising edge, respectively. The measured interval between start and stop signals can be expressed as:

$$T_{IN} = T_{REF} + T_{S1} - T_{S2}$$

where T_{REF}, T_{S1}, and T_{S2} denote the measurement results of the counter, start interpolator, and stop interpolator, respectively. Finer resolution can be achieved when start and stop interpolators are further divided into more measurement levels. Another merit of Nutt-method-based TDC is its natural implementation of the sliding scale technique [**?**], which can greatly improve TDC measurement linearity.

To meet STCF EMC requirements, this paper proposes an 8-channel, Nutt-method-based, 3-level TDC. The first level uses a coarse counter, the second level based on polyphase clock sampler measures the time residue of the first level, and the time margin of the second level is quantized by a modified Vernier Delay Loop (VDL) serving as the finest level. The polyphase clocks used in the second level are provided by a low-jitter DLL which, together with another shorter DLL, serves vernier measurements in the finest level.

The remainder of this paper is organized as follows. Section II introduces the overall framework and principles of the proposed TDC and provides analysis of key parameters. Section III describes the circuit design of the DLL and 3-level TDC. Section IV presents experimental setups and measurement results. Section V summarizes and concludes this work.

II. Framework and Analysis

A. The Framework and Principles of the Proposed TDC

Fig. 1 [Figure 1: see original paper] shows the overall framework of the proposed TDC and the structure of one channel. The PLL, DLLs, and coarse counter are global for the chip, and 8 TDC channels with identical structure can operate independently. In actual applications with ROC, one TDC channel samples the external start signal while another channel measures the trigger signal generated by ROC (the stop signal). The time interval between start and stop is calculated and stored off-chip as the time stamp.

The chip reference clock, named Clk, can be provided by an integrated PLL or directly from an off-chip clock source. As shown in Fig. 1, DLL-1 and DLL-2 using Clk as input are composed of delay lines with n and $n-1$ delay cells, respectively. The counter as the first TDC level can be triggered by both rising and falling edges of Clk, with results delivered continuously to each TDC channel. The second TDC level uses multi-phase clocks produced by DLL-1, which are fed to the clock sampler in each channel. The residual time of the second

level (the interval between the hit event and its subsequent polyphase clock rising edge) is measured by the third TDC level—a vernier delay loop. Vernier measurement utilizes the slightly different delay times between two delay cells, τ_1 and τ_2, controlled by DLL-1 and DLL-2, respectively. The TDC resolution is determined by the third level and expressed in (2):

$$Re = \tau_2 - \tau_1 = \frac{(n-1)f_0}{n(n-1)f_0}$$

where f_0 denotes the Clk frequency. The TDC dynamic range is proportional to the number of counter bits, which can be increased according to power consumption and die area limits [**?**]. The dynamic range can be expressed by (3), where N_1 denotes counter bits.

B. Tradeoffs Among Key Parameters

From formula (2), we see that n and f_0 values should be increased for finer resolution, meaning more delay cells in DLLs or higher reference clock frequency. TDC precision depends mainly on quantizing noise and random noise. The former depends on resolution value, which can be expressed in time domain as follows [**?**].

Jitters from the reference clock, hit signals, and DLLs also degrade precision, contributing to random noise in the phase domain. Assuming clean clock and hit signals, jitter primarily arises from DLLs. Fig. 2 Figure 2: see original paper shows how DLL jitter affects TDC precision. Assuming the hit signal lies between Clk$\langle n-1\rangle$ and Clk$\langle n\rangle$ provided by DLL-1, a replica of Clk$\langle n\rangle$ is delivered to the VDL for finest quantization. Jitter generated by a single delay cell can be indicated as σ_0, due to noise from control voltage, power supply, and substrate. The jitter of Clk$\langle n\rangle$ is $n\sigma_0$, which is also the maximum accumulated jitter of DLL-1. As shown in Fig. 2(b), cycling occurs m times on loops corresponding to Hit and Clk$\langle n\rangle$, with OUT_A and OUT_B as VDL output signals. Assuming uncorrelated jitters from the 4 cascaded delay cells in VDL, accumulated jitters on OUT_A and OUT_B are represented by (5) and (6), respectively:

$$\sigma_{r1} = \sigma_{r2} = n + 4m\sigma_0$$

At cycling end, OUT_A and OUT_B are fed to an arbiter for phase comparison. Time uncertainty due to jitter can be regarded as accumulation of σ_{r1} and σ_{r2} and expressed by:

$$\sigma_{total} = \sqrt{\sigma_{r1}^2 + \sigma_{r2}^2} = \sqrt{2}(n+4m)\sigma_0$$

The value of m can be deduced from the relation between τ_1 and Re:

$$m = \frac{\tau_2}{Re} = \frac{n-1}{Re \cdot f_0}$$

Total time uncertainty, or TDC time precision, is represented by:

$$\sigma_{TDC} = \sqrt{\sigma_q^2 + \sigma_{jitter}^2}$$

where σ_q is quantizing noise and σ_{jitter} is random jitter.

We designed the delay cell with symmetrical current-starved structure [**?**] as shown in Fig. 2(c), characterized by almost equal rise and fall times. To prevent phase reversal, a delay cell comprises two current-starved inverters whose propagation delay is controlled by DLL output voltage (V_{C1} or V_{C2}). Defining the toggle point for both edges as $V_{DD}/2$, the unit propagation delay in DLL-1 can be expressed by:

$$\tau_1 = \frac{V_{DD} C_L}{I_{CS}}$$

where C_L denotes parasitic capacitance on each stage' s output node and I_{CS} denotes the mean charging/discharging current through C_L during output level switching. According to [**?**], delay cell phase noise is dominated by white noise, and low-frequency noise can be neglected when rise and fall edges are symmetric. Fig. 2(d) shows the delay cell noise model for a positive input step (PMOS noise contribution omitted). For simplicity, bias transistors (NM2, resistors) have negligible voltage drop, and the input transistor (NM1 in Fig. 2(d)) is assumed saturated. The spectral density of output noise [**?**] can be described by:

$$S_{in,N} = \frac{8kT\gamma I_{CS}}{V_{DD} - V_{tN}}$$

where V_{tN} is NMOS threshold voltage and R_D denotes the equivalent resistance of NM2 in Fig. 2(c). As R_D is constant when NM2 bias is fixed, we adopted the phase noise model for inverters from [**?**] to obtain delay spectral density:

$$S_{td} = \mathrm{sinc}^2(f t_d) S_{in,N}$$

The mean square value of t_d can be derived using the Wiener–Khinchine theorem [**?**]:

$$\sigma_{td}^2 = \int_{-\infty}^{\infty} S_{td} df = \int_{-\infty}^{\infty} \mathrm{sinc}^2(x) dx \cdot \frac{8kT\gamma I_{CS}}{V_{DD} - V_{tN}}$$

With appropriate simplifications, the jitter of this delay cell with positive input is:

$$\sigma_0^2 = 2\sigma_{td}^2 = \frac{8kT\gamma V_{DD}C_L}{(V_{DD} - V_{tN})(I_{CS})^2}$$

All terms except n and f_0 in this formula can be considered constants. f_0 is constrained to (50 MHz, 100 MHz) due to power consumption. For simplification, TDC resolution is fixed (e.g., 45 ps). The quantizing noise σ_q is thus fixed, leaving only the random jitter component to minimize, derived from equations (2), (7), (8), (15), and (16):

$$\sigma_{jitter} = \sqrt{\frac{(9n-8)kT \cdot 2\gamma V_{DD}C_L}{(V_{DD} - V_{tN})(V_{DD}C_L)^2((n-1)Re)^{-2}}}$$

Equation (17) shows that minimizing random jitter requires smaller n values. With Re fixed at 45 ps, we determined $f_0 = 100$ MHz and $n = 16$, yielding an ideal TDC resolution of approximately 41.7 ps.

III. Design of Circuit

A. Delay Locked Loop

The two DLLs integrated in the TDC have nearly identical structures, as shown in Fig. 3 Figure 3: see original paper, except for voltage-controlled delay lines (VCDLs) containing different numbers of delay cells. Based on the above analysis, VCDLs in DLL-1 and DLL-2 contain 16 and 15 cells, respectively. The 100-MHz reference clock is fed to DLL-1 and DLL-2, which operate independently without requiring synchronization.

The lock controller [**?**] prevents false locking and harmonic locking by comparing the first phase with several intermediate phases. When enabled, the lock controller forces VCDL delay to range within 8–13.33 ns, reducing DLL lock time. The phase detector operates with the first and last phases, determining charge pump charging/discharging status. Complementary switches, dummy transistors, and wide-swing cascaded current mirrors are adopted in the charge pump to improve charging/discharging matching, enabling much smaller locked phase error. Additionally, a start-up circuit provides proper initial values to V_{C1} and V_{C2}.

The VCDL consists of 15/16 cascaded delay cells and 2 dummy cells, all based on the modified current-starved structure. As shown in Fig. 3(b), variable PMOS resistances (PM2, PM5) and variable NMOS resistances (NM2, NM5) are controlled by V_{BP} and V_{C1}, respectively, varying in opposite directions. With appropriate transistor dimensions, approximately equal rise and fall times are achieved across the tuning range. However, the biasing transistor NM0 can

contribute considerable noise, so only one bias circuit is used per DLL, with control voltages V_{C1} and V_{BP} shared by all delay cells in both VCDL and TDC channels. Constant MOS resistances (PM3, PM6, NM3, and NM6) supply basic operating current and ensure the delay cell functions when V_{C1} is below NMOS threshold voltage, preventing DLL inactivity.

Fig. 3(c) shows simulated delay-voltage characteristics under different PVT conditions. The effective tuning range is 390–850 ps, covering expected unit delays for both DLLs (625 ps for DLL-1 and 666.7 ps for DLL-2). As control voltages are distributed to multiple channels at varying distances from DLLs, control voltage shifts occur at each channel. As shown in Fig. 3(d), assuming shifts ΔV in both V_{C1} from DLL-1 and V_{C2} from DLL-2, the high linearity of delay-voltage characteristics within small voltage ranges means both unit delays are skewed by Δt. Therefore, all channel resolutions remain roughly consistent as they are dominated by the difference between these two unit delays.

B. The First and Second Level

The first TDC level uses an 8-bit global counter with double-edge-triggered structure [**?**] shown in Fig. 4 Figure 4: see original paper. Counting results $CntP$ and $CntN$, obtained with rising and falling edges of Clk respectively, are delivered simultaneously to each channel. The channel data selector captures the proper counting result when the asynchronous Hit signal arrives, based on the second-level result $L2[3:0]$ as shown in Fig. 4(b). If the asynchronous input signal Hit lies in the first half of the clock cycle, $L2[3] = 1$ and $CntN$ is selected as the first-level result. If Hit lies in the second half, $CntP$ is selected. The double-edge-triggered counter implementation and appropriate settings aim to eliminate counter metastability.

The second level measures the time interval between Hit and the first rising Clk edge following Hit, realized with a polyphase clock sampler composed of 16 arbiters as shown in Fig. 4(b). Another task is transferring residual time to the next level via the synchronizer. For example, if Clk$\langle 1 \rangle$ is captured by the sampler, the residual time is the interval between Hit and Clk$\langle 1 \rangle$. Although well-matched loads are inserted on both synchronizer signal paths, errors remain between input and output intervals. Monte Carlo simulation shows maximum error of approximately 5.1 ps, which is tolerable as the final resolution is much larger.

C. The Third Level–Vernier Delay Loop

The Vernier Delay Loop (VDL) quantizing the second-level residual time is a modified version of that proposed in [**?**], as shown in Fig. 4(c). The VDL contains two structurally identical loops: the slow loop with input $SI1$ and the fast loop with input $SI2$. $SI1$ and $SI2$ are the two synchronizer outputs shown in Fig. 4(b). $SI1$ precedes $SI2$ with interval T_f varying within 0–625 ps. The edge detect circuit generates a narrow pulse when the $SI1/SI2$ rising edge

arrives. Each loop contains two unit-delay types, τ_1 and τ_2, regulated by control voltages from DLL-1 and DLL-2, respectively. A single delay cell and arbiter convert the narrow pulse to a τ_2-width pulse. Cycle periods are determined by 3-cascaded delay cells (neglecting other logic delays): $3\tau_2$ for the slow loop and $\tau_1 + 2\tau_2$ for the fast loop. Signals at nodes A1 and A2 are denoted $SA1$ and $SA2$, respectively. $SA1$ precedes $SA2$ by T_f before cycling, and the $SA1$-$SA2$ interval decreases by $(\tau_2 - 2\tau_1)$ after each cycle. Cycling stops when $SA2$ catches $SA1$. The cycle count required for alignment is obtained by the pulse counter and expressed by:

$$n_f = \left\lceil \frac{T_f}{\tau_2 - \tau_1} \right\rceil$$

Ideally, maximum n_f is 15, requiring only a 4-bit counter, but a redundant bit is added for calibration.

As the VDL must measure arrival times of sequential pulses, an auxiliary circuit enables automatic VDL reset after quantization, shown in the dotted box of Fig. 4(c). Nodes B, C, D, and E signals are denoted SB, SC, SD, and SE, respectively. The timing diagram of critical signals is shown in Fig. 4(d). Before quantization, global $Rstn$ first pulls SB to 0 to clear all loop nodes, then SB is pulled up to 1 to ready the loop for cycling. The VDL cycling stage begins when $SI1/SI2$ arrives. After $SA1$ and $SA2$ align following several cycles, the flip-flop samples to 1, then SB is pulled to 0 and both loops are cleared. Synchronized with SB, SD and SE are successively pulled down to 0 with $2\tau_2$ delay. The flip-flop is then cleared and SB, SD, SE are pulled up to 1 in turn. After these steps, the VDL is again ready for the next quantization. With this automatic reset mechanism, VDL maximum dead time is less than 45 ns, enabling single-channel conversion rates up to 22.2 MS/s. Considering integration and serial readout of 8 channels, the overall TDC chip conversion rate reaches 5 MS/s. Combined with a fast ROC, pileup effects in STCF EMC can be mitigated given the 1-MHz background counting rate [**?**].

IV. ASIC Prototype and Performance

A. ASIC Prototype and Experiment Setups

The proposed 8-channel TDC was taped out using standard 180-nm CMOS process with 1.8-V power supply, with chip microphotograph shown in Fig. 5 Figure 5: see original paper. The TDC channel layout uses a strip shape with 8 channels arranged in a column, minimizing V_{C1} and V_{C2} distribution path lengths. The chip die area is 1.55 mm × 1.42 mm including the pad ring.

Fig. 5(b) shows the experiment setup comprising an oscilloscope for signal observation, spectrum analyzer for jitter measurement, two pulse generators for reference clock and TDC input signals, an FPGA board and host computer for chip control, and a logic analyzer for data collection and processing. An AD9552

clock generator chip provides the 100-MHz reference clock with jitter below 1 ps (rms). For linearity evaluation, the reference clock is provided directly by the pulse generator.

B. Performance of DLL

Three chips were tested and verified: chip-1, chip-2, and chip-3. Unless specified otherwise, all following measurements use chip-2. Two approaches measured DLL jitter: obtaining the phase noise curve of the last polyphase clock and integrating within 10 kHz–20 MHz frequency offset range, and direct jitter measurement with the oscilloscope. Both approaches yield 5 ps (rms) jitter, much less than TDC resolution. Other performances are shown in Table 1 .

Variable "margins" between the second and third levels result from non-ideal factors. To explain, assume two second-level step sizes of 600 ps and 650 ps, which are also intervals measured by VDL. Neglecting VDL non-ideal factors, resolution is fixed at 41.7 ps. Then VDL last-bin sizes for 600-ps and 650-ps input intervals are 16.2 ps and 24.5 ps, respectively.

To prevent the last VDL quantization bin from becoming too narrow and worsening DNL, a bin-size filtration mechanism is implemented. First, the approximate LSB magnitude is ascertained. If the last bin size is less than LSB/4, the last bin is combined with the second-to-last bin; otherwise, the last bin is retained. Channel-1 bin distribution within one clock period is shown in Fig. 6 Figure 6: see original paper. After this processing, LSBs of eight channels are shown in Fig. 6(d), providing approximate measured results across 3 chips. Channel-1 LSB is larger than other channels, explained by significant supply voltage deviation in this channel.

C. Performance of TDC

First, each TDC channel' s actual resolution (LSB) must be determined. As bin distributions are nearly consistent across all clock periods [**?**], actual LSB evaluation within one clock period suffices. One pulse generator channel provides the 100-MHz reference clock, while TDC input at 4.00001 MHz is derived from another channel. This makes the interval between TDC input and reference clock rising edge increase by 0.625 ps each clock cycle, cyclically repeating within 0–10 ns range—an approximate code density test method [**?**].

In ideal scenarios, the 10-ns measurement range contains a fixed number of bins (approximately 240) with LSB size around 41.7 ps. However, numerous non-ideal factors cause actual LSB to vary. Tested DNL and INL of the second TDC level across 8 channels show high consistency, as shown in Fig. 6(a) and Fig. 6(b), respectively. Second-level non-linearity mainly arises from VCDL mismatches in DLL-1. Table 2 shows DNL and INL distribution ranges for each of the 8 channels over one clock period (10 ns).

Asynchronous measurement mode linearity was also assessed, with Ch-1 as start

channel and another channel as stop channel. Code density testing was repeated using one pulse generator providing Start at 4.00001 MHz and Stop at 4 MHz. Since only second and third level results are collected, the Start–Stop interval is randomly distributed within (0, 10 ns) with 100-MHz reference clock. Table 3 shows linearity performance for 7 channel combinations, demonstrating DNL better than 0.4 LSB and INL better than 0.5 LSB for all cases. Comparing single-channel and dual-channel results confirms that the asynchronous TDC inherently employing sliding scale technique provides significant linearity advantages.

Single-Shot Precision (SSP) was measured in asynchronous mode. The pulse generator output is split into two identical signals: one transmitted to the start channel (Ch-1) through a 0.1-m cable, the other to the stop channel (one of the other channels) through a 0.3-m cable—called Cable Delay Measurement Test [**?**]. The best uncalibrated SSP of 52.4 ps is achieved with Ch-1 and Ch-2 combination, as shown in Fig. 7(a). Precision can be improved using an INL look-up table [**?**]. The calibration principle is:

$$TDC_{CAL} = TDC_{RAW} + INL[TDC_{RAW}]$$

where TDC_{RAW} and TDC_{CAL} denote raw and calibrated TDC codes, respectively. Fig. 7(b) shows calibrated SSP of 46 ps. SSPs for other channel combinations are shown in Fig. 7(c), all within 45–70 ps after calibration.

Calibration effectiveness was validated by measuring SSP across input interval range (0.5 ns, 10 ns). As shown in Fig. 7(d), SSP results become more consistent after calibration. Since this INL-based calibration compensates for non-uniform LSBs, test results corroborate the theory, proving our test and calibration method correct. Accuracy, representing input–output error, was also measured across TDC dynamic range, as shown in Fig. 7(e). With metastability eliminated by the double-edge-triggered counter, no significant accuracy deviation was observed.

TDC precision can degrade due to cross-talk, causing Start or Stop edge distortion. Correlated and uncorrelated cross-talk are the two mechanisms. Uncorrelated cross-talk is difficult to evaluate, so we focused on correlated cross-talk [**?**]. An experiment studied cross-talk effects using adjacent channels Ch-1 and Ch-2 for Start and Stop timestamps, respectively. Input pads of these channels are close, making cross-talk effects more significant. Both Start and Stop frequencies are 4 MHz, with intervals T_m varied within (0, 249 ns). As shown in Fig. 7(f), rising edges distort each other at $T_m = 0$, and Stop rising edge distorts by Start falling edges at $T_m = 125$ ns. SSP evaluations with variable intervals show in Fig. 7(g) that SSP at $T_m = 0$ is significantly worse than other cases, but not significantly worse at $T_m = 125$ ns. This suggests cross-talk effects are greater when Start and Stop rising edges coincide. Due to asynchronous measurement mechanism and double-edge-triggered counter, metastability effects are negligible and SSP degradation can be explained by cross-talk. Therefore,

instances with correlated cross-talk should be excluded from TDC system operating modes.

Table 4 compares the proposed TDC with others suitable for multi-channel applications. Compared with delay line structures [**?**] and counter structures [**?**], the proposed TDC offers precision advantages. Versus ring oscillator-based structures [**?**, **?**], our design exhibits superior conversion linearity. The TDC in [**?**] also uses vernier controlled by dual DLLs but has worse linearity and slower conversion rate. [**?**, **?**] are Xilinx 7-series 28-nm FPGA-based TDCs, and our TDC performance remains competitive.

V. Summary

This work presents the design and experimental results of an 8-channel, high-precision TDC ASIC for STCF EMC. The proposed TDC uses a 3-level Nutt structure achieving wide dynamic range and high resolution. The sliding scale technique is employed and its role in improving conversion linearity is demonstrated. The prototype chip is implemented in standard 180-nm CMOS process with 1.55 mm $\times$ 1.42 mm die area. Testing results show the proposed TDC features 46-ps single-shot precision for the best channel, DNL better than 0.4 LSB, INL better than 0.5 LSB, and good consistency across all channels. Good performance consistency across all TDC channels is demonstrated.

Given the flexible vernier-type framework employed, our next steps are to further improve TDC resolution and expand to more channels. Future work will also investigate multi-channel synchronization and matching, jitter suppression, and temperature compensation techniques.

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Note: Figure translations are in progress. See original paper for figures.