A High-Precision Amplitude-Time to Digital Converter based on FPGA for Digital Multi-channel Analyzer

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Abstract

This paper presents a high-precision Amplitude-Time-to-Digital Converter (A-TDC) for use in a Multichannel Analyzer (MCA). Utilizing this method, the MCA quantifies and statistically analyzes the discharge time of nuclear pulse signals, ultimately obtaining the gamma energy spectrum. The autonomous linear discharge circuit presented in this paper significantly simplifies the components and control logic of conventional discharge circuits. By leveraging the underlying logic of the FPGA's internal carry-chain, a delay chain capable of precise time measurement for both leading and trailing edges is designed, resulting in a substantial reduction in logic resource consumption. The high-resolution TDC, designed based on the Xilinx Artix-7 series FPGA, achieves a resolution of 69.4 ps, and the average time measurement precision is 52.3 ps. The linear discharge circuit has an inherent nonlinearity of less than 0.05%, and the overall linearity is better than 0.1%. When used in conjunction with a $ $25 mm × 25 mm NaI(Tl) detector for measuring the 662 keV full-energy peak of a 137Cs source, the energy resolution achieved is 8.5%.

Full Text

Preamble

A High-Precision Amplitude-Time to Digital Converter based on FPGA for Digital Multichannel Analyzer

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MCA quantifies and statistically analyzes the discharge time of nuclear pulse signals, ultimately obtaining the gamma energy spectrum. The autonomous linear discharge circuit presented in this paper significantly simplifies the components and control logic of conventional discharge circuits. By leveraging the underlying logic of the FPGA's internal carry-chain, a delay chain capable of precise time measurement for both leading and trailing edges has been designed. Compared to using two delay chains for measuring the leading and trailing edges separately, this approach significantly conserves logic resources. The high-resolution TDC designed based on the Xilinx Artix-7 series FPGA achieves a resolution of 69.4 ps, with an average time measurement precision of 52.3 ps. The linear discharge circuit exhibits inherent nonlinearity of less than 0.05%, and overall linearity better than 0.1%. When used in conjunction with a Φ25mm$×$25mm NaI(Tl) detector for measuring the 662 keV full-energy peak of a ^{137}Cs source, the overall system achieves an energy resolution of 8.5%.

Keywords: Amplitude-time conversion; FPGA-TDC; Gamma energy spectrum; Constant current source discharge

Introduction

Digital multichannel analyzers have been extensively used in fields such as nuclear spectroscopy, environmental monitoring, nuclear accident response, and mineral resource exploration [**?**]. Digital pulse amplitude analyzers directly employ high-speed ADCs for full waveform sampling of pulse signals, followed by devices such as Field Programmable Gate Arrays (FPGA) and Digital Signal Processors (DSP) to perform digital filtering, pulse shaping, and amplitude extraction on the digitized signal [**?**, **?**]. These systems are particularly relevant for applications requiring amplitude measurements across dozens, hundreds, or even thousands of channels, such as multi-channel energy spectrum measurement, gamma irradiation imaging, and astronomical telescopes [**?**]. In such systems, the ADC circuit design faces significant complexity challenges. These systems typically require numerous high-speed ADC chips to accurately acquire nuclear information. However, high-speed ADCs are expensive, and as the number of channels increases, circuit complexity rises exponentially. Moreover, due to large differences in signal strength between channels, ADCs must also have high dynamic range to accommodate signals of varying amplitudes.

Time-to-Digital Converters (TDC) have been used in various fields such as high-energy particle measurement and phase-locked loops since the 1980s [**?**]. TDCs have transitioned from analog to digital implementations [**?**], and researchers have studied vernier, passive interpolation, and gated ring oscillator TDC structures to improve timing resolution and measurement range. Some of these structures can achieve sub-gate-level time resolution, and in certain applications, they can reach femtosecond (fs) level timing resolution [**?**]. TDCs are primarily implemented using Application-Specific Integrated Circuits (ASIC) and FPGAs. TDC systems based on ASIC offer better channel stability and consistency, whereas ASIC devices are complex to design and have high development costs.

In contrast, FPGA-based TDCs boast short design cycles, high flexibility, low cost, and high temporal resolution, with some designs achieving picosecond-level resolution [**?**]. The amplitude of the pulse signal output from a detector is proportional to the energy deposited by the radiation or particles in it. By using a peak detection and hold circuit, the pulse peak is stored in a holding capacitor. Then, a constant current source discharges the holding capacitor at a uniform rate, and the discharge time is proportional to the pulse amplitude. By measuring this discharge time, the energy deposited by the radiation can be accurately obtained.

Considering the strong competitiveness of FPGA-based high-precision TDC pulse amplitude analyzers in fields such as high-energy physics, radiation imaging, multi-channel energy spectrum measurement, and gamma irradiation imaging [**?**, **?**], this paper proposes an Amplitude-Time to Digital Converter for pulse amplitude measurement.

2 System Design

The high-precision A-TDC based on FPGA primarily consists of a signal conditioning circuit and a TDC implemented within the FPGA. The signal conditioning circuit mainly handles signal gain adjustment, peak-holding, constant-current discharge, and pulse-width conversion. The TDC in the FPGA comprises a fine counter, a coarse counter, and a Processing Unit. The nuclear pulse signal output from the NaI(Tl) detector, after appropriate gain adjustment, enters a peak-holding and constant current discharge unit. This unit converts the nuclear pulse signals into single-slope pulse signals whose widths are proportional to the peak amplitude of the nuclear pulse signals. Subsequently, a comparator transforms the single-slope pulse signals into square wave signals. The widths of these square wave signals are proportional to the amplitudes of the original nuclear pulse signals and are measured by the TDC, which consists of a fine counter based on the delay chain and a coarse counter in the FPGA.

2.1 Automatic Peak-Holding and Constant Current Discharge

In low-channel discharge measurement systems, typical components include decision-making circuits, linear gates, and constant-current discharge circuits. These components are further coordinated with specially designed switches to control the discharge process [**?**, **?**]. However, in multi-channel measurement systems, configuring a discharge control circuit for each channel would significantly elevate circuit complexity and complicate the control logic. To accommodate multi-channel measurement systems, simplify control logic, and reduce circuit complexity, this paper employs an automatic peak-holding and constant-current source discharging method, as depicted in Fig. 1a [Figure 1: see original paper].

After gain adjustment, the input nuclear pulse signal proceeds into the automatic peak-holding circuit and the constant-current discharging circuit. Due to the direct-current bias power supply Vb and diodes D1 and D2, the incoming nuclear pulse signal charges the peak-holding capacitor Ch. The charge stored in the peak-holding capacitor is proportional to the signal peak value, $Q(t) = C$

· V(1 − e⁻). The constant-current discharging mechanism is realized through the cooperation of transistor Q1 and resistors Rdis, R1, and R2. According to the voltage characteristics of the NPN (Negative-Positive-Negative) transistor base-emitter junction, Vb provides a stable static operating point for the Q1 base after the voltage drop across the two diodes, enabling the transistor to operate stably in the active region during the discharge process, with Vbe maintained at a constant value of about 0.6 V. During the discharging process, Vbe maintains a constant value of approximately 0.6 V and the current fluctuation into the base of Q1 is less than 0.05 µA, so its influence can be disregarded. By connecting resistor Rdis in parallel between the base and emitter of Q1, the discharge current of Ch is directed through Rdis. Additionally, since Vbe remains constant, the current flowing through resistor Rdis during discharging remains consistent at I Vbe, facilitating the achievement of constant-current discharging.

Upon the arrival of the nuclear pulse signal, the capacitor Ch undergoes swift charging. Due to the exceptionally brief rise time of the nuclear pulse signal, the voltage across Ch rapidly attains the peak value of the signal. The presence of Vb positions transistor Q1 within its amplification zone. Simultaneously, as the input nuclear pulse signal charges Ch, the constant-current discharging circuit operates to concurrently discharge it. Consequently, a minor charge loss occurs during the charging phase, leading to a divergence between the peak voltage achieved by capacitor Ch and the peak value Vamp of the nuclear pulse signal. This discrepancy is influenced by both the rise time of the nuclear pulse signal and the magnitude of the discharging current.

Using the NaI(Tl) detector as an illustrative example, the input signal's rise time ranges between 100 ns and 300 ns. With a constant discharge current of 6 µA and an input signal amplitude of 1 V, the peak voltage experiences a reduction of 60 mV. It is evident that the constant current discharge influences the capacitor's peak voltage by approximately 6%, while having a negligible impact on the amplitude conversion process. To maintain a uniform discharge process, a diode D2 is placed above Ch. During the slow discharge of Ch, D2 remains in the cutoff state, allowing current to flow only towards the subsequent circuit, with the discharge current Idis determining the entire discharge process rate. The peak-holding and constant current discharge circuit converts the input nuclear pulse signal into a single-slope pulse signal.

The circuit simulation results shown in Fig. 1b indicate that there is a small non-linear region at the end of the discharge process, which is primarily determined by the Volt-Ampere (V-A) characteristics of the diode. When the forward voltage applied to the diode is less than the threshold voltage, the diode exhibits high impedance, and the forward current is nearly zero. When the applied voltage exceeds the threshold voltage slightly, the internal PN junction's built-in electric field of the diode is neutralized. Consequently, the diode exhibits low impedance and enters the forward conduction region. However, at this initial stage of conduction, the voltage and current are not yet fully proportional. As

the external electric field continues to increase, the forward current of the diode increases rapidly, and the V-A characteristics become approximately linear, indicating that the diode is now in full conduction. Once the diode is in the forward-biased conduction state, the forward voltage drop across it remains essentially constant. From the simulation diagram, it can be observed that during the signal discharge process, the fluctuation of the discharge current Idis is less than 0.1 μA, while the discharge current is 5.875 μA. Testing has shown that the inherent non-linearity for signals with a peak-to-peak value of 0.4 V or greater is less than 0.05%, and the overall linearity is better than 0.1%. This signifies that the system has good linearity in converting amplitude values into time widths and responds well to small signals within a certain range, as illustrated in Fig. 1b.

The signal transformation circuit converts the single-slope pulse signal into a square wave signal that complies with the FPGA input levels, thereby facilitating the measurement of pulse width time. The transformation circuit employs a comparator to perform threshold comparison on the single-slope pulse signal outputted from the previous stage, converting it into a square wave signal. The bandwidth of a comparator determines the range of signal frequencies it can respond to. If the bandwidth is insufficient, it will result in increased setup time for the output signal and a longer rise time for the output signal's leading edge. A longer leading edge can increase the uncertainty in TDC time measurements. Therefore, it is necessary to choose a high-speed comparator to ensure the resolution and accuracy of the system's measurements.

The DC bias voltage Vb provides a DC offset of approximately 0.53 V for the signal. The overall analog circuit noise is less than 10 mV; therefore, the comparator threshold must be at least 0.54 V to avoid the impact of noise on pulse width conversion. To test the relationship between the pulse width conversion circuit performance and the setting of the comparator threshold, input amplitudes ranging from 0.1 V to 0.2 V were selected, with a test point every 20 mV. From 0.2 V to 0.4 V, a test point was selected every 50 mV, and from 0.4 V to 1.2 V, a test point was chosen every 100 mV. At each test point, over 100,000 sets of sample data were collected. Additionally, different comparator threshold values were selected based on the actual signal discharge baseline for testing, specifically 0.55 V, 0.57 V, 0.60 V, 0.62 V, and 0.64 V.

The final test results are shown in Fig. 1c. From Fig. 1c, it can be observed that when the peak-to-peak value of the input signal is less than 0.4 V, the relationship between the input signal amplitude and time does not exhibit a clear, linear one-to-one correspondence. The primary reason for this phenomenon can be attributed to the V-I (voltage-current) characteristics of the diode. According to the basic V-I characteristics of an ideal diode, when the forward voltage across the diode exceeds its forward voltage drop, the current through the diode undergoes an abrupt change. However, during actual testing, when the forward voltage is in the vicinity of the diode's critical conduction voltage, the diode exhibits a soft conduction phenomenon. This means that when the forward

voltage difference across the diode is slightly greater than the critical conduction voltage, the current does not undergo an abrupt change as per ideal diode characteristics; instead, it displays a nonlinear, smooth transition. Due to this soft conduction characteristic, when the peak-to-peak value of the input signal is relatively small, the relationship between Vpp (peak-to-peak voltage) and time is not entirely linear.

2.2 FPGA-TDC Design

The direct counting method utilizes a high-frequency clock to measure the width of the input signal. When the leading edge of the input signal arrives, the FPGA initiates counting, and halts it upon arrival of the trailing edge. By calculating the number of clock cycles elapsed between the start and end times, the time width of the input signal can be determined. Direct measurement of pulse width using clock counts offers a wide measurement range, but the period interval of the counting clock may introduce significant leading and trailing edge errors.

This paper utilizes the internal carry chain of the FPGA to construct a refined carry chain that precisely counts the leading and trailing edges of the pulse separately. A high-frequency clock is employed for coarse counting of the main pulse width, and the two counts are then summed to obtain the pulse width time. The carry chain is a fundamental structure within the FPGA. In the Xilinx Artix-7 series FPGA, the structure of the CARRY4 (Carry Chain Block 4) is depicted in Figure 2 [Figure 2: see original paper]. Each CARRY4 consists of a carry multiplexer (MUXCY) and an XOR gate, which together generate carry signals. The CI (carry input) is connected to the carry output of the previous stage, while the CO (carry output) serves as the carry output of the CARRY4. The signal S controls the output of the MUXCY.

This design establishes a carry chain delay measurement by cascading CARRY4 units, capturing the internal signals of the CARRY4, and subsequently extracting fine count time through encoding and decoding processes. By configuring the S[3:0] of CARRY4 to 1111, four MUXCY input signals are programmed to select the cascaded carry input and the carry-out of the previous stage. This interconnection links the CO (Carry-Out) with CI (Carry-In) within the CARRY4, forming a single CARRY4 delay module. Within this module, the carry signal traversing from CI to CO represents the minimum delay unit of the delay chain. Within the CARRY4 carry chain, there are tap signals designated as O[3:0] and CO[3:0]. Upon the arrival of the leading edge of the measured signal, each MUXCY triggers its corresponding CO output to transition from “0” to “1”. Conversely, when the trailing edge of the measured signal arrives, O becomes the XOR result of S and the carry signals CO and CI. Given that S is set to 1, O changes from “0” to “1”. Consequently, the sensitivity of the CO and O tap signals to the leading and trailing edges of the measured signal can be utilized to determine the precise moment of the square wave signal’s edge. This capability allows for the simultaneous measurement of both the leading and trailing edges of the signal using a single delay chain.

Figure 2 depicts the specific design approach of the FPGA-TDC, which incorporates a fine counter for measuring the temporal segments of both the front and back of the signal. In the initial delay unit, two delay flip-flops, TD and LD, are inserted to signify the valid leading edge or trailing edge. Following a delay of one clock cycle, the signal branches into two paths. One path directs to MUX(a) for selecting the encoding of the time signal's leading or trailing edge, while the other path passes through MUX(b) to choose the corresponding leading or trailing edge as a latch signal. Upon passing through flip-flop FF(a), the latch signal latches the result in the encoder and concurrently serves as the start and end signal for the coarse counting module. The latch signal, after traversing another flip-flop FF(b), generates the enable signal "Process En" for the Processing Unit module. Upon reaching the Processing Unit, "Process En" integrates the latched encoding result (fine count value) with the coarse count result to produce the final timing data, which is then written to the FIFO. Notably, no additional clocks are utilized during the encoding and data processing. Thus, the longest delay path of TD and LD spans from the edge indication signal to the FIFO write enable, consuming two system clocks. Consequently, the TDC designed in this paper has a maximum dead time of two clock cycles, significantly reducing the system dead time attributed to the TDC during measurement.

In the A7 series FPGAs, each clock domain encompasses 50 slices, equivalent to 50 CARRY4 resources. The theoretical delay time from CI to CO in each CARRY4 is approximately 98 ps [cite{39}], though actual measurements indicate a shorter duration. Prior to designing the delay chain, it is crucial to estimate the number of delay units and ensure it remains below 50 to prevent the delay chain from spanning across banks, which could result in uneven delays.

The Encoder module translates the time signal into a digital signal code, resulting in a thermometer code with a bit width equivalent to the carry chain, exemplified by "111111…00000". In the Processing Unit module, which includes a thermometer code decoding circuit, the time data is derived by counting the "1"s in the thermometer code. To enhance FPGA resource utilization and minimize system dead time during measurement, this paper adopts a binary search method for decoding the thermometer code. This method offers favorable time and space complexity, allowing for the swift and efficient identification of the transition point from "0" to "1" in the code [cite{40}].

Regarding the output signals from the detector, the majority fall within the system's dynamic range. However, a minority of signals exhibit intensities below the dynamic range's lower limit, particularly those with widths less than half of the sampling clock period. For these signals, the TDC measurement circuit may only capture one edge (leading or trailing) when attempting to detect both, resulting in inaccuracies. To address this challenge, an event assembly circuit, implemented using a finite state machine (included in the Processing Unit module shown in Fig. 2), is tasked with screening all signals to ensure data accuracy and completeness.

2.3.1 TDC Code Density and Non-linearity Test

Due to the influence of manufacturing processes and layout routing, it is difficult for each delay unit in the FPGA's carry chain to have exactly the same delay time. Therefore, it is necessary to precisely calibrate the delay time of each delay unit in advance. To achieve this goal, the standard code density test method [cite{41,42}] is commonly used to measure the delay characteristics of each delay unit.

A large number of pulses of randomly varying widths, uniformly distributed within [0, T], are used as test signals for the TDC (where T is the period of the standard system clock). If the delay time of each delay element were the same, when there are enough test samples, the number of signals falling on each delay element should be evenly distributed. However, since the delay time of each delay element varies, the uneven distribution of signals across the delay elements is determined by the additional delay time. By recording the total number of times each delay element is hit by events, we can determine the corresponding code density for each delay element.

Assuming there are enough test samples and ignoring the non-uniform distribution factors of the input signal, the delay time of each delay element is proportional to the number of pulses that fall into it. This means that the more times a random input signal falls into a particular delay unit, the longer its delay time and the greater its code density. Since the sum of the delay times of all delay units equals one reference clock cycle, by multiplying the proportion of the code density occupied by each delay unit with the sampling period T, one can determine the delay time of each delay unit in the delay chain.

To ascertain the precision and dependability of the measurement outcomes, it is imperative to establish the requisite number of test samples prior to conducting the tests. Suppose the range of values for the individual pulse signals is uniformly distributed across the interval [0, Tc], with P representing their probability density function, expressed as P = 1/Tc. The likelihood of a pulse occurring within a specific delay element is directly proportional to the delay time Td of that element, with the probability given by Pd = Td/Tc. The frequency of occurrence within delay element i is denoted by ni = N × Pi = N × Ti/Tc. By leveraging the relationship between the density of the delay element codes and the sampling interval, the delay time $\hat{T}$i for the i-th delay element can be derived, as presented in Eq. (1):

$\hat{T}$i = (Ni/N) × Tc

By tallying the number of events Ni that occur in each successive delay element, one can ascertain the delay times for all elements. Subsequently, summing the delay times of the initial i elements yields the cumulative delay time ti experienced by the pulse as it reaches each specific delay element, as detailed in Eq. (2):

ti = Σ_{n=0}^{i} $\hat{T}$n

Therefore, when a random signal falls within a delay element, the measured value should be taken at the midpoint of the delay element to minimize the standard deviation of the measurement value. From Eq. (4), it is evident that an inadequate sample size results in excessive statistical errors, necessitating a specific requirement for sample size in code density testing.

For a finite number N of test events, the event count ni where the test pulse edge falls within a delay element follows a binomial distribution D(Ni) = N × Pi(1 - Pi), with the expected value n = N × Pi and the standard deviation σni = $\sqrt{}$[N × Pi(1 - Pi)]. Since all events are independent, the count values ni are also independent. Therefore, using Eq. (2) and (4), we can derive Eq. (5):

σ^2ti = Σ_{n=0}^{i} σ^2Tn + σ^2Ti = Σ_{n=0}^{i} σ^2nn + σ^2ni

In practice, the edge of the test signal falls within the interior of the i-th delay element, so there will be an error regardless of whether ti or ti-1 is chosen as the total delay time. Assuming the measured value is τ, then ti-1 < τ < ti, the variance σ^2 of τ is:

σ^2 = (1/(ti - ti-1)) _{ti-1}^{ti} (t - τ)^2 dt = [(ti - τ)^3 - (ti-1 - τ)^3] / [3(ti - ti-1)]

In Eq. (3), the standard deviation σ^2 reaches its minimum value when τ = (ti-1 + ti)/2. At this point, the observed value is t, as shown in Eq. (4):

t = (ti-1 + ti)/2

If the delay time of each delay element is equal, then the probability of a pulse falling on the i-th delay element is Pi = 1/S, where S is the number of delay elements in a delay chain. When i = S, i is the last delay element in the delay chain, and at this point, σi reaches its maximum value σmax:

σmax < $\sqrt{}$[Tc^2/(12S)]

Given that the external signal sampling clock designed in this study is 250 MHz, we have Tc = 4000 ps. To ensure that σmax does not exceed 40 ps, we set σmax = 40 ps. Substituting this value into Eq. (6), we get N ≥ 10000, which means the number of test events must not be less than 10000.

Hence, a signal generator is employed to generate 20000 random pulse width square waves. It is essential that the external sampling clock and the measurement sampling clock are not sourced from the same origin, and they should not be in an integer multiple relationship, as this would result in a fixed phase between them, which is inadequate for achieving complete randomness. The sampling clock is a 300 MHz clock generated by a PLL from an external crystal oscillator, with a period of 3.33 ns. According to the theoretical delay time of 98 ps, 34 CARRY4 delay elements would be required. However, after testing with random signals, it was found that at a clock frequency of 300 MHz, the actual delay time of each CARRY4 delay element is less than 98 ps. Therefore, for both the leading and trailing edges, there are effectively 48 delay elements, which is fewer than the maximum number of delay elements per bank mentioned

earlier. Thus, using a 300 MHz clock as the coarse counting clock can meet the design requirements, and the delay chain is theoretically expected to exhibit better linearity.

The test results are shown in Fig. 3a-d. If automatic layout and routing are performed using software, it is common for the delay chain to span different Banks, leading to uneven delays. The test results in Fig. 3a-d show the code density test results after manual layout and routing, where the distribution of each delay element is more uniform. The delay differences between each delay element are mainly attributed to the time differences in the sampling clock reaching various registers, as well as the inherent non-uniformity of the semiconductor manufacturing process.

The nonlinear performance of a TDC is primarily assessed using two metrics: Differential Nonlinearity (DNL) and Integral Nonlinearity (INL). These parameters reflect the uniformity of the TDC's bin widths. Fig. 3e-h illustrates the DNL and INL of delay units in a manually routed delay chain within a digital circuit. The formulas for calculating DNL and INL are as follows:

DNLi = LSBi - LSB INLi = Σ_{n=0}^{i} LSBn - i × LSB

In this context, LSBi refers to the delay time corresponding to the i-th delay element. When analyzing this section, LSBi represents the number of measured pulses for the corresponding delay element, and the time resolution is the average number of pulses.

The differential nonlinearity for the leading edge is optimized to the range [-0.91, 0.42], and the integral nonlinearity is [-1.30, 0.33]. For the trailing edge, differential nonlinearity is [-0.75, 0.63], and the integral nonlinearity is further optimized to the range [-1.0, 0.33]. In an ideal scenario, the delay time of each delay unit that constitutes a TDC should be identical, which implies that the width of all bins should be exactly the same. The smaller the bin width, the higher the resolution of the TDC. The average resolution of a TDC can be represented by Eq. (9), which takes into account the uniformity of all delay units and the impact of bin width on resolution:

LSB = Tc/N

In the TDC delay chain, N represents the number of effective delay units within the time Tc. For the TDC delay chain designed in this paper with 48 effective delay units and a sampling clock of 300 MHz, Tc = 3333.3 ps. The average resolution of the delay chain is LSB = 69.4 ps.

2.3.2 RMS Accuracy Analysis

By conducting multiple measurements within a fixed time period and analyzing the dispersion of the resulting data, the root mean square (RMS) accuracy of TDC measurement data can be assessed. RMS accuracy is an important metric for evaluating the precision of TDC measurement results in characterizing pulse

width signals. RMS accuracy reveals the degree of deviation of the measured values from the ideal values. The calculation of RMS follows Eq. (10):

RMS = √[(1/(N-1)) × Σ_{i=1}^{N} (Xi - (1/N) × Σ_{i=1}^{N} Xi)^2]

Where N denotes the number of measurements, and Xi represents the data from the i-th measurement. The more data tested for a pulse of the same time width, the more accurate the calculated RMS value becomes. Fig. 4a [Figure 4: see original paper] shows the RMS test results for a square wave signal with a pulse width of 800 ns, with an RMS value of 53.4 ps.

To comprehensively evaluate the performance of the TDC designed in this study over a wide range of times, we adopted a strategy of selecting test points in stages: within the 0 to 1 µs range, a test point was set every 100 ns; within the 1 to 10 µs range, a test point was set every 1 µs; within the 10 to 40 µs range, a test point was set every 2 µs. This distribution of test points ensures an accurate assessment of the TDC's performance across different time scales. At each test point, we collected more than 100,000 sets of sample data to ensure the statistical reliability of the data. Through the analysis of this data, we obtained the distribution of time measurement accuracy results as shown in Fig. 4b.

Based on these measurement data, we calculated that the average accuracy of the TDC designed in this study in time measurement is 52.3 ps. This result not only demonstrates the high performance of the TDC in the time range from nanoseconds to microseconds but also verifies its application potential in the field of high-precision time measurement. Using the same precision evaluation method as mentioned above, we added three more measurement channels identical to the system and tested the other three channels in the same way. Under the condition that all test conditions remain unchanged, the measurement results of time precision for each TDC channel are shown together. The measurement results indicate that the average precision of the four TDC measurement channels is approximately 50 ps in the range of 100 ns to 40 µs.

Main system parameters.

FPGA-TDC Parameter	Specification
FF Utilization rate	0.48%
LUT Utilization rate	0.60%
Resolution	69.4 ps
Measuring dead time	$ $30 ns
Analog Circuit Power dissipation	$ $100mW/channel||PCBarea|24\times$30 mm/channel
Measuring range	0-5.3 V

2.4 Gamma-ray Spectrometry Measurement and Analysis

Fig. 5a [Figure 5: see original paper] shows the system field joint test experimental diagram, which includes a radioactive source (I), a NaI(Tl) detector (II),

a main measurement board (III), a signal generator (IV), and an oscilloscope (V). In this study, we selected the CH132-07 type NaI(Tl) scintillation detector produced by Beijing Hamamatsu Photonics as the signal input source. This detector is equipped with a crystal of size Φ25mm$×$25mm, and its energy resolution for the characteristic peak of ^{137}Cs is better than 9% (nominal energy resolution). During the experiment, we used the "TDC scheme" and the "ADC scheme" for comparison.

In the experiment, we utilized ^{131}I and ^{137}Cs radioactive sources for energy calibration. The energy spectra obtained by these two schemes are shown in Fig. 5b. In the TDC scheme, the comparator threshold was set to 0.64 V. After energy calibration, it can be observed that the energy spectrum results of the TDC scheme and the ADC scheme coincide at the high, medium, and low energy characteristic peaks. The two characteristic peaks corresponding to the energies of 365 keV and 662 keV from ^{131}I and ^{137}Cs in the energy spectrum measurement results of the two schemes are clearly distinguished, and the peak positions of the characteristic peaks coincide. The Root Mean Square Error (RMSE) in the range of 70 keV to 1000 keV is 12.3. Under the same test conditions, the energy resolution of the ADC scheme for the characteristic peak of ^{137}Cs is 8.3%, while the resolution of the TDC scheme designed in this paper for the characteristic peak of ^{137}Cs is 8.5%.

3 Summary

This paper proposes a high-precision Time-to-Digital Converter (TDC) for use in a digital multichannel analyzer. By using this method, the digital multichannel analyzer quantifies and collects statistics on the discharge time of nuclear pulse signals, ultimately obtaining the gamma energy spectrum. Experimental results show that the TDC resolution can reach 69.4 ps on a Xilinx A7 series FPGA, the differential nonlinearity range of the leading edge measurement of the delay chain is [-0.91, 0.42], and the integral nonlinearity range is [-1.30, 0.33]; the differential nonlinearity range of the trailing edge measurement is [-0.75, 0.63], and the integral nonlinearity range is [-1.0, 0.33]. An analysis of the key parameters in the circuit's impact on the results reveals that, for signals with voltages higher than 0.4 V, the nonlinearity of the conversion results of the autonomous linear discharge circuit is less than 0.05%. Tests were conducted using a NaI(Tl) detector with a size of Φ25mm$×$25mm, alongside a linear discharge circuit and a high-precision TDC for the measurement of the 662 keV full-energy peak of the ^{137}Cs source, with an energy resolution of 8.5%. Under the same measurement conditions, the energy resolution measured using the ADC scheme was 8.3%. The analysis of the experimental results demonstrates the feasibility of the proposed method in the context of digital multichannel analyzers. Through innovating the front-end analog circuit, a compact and structurally simple autonomous linear discharge analog scheme is proposed, where the autonomous linear discharge structure, combined with the use of high-precision FPGA-TDC, provides a new solution for the acquisition and measurement of multi-channel systems.

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Note: Figure translations are in progress. See original paper for figures.