A 32-channel charge sensitive amplifier for delay-line readout of parallel plate avalanche counter array

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Abstract

Charge sensitive amplifiers for fast timing in delay-line readout of parallel plate avalanche counter (PPAC) array are designed. In total, 32 channels are realized on a single printed circuit board with operational amplifiers and other discrete components. Each channel is composed of an integrator, a pole-zero cancelation net, and a linear amplification stage, which can be accommodated to either positive or negative input signals. The design procedure is described in detail. The amplifier performance is calibrated with a signal generator. The gain approximately reaches #6;3 mV/fC with an RMS noise level of around 6 mV. In the application to a prototype PPAC, the amplifiers exhibit good practicality and stability.

Full Text

Preamble

A 32-Channel Charge Sensitive Amplifier for Delay-Line Readout of Parallel Plate Avalanche Counter Array

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We present the design of charge sensitive amplifiers for fast timing applications in delay-line readout of parallel plate avalanche counter (PPAC) arrays. A total of 32 channels are implemented on a single printed circuit board using operational amplifiers and other discrete components. Each channel comprises an integrator, a pole-zero cancellation network, and a linear amplification stage, and can be configured for either positive or negative input signals. The design procedure is described in detail. Amplifier performance is characterized using a signal generator, achieving a gain of approximately $±$3 mV/fC with an RMS noise level around 6 mV. When applied to a prototype PPAC, the amplifiers demonstrate excellent practicality and stability.

Keywords: Charge sensitive amplifier, Fast timing, Discrete components, Delay line, Parallel plate avalanche counter

Introduction

Radiation detectors are widely employed in heavy ion collision experiments to investigate nuclear structures and reaction dynamics. These detectors capture the kinematics of secondary protons, neutrons, or ions, while coincident measurements of secondary particles and particle-photon coincidences provide insights into collision dynamics, energy level structures, and other internal states of the reaction participants. Among the most commonly used detectors for such applications are low-pressure parallel plate avalanche counters (PPAC) [1, 2], semiconductor silicon detectors [3], and solid scintillation detectors [4, 5]. Compared to scintillation detectors, PPACs are particularly well-suited for fast timing and position-sensitive applications, simultaneously achieving sub-nanosecond timing resolution and sub-millimeter position resolution over sensitive areas of several hundred square centimeters. Relative to silicon detectors, PPACs offer greater radiation tolerance and cost-effectiveness.

To study Coulomb excitation of atomic nuclei [6], we are developing a PPAC array consisting of 20 PPAC units that will cover nearly 4π solid angle around a solid target, similar to the CHICO2 array [1]. During projectile-target collisions, both nuclei can be excited through Coulomb interactions, subsequently emitting gamma rays during de-excitation. The PPAC array detects the two-dimensional positions and flight time differences of recoil and scattered nuclei, enabling particle identification and Doppler correction of gamma-ray energies [7]. Each PPAC unit achieves sub-nanosecond timing precision via signals from the membrane electrode and sub-millimeter position resolution through four sig-

nals from two perpendicular delay lines. The delay-line signals and membrane signals have opposite polarities and are immediately processed by preamplifiers that output negative voltage pulses to subsequent discriminators. Consequently, both positive and negative detector current pulses must be converted to negative voltage pulses. Since each PPAC unit requires five readout channels, a total of 100 channels is needed.

Preamplifier performance directly impacts the resolution of the detector system, prompting the development of various customized preamplifiers for different detectors. Multichannel preamplifier integration schemes can be broadly classified into three categories. First, pixel-level integration using detector-specific integrated circuits (pixel ASICs) such as TaichuPix [8], JadePix [9], Timepix [10], Supix [11], ALPIDE [12], Topmetal [13], Nupix [14], and IMPix [15]. In these systems, the preamplifier and subsequent electronic stages are photolithographically fabricated adjacent to the detector sensor in the same substrate or connected via eutectic solder bumps. With pixel sizes of tens to hundreds of micrometers, these systems achieve micrometer-level position resolution and are employed as vertex or tracking detectors in large-scale collider experiments requiring thousands of high-density electronic channels [8–12], or in applications demanding ultra-high position resolution such as beam telescopes [16] and X-ray imaging [17].

Second, chip-level integration encapsulates several to over a hundred channels of front-end electronics (FEE), including preamplifier stages, in a single semiconductor chip. Representative examples include SAMPA [18], PIST [19], AGET [20], the ASIC developed for CdZnTe and Si-PIN detectors [21], and the micromegas readout ASIC [22]. Connections between detector electrodes and FEE are established via transmission lines, typically on printed circuit boards (PCBs). Separating the FEE from the detector eliminates the size constraints encountered in pixel ASICs while maintaining high circuit density, making this scheme widely adopted in large-area detectors and applications requiring high-density readout electronics. Examples include the time projection chamber (TPC) in the ALICE experiment [18], micro-pattern gaseous detectors [22, 23], avalanche photodiode array detectors [24], the silicon tracker and BGO calorimeter on the DAMPE satellite [25, 26], Compton telescopes for dose monitoring in hadron therapy [27], and positron emission tomography (PET) detectors [28, 29].

Third, board-level integration typically realizes several to tens of channels on a single PCB, with each channel constructed from discrete components including operational amplifiers (OPAs), resistors, and capacitors. This approach is commonly adopted when several to hundreds of channels are required and board-level circuit density is acceptable. Compared to chip-level implementations, the dynamic range and circuit logic can be more conveniently and economically adjusted to meet various requirements by selecting appropriate components from the commercial market. Typical applications include the SPA02-16 and SPA03-16 preamplifier modules for silicon detectors [30], the multi-purpose TPC at CSNS Back-n [31], the NEXT experiment searching for 0 $\beta\beta$ decay [32, 33],

scintillation detector arrays for PET [34, 35], CZT-based gamma-ray spectrometers [36], and the ITER radial X-ray camera [37].

In this work, we adopt the third scheme and design a versatile 32-channel charge sensitive amplifier (CSA) for our PPAC array under development. Section II describes the schematic and PCB design of the amplifier, Section III presents performance calibrations using a signal generator and oscilloscope, Section IV shows test results from a prototype PPAC application, and Section V concludes the work.

II. Schematic Circuit Diagram and PCB Design

Typical PPACs employ delay-line readout schemes [38] requiring fast timing amplifiers. The characteristic fast response of PPACs is summarized in Table 1 . Although 10^6 to 10^7 electron-ion pairs can be generated in avalanche multiplication [39, 40], only approximately 10% of the electrons contribute to the fast signal [38, 41]. The rise time is typically 5–10 ns [38–42], with a full width around 15 ns [39, 41]. Consequently, the maximum current is estimated to be several microamperes.

The preamplifier is designed to convert the PPAC output charge into voltage pulses several hundred millivolts in amplitude, with pulse widths comparable to the original detector response time to enable high counting rates.

A. Schematic Design

Each CSA channel consists of two OPA circuit stages. The first stage is a charge integrator (Qint), and the second is either a non-inverting amplification (NinvAmp) or inverting amplification (InvAmp) stage to accommodate different detector response polarities. Figure 1 [Figure 1: see original paper] shows the schematic diagrams for (a) Qint + NinvAmp and (b) Qint + InvAmp configurations, respectively.

The Qint input is AC-coupled to the detector electrode via a single-ended 50 Ω transmission line. To control noise levels at the Qint output, a long decay time constant of 1 μs is implemented, which can cause significant signal pile-up and DC voltage shift at high counting rates. Therefore, a pole-zero cancellation (PZC) network is inserted between the Qint stage and the subsequent linear amplification stage.

We employ the OPA657 [43] and OPA847 [44] from Texas Instruments in the first and second amplifier stages, respectively. Both are voltage feedback amplifiers featuring very low input voltage noise density, while the JFET-input stage of the OPA657 provides much lower input current noise density and input bias current. Using the OPA657 in the first stage thus favors lower noise and higher DC precision.

The signal-to-noise ratio (SNR) of the final output is principally determined by the SNR of the Qint output. As a compromise between noise

level and conversion gain, we select feedback capacitor C_{{{int}}*{{f1}}} = 5 pF and feedback resistor R{{{int}}*{{f1}}} = 200 kΩ (with parasitic capacitance in parallel of about 0.1 pF). The time constant τ{int} = R_{{{int}}*{{f1}}} × C{{{int}}*{{f1}}} = 1 μs. The Qint stage gain is G{int} = 1/C_{{{int}}*{{f1}}} under normal operating conditions where A{ol} × C_{{{int}}*{{f1}}} C_s + C{{{int}}*{{f1}}}, with C_s being the total input capacitance and A{ol} the OPA open-loop gain.

To stabilize the Qint circuit, resistor R_{{{int}}*{{g1}}} = 10 Ω in series with capacitor C{{{int}}_{{g1}}} = 10 pF is installed for input lag compensation. The coupling capacitor C_c is set to 10 nF, with self-resonant frequency near the input signal bandwidth. Resistor R_c = 50 Ω serves as the termination resistor for impedance matching to the 50 Ω input transmission line.

The InvAmp stage gain G_{inv} = -R_{{{inv}}*{{f1}}/R{{{inv}}*{{g1}}}, and the NinvAmp stage gain G{ninv} = 1 + R_{{{ninv}}*{{f1}}/R{{{ninv}}*{{g1}}} are tuned by adjusting four resistors. The feedback resistors are R{{{inv}}*{{f1}}} = R{{{ninv}}*{{f1}}} = 500 Ω, while resistors R{{{inv}}*{{g1}}} and R{{{ninv}}*{{g1}}} are fixed at 10 Ω. Capacitors C{{{inv}}*{{f1}}} and C{{{ninv}}*{{f1}}}, together with parasitic capacitance in parallel, function as feedback lead compensation to stabilize circuit operation. After fine adjustment, C{{{inv}}*{{f1}}} = C{{{ninv}}*{{f1}}} = 0.5 pF are installed. Pull-down resistors R{{{inv}}*{{g1}}} 9.8 Ω and R{{{ninv}}*{{g1}}} 9.8 Ω at the non-inverting OPA847 inputs suppress output DC error caused by input bias current. Capacitors C{{{inv}}*{{g2}}} = 10 nF and C{{{ninv}}*{{g2}}} = 10 pF are placed in parallel with R{{{inv}}*{{g2}}} and R{{{ninv}}_{{g2}}}, respectively, minimizing output noise contribution from the resistors without significantly impacting the PZC network. Resistor R_o = 50 Ω provides source-end impedance matching to the 50 Ω output transmission line.

The OPA847 gain-bandwidth product is GBW_{847} = 3.9 GHz. The critical input amplitude before slew rate limitation begins is V_{{{847}}*{{crit}}} = SR{847}/(2π × GBW_{847}) = 38.8 mV, where SR_{847} = 950 V/μs is the slew rate. For a gain of 50 V/V, this corresponds to 1.9 V output voltage. The full power bandwidth (FPB) of the OPA847 at $±5V power supply is FPB_{847} = SR_{847}/(2 $ × V_{{{847}}*{{sat}}}) = 45.8 MHz, where ±V{{{847}}_{{sat}}} = $±$3.3 V is the output voltage swing.

In the Qint + NinvAmp configuration, the PZC circuit consists of C_{{{ninv}}*{{pz}}} = 1 nF, R{{{ninv}}*{{pz}}} = 1 kΩ, and R{{{ninv}}*{{g2}}} = 9.8 Ω, satisfying the condition τ{{{ninv}}*{{pz}}} = τ{int}. However, in the Qint + InvAmp configuration, the PZC circuit comprises C_{pz} = 1 nF, R_{{{inv}}*{{pz}}} = 500 Ω, and R{{{inv}}*{{g2}}} = 10 Ω, which breaks the equality τ{inv} ≠ τ{int}. If R{{{inv}}*{{pz}}} were set to 1 kΩ to enforce equality, significant overshoot would appear at the decay edge end, likely because the inverting OPA847 input is no longer at virtual ground. With R{{{inv}}*{{pz}}} = 500 Ω in the present circuits, both overshoot and resultant overcompensation remain at the noise level, as shown in Fig. 3 [Figure 3: see

original paper]. The PZC output signal decay time constant is τ\{pz\} 10 ns.

For input charges of 10^5 to 10^6 equivalent electrons, the Qint output pulse height is expected to be 3.2 mV to 32 mV. The PZC network roughly halves this amplitude to 1.6 mV to 16 mV due to ballistic deficit. This signal is further amplified by 51× in the NinvAmp stage or -50× in the InvAmp stage. Finally, the impedance matching resistor R_o halves the voltage transmitted to the subsequent 50 Ω transmission line. Therefore, the final output pulse height ranges from 40 mV to 400 mV, corresponding to an estimated conversion gain of 2.5 mV/fC, which agrees with the calibrated gain in Section III B.

B. PCB Layout and Routing

On a rectangular 10 cm × 20 cm PCB, 4 × 8 preamplifiers are arranged in a planar array, as shown in Fig. 2 [Figure 2: see original paper]. The pad layout and routing are identical for every unit. By marking certain pads as DNP (do not populate), considerable flexibility is available for circuit adjustment, allowing implementation of both CSA configurations. In Fig. 2, the 1st and 3rd rows are Qint + NinvAmp amplifiers, while the 2nd and 4th rows are Qint + InvAmp circuits. Input and output signals are routed through surface-mount board-to-board (BTB) connectors. Adjacent signal pins on each connector are isolated by pairs of pins independently connected to power and ground planes, minimizing connector-mediated crosstalk, unifying signal return paths, and reducing power-ground impedance. Two LEMO connectors soldered on the bottom provide power supply during circuit testing.

The PCB stackup design is detailed in Table 2 . The stackup comprises ten layers: the second and bottom layers are both ground planes for improved electromagnetic compatibility (EMC). Between them, four signal layers are interleaved with ground or power planes. Consequently, all 32 input and 32 output signal traces are striplines routed in parallel. Signal trace impedance is adjusted to 50 Ω with trace width set to 9 mil. The minimum separation between adjacent traces is at least 120 mil if they reside in the same layer, 60 mil if in adjacent signal planes, and 0 if three layers apart. Except for 16 parallel signal traces (8 input, 8 output) on each signal plane, the remaining area is filled with grounded copper, providing enhanced decoupling for power planes. A grounded guard ring surrounds each channel on the top layer to suppress crosstalk, with stitching vias extensively placed along guard rings, PCB borders, and both sides of every signal trace.

III. Performance Tests

The Qint + NinvAmp and Qint + InvAmp channels used for performance calibration are indicated as (a) and (b) in Fig. 2, respectively. Amplitude-frequency characteristics and linearity are tested by connecting resistor R_\{test\} = 20 kΩ in series with capacitor C_c. A series of voltage signals is fed to each circuit through R_\{test\}, which converts voltage signals to current signals; the input

charge signals are simply the integration of the respective current signals. Output signal amplitudes are measured with an oscilloscope (12-bit analog-to-digital converter, 1.5 GHz bandwidth, 2.5 GS/s sampling rate). Figure 3 [Figure 3: see original paper] presents CSA outputs together with the equivalent input charge signal. The input voltage pulse has rise time, fall time, and full width at half maximum of 2 ns, 2 ns, and 10 ns, respectively. The leading edges of the input charge signal, Qint + NinvAmp output, and Qint + InvAmp output are 8.1 ns, 7.1 ns, and 7.4 ns, respectively, with amplitudes of -481.5 fC, 1.326 V, and -1.471 V.

A. Bandwidth

Sinusoidal voltage signals from 1 MHz to 100 MHz are fed to each circuit via the R_{test} resistor, with output amplitudes measured using an oscilloscope. The amplitude-frequency responses are plotted in Fig. 4 [Figure 4: see original paper]. The -3 dB bandwidths of the Qint + NinvAmp and Qint + InvAmp circuits are determined to be 18 MHz and 21 MHz, respectively. As analyzed in Section II A, the linear amplification stage bandwidth is much larger than these measured values, indicating that the overall bandwidth is dominated by the Qint stage and PZC network, consistent with the ~10 ns decay time constant. The PZC output leading edge is typically faster than the decay edge, as the full PPAC response width is less than 20 ns, also illustrated in Fig. 3.

B. Linearity

Input charge signals similar to those in Fig. 3 are used, varying only in total input charge. The output pulse amplitude evolution with total input charge is shown in Fig. 5 [Figure 5: see original paper]. Conversion gain is determined by fitting the data, yielding -2.772 mV/fC and 3.083 mV/fC for the Qint + NinvAmp and Qint + InvAmp circuits, respectively. The measured input ranges are -14.4 fC to -577.8 fC and -14.4 fC to -529.7 fC, with linear correlation coefficients of -0.99989 and 0.99990. The corresponding integral nonlinearities are $±$1.46% and $±$1.29%. Since energy deposition by incident particles in PPACs and charge avalanche amplification exhibit fluctuations much larger than these nonlinearities, the circuit linearities are acceptable.

C. Noise and Baseline

The RMS noise evolution with detector capacitance is measured by mimicking detector capacitance C_d with a capacitor soldered between the channel input pad and a ground pad under the input BTB connector. The data are shown in Fig. 6 [Figure 6: see original paper], with each dataset fitted by a cubic polynomial. For the Qint + NinvAmp and Qint + InvAmp circuits, the zero-capacitance RMS noises are 5.85 mV and 6.59 mV, respectively. Noise evolution is dominated by linear coefficients of 6.58×10^{-2} and 9.27×10^{-2}, respectively, and modified by quadratic coefficients of -5.01×10^{-4} and -9.84×10^{-4}, and cubic coefficients of 1.60×10^{-6} and 4.37×10^{-6}. The maximum baseline shift

for each output when varying detector capacitance is 1.35 mV and 6.12 mV, respectively, both smaller than the corresponding RMS noise.

D. Crosstalk

Crosstalk between channels is measured by feeding a charge signal identical to Fig. 3 into one channel with a 50 Ω load resistor installed at its output BTB connector, then observing any other channel's output via the corresponding BTB connector pins. Waveforms show no difference whether the input charge signal is present or not, indicating that crosstalk between any channels is completely submerged by noise.

IV. Application in PPAC

The CSA practicality is verified using a homemade PPAC prototype for one unit of the aforementioned array under development. The detector consists primarily of a cathode membrane and an anode readout PCB, as sketched in Fig. 7 [Figure 7: see original paper] (detailed elsewhere). Particle Cartesian coordinates (x, y) are read independently from two delay lines on the anode. During testing, an aperture mask is mounted on the membrane (also shown in Fig. 7), and ~5.4 MeV alpha particles passing through the apertures are detected.

Typical CSA waveforms are shown in Fig. 8 [Figure 8: see original paper]. The trigger signal (S0) is read from the membrane by one Qint + NinvAmp amplifier, while four signals (Sx1, Sx2, Sy1, Sy2) are read from the delay lines by four Qint + InvAmp amplifiers. Note that membrane and delay-line signals originate from independent events without temporal correlation; they are shown together only to illustrate the common temporal sequence where the membrane signal precedes delay-line signals. The leading small positive peak followed by a large negative peak in each delay-line signal indicates bipolar output current pulses, likely caused by induction between the membrane and anode.

The five analog CSA signals are fed to an ORTEC CF8000 constant fraction discriminator [45]. The resulting five logic signals are processed by a CAEN V775 time-to-digital converter (TDC) module [46]. Digital times of the four delay-line signals (tx1, tx2, ty1, ty2) are measured relative to trigger time t0, which signifies particle arrival time. Coordinates are calculated by:

$$x = (tx1 - tx2)/(tx1 + tx2 - ts) \times HL$$
$$y = (ty1 - ty2)/(ty1 + ty2 - ts) \times HL$$

where HL = 30 mm is the detector half-length in either x or y direction and ts = 3318 is fitted from the measured mask pattern. As shown in Fig. 9 [Figure 9: see original paper], the measured pattern faithfully reproduces the aperture mask geometry.

V. Summary

In summary, we have designed a 32-channel preamplifier for a PPAC array under development for Coulomb excitation studies of atomic nuclei. The amplifier is implemented on a 10 cm × 20 cm PCB using OPAs and discrete components. Each channel is charge-sensitive, essentially comprising an integrator, a pole-zero cancellation network, and a linear amplification stage. Channels can be configured for either positive or negative inputs (Qint + NinvAmp and Qint + InvAmp, respectively). The two circuit configurations achieve bandwidths of 18 MHz and 21 MHz, integral nonlinearities of $±$1.46% and $±$1.29%, and zero-capacitance noise levels of 5.85 mV and 6.59 mV, respectively. Baseline shift in either circuit is smaller than the RMS noise, and no crosstalk is observable between channels, thanks to careful PCB layout and routing. In prototype PPAC applications, both circuits exhibit good practicality and stability. This multichannel preamplifier is expected to be deployed in the PPAC array.

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Data Availability: Related data are available from the corresponding author upon reasonable request.

Declarations of Conflict of Interest: The authors declare no competing interests.

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Note: Figure translations are in progress. See original paper for figures.