Performance Analysis of Digital Flux-locked Loop Circuit with Different SQUID V-ϕ Transfer Curves for TES Readout System

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Abstract

A superconducting quantum interference device (SQUID), functioning as a non-linear response device, typically requires the incorporation of a flux-locked loop (FLL) circuit to facilitate linear amplification of the current signal transmitted through a superconducting transition-edge sensor (TES) across a large dynamic range. This work presents a reasonable model of the SQUID-FLL readout system, based on a digital proportional-integral-differential (PID) flux negative feedback algorithm. This work investigates the effect of V-ϕ shape on the performance of digital FLL circuits. Such as the impact factors of bandwidth, design limits of slew rate of the system and the influence of the shapes of SQUID V-ϕ curve. Furthermore, the dynamic response of the system to X-ray pulse signals with rise time ranging from 4.4∼281 s and amplitudes ranging from 6∼8 $_0$ was simulated. All the simulation results were found to be consistent with the existing mature theories, thereby validating the accuracy of the model. The results also provide a reliable modelling reference for the design of digital PID flux negative feedback and multiplexing SQUID readout electronic systems.

Full Text

Preamble

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A superconducting quantum interference device (SQUID), functioning as a nonlinear response device, typically requires incorporation of a flux-locked loop (FLL) circuit to facilitate linear amplification of the current signal transmitted through a superconducting transition-edge sensor (TES) across a large dynamic range. This work presents a reasonable model of the SQUID-FLL readout system based on a digital proportional-integral-differential (PID) flux negative feedback algorithm and investigates the effect of V- shape on the performance of digital FLL circuits, including impact factors on bandwidth, design limits of system slew rate, and the influence of SQUID V- curve shapes. Furthermore, the dynamic response of the system to X-ray pulse signals with rise times ranging from 4.4 281 µs and amplitudes ranging from 6 8 $_0$ was simulated. All simulation results were found to be consistent with existing mature theories, thereby validating the accuracy of the model. These results also provide a reliable modeling reference for the design of digital PID flux negative feedback and multiplexing SQUID readout electronic systems.

Keywords: TES, SQUID, Digital flux-locked loop, Readout system

INTRODUCTION

As an ultra-low-noise detector, a superconducting transition-edge sensor (TES) can achieve an energy resolution ranging from several to several tens of eV [1–3]. To ensure a high signal-to-noise ratio for TES, a low-noise direct current superconducting quantum interference device (SQUID) is typically used to couple the TES current and perform readout [4]. However, SQUID is a nonlinear device that can only guarantee linear amplification of the signal over a very small dynamic range. To enable the nonlinear SQUID to amplify the TES signal linearly over a larger dynamic range, it is necessary to construct a flux negative feedback lock loop (FLL) [5].

A significant benefit of employing a digital system to control a SQUID is the convenient manipulation of digitized signals. For example, the analog integrator and its reset circuit can be easily implemented using just a few lines of code [6, 7]. The reset circuit not only automatically resets the position of the V-curve prior to SQUID lock, but also automatically adjusts the position of the FLL circuit working (locking) point. It has been demonstrated that digital FLL can substantially increase the dynamic input range of a SQUID by using flux-quanta counting and dynamic field compensation (DFC) methods [8]. Noise spectral density measurements show that digital FLL systems perform similarly to analog FLL controllers in previous work [9]. Digital FLL is now widely used in experiments such as magnetoencephalography (MEG) [10], magnetocardiography (MCG) [11], cosmic microwave background (CMB) detection [12], and X-ray and γ-ray detection [13, 14].

Previous works have mainly focused on digital FLL noise in these experiments and lack detailed description of the parameters that affect digital FLL system performance. For example, X-ray detection requires fast response, which necessitates a large slew rate for the FLL—typically several µs at 10 µA [15], corresponding to less than 2 $_0$ if the mutual inductance coefficient of the SQUID coil is 5 µA/ $_0$. In CMB detection experiments, digital FLL design requires large bandwidth to improve multiplexing numbers of readout channels [16]. To understand the performance of the digital SQUID-FLL system and design higher-performance readout circuits, we simulate the functional upper limits of the SQUID-FLL system. Little previous work has investigated the effect of different shapes of SQUID V- curves on the performance of digital FLL systems. Therefore, we analyze the effect of shapes on digital FLL performance using three different SQUID V- curve models.

The paper is organized as follows: In Section II, a sinusoidal-like approximation is made to the SQUID flux response model, and the fundamentals of the digital SQUID-FLL circuit are introduced. In Section III, we conduct comprehensive simulation analysis to validate the reliability of the model, primarily entailing simulations of the fundamental linear amplification readout function of the input magnetic flux signal, system bandwidth, and slew rate. Finally, the dynamic response of the system was simulated using pulse signals designed to resemble actual TES pulse signals with varying rise times and amplitudes. This SQUID-FLL readout system model can provide reliable design references for digital flux negative feedback (DFB) readout and multiplexing SQUID readout systems. Section IV concludes the paper.

II. PRINCIPLE OF DIGITAL SQUID-FLL MODEL

A. Simplified SQUID Transfer Model

The circuit model of the SQUID-FLL is illustrated in Figure 1. It comprises a single-stage SQUID. The current signal flowing through the TES is coupled with the input coil L_{in} and converted into a magnetic flux signal _{in}. Although different SQUID designs exhibit varying responses to input magnetic flux _{in}, they all share common characteristics: the response of SQUID to _{in} is periodic and nonlinear, resembling a quasi-sinusoidal curve [17]. Following magnetic flux locking, the error between the input and feedback magnetic flux is nearly zero, maintaining the total flux value in the SQUID at the working point. Theoretically, we only need to know the linear conversion coefficient of dV_{SQUID}/d _{in} at the lock point [18] but do not need to consider any shape of the V- response curve of SQUID, where V_{SQUID} represents the voltage across SQUID. To prove this point, we simulate the FLL circuit for different SQUID flux response cases in Section III.

We simplify the SQUID V- transfer model to a standard sinusoidal function. Assuming that the mutual inductance coefficient of the SQUID input coil is M_{in} and the mutual inductance coefficient of the feedback coil is M_{fb}, the relationship between the error signal $u_{err}(t)$ and the input and feedback magnetic fluxes can be expressed as follows:

$$u_{err}(t) = A\sin\left(\frac{2\pi}{\phi_0}\left(i_{in}(t)M_{in} - u_o(t)M_{fb}\right)\right) + \phi_{offset}G_1 + u_{offset}$$

where ${}_0$ denotes the quantum magnetic flux, $i_{in}(t)$ is the TES signal through the input coil, and the input flux is given by ${}_{in} = i_{in}(t)M_{in}$. ${}_{offset}$ is the magnetic flux bias applied to the input or feedback coils, $u_o(t)$ denotes the feedback voltage signal, R_{fb} denotes the feedback resistor, and the feedback magnetic flux is given by ${}_{fb} = u_o(t)M_{fb}$. G_1 denotes the linear gain of the room-temperature low-noise preamplifier, A denotes the amplitude of the voltage across the SQUID, and u_{offset} denotes the voltage offset of the amplifier.

B. Principle of Digital FLL

The fundamental structure of the FLL is the construction of a closed-loop negative flux feedback circuit based on operational amplifiers [19], as shown in the left part of Figure 1 [Figure 1: see original paper]. By analyzing the current relationships within the green dashed line in Figure 1, we can derive the circuit equation relating the output digital signal $u_o(n)$ to the input error signal $u_{err}(n)$:

$$u_o(n) = \left(\frac{R_2}{R_1}\right)u_{err}(n) + \left(\frac{\Delta t}{R_{1C}2}\right)\sum u_{err}(i) + \left[\frac{R_{2C}1}{\Delta t}\right]\left(u_{err}(n) - u_{err}(n-1)\right)$$

where R_1 and C_1 are the input resistance and capacitance, respectively, R_2 and C_2 are the feedback resistance and capacitance, respectively, P R_2/R_1 is a proportional parameter, I $\Delta t/R_1C_2$ is the integral parameter, D $R_2C_1/\Delta t$ is the differential parameter, and Δt represents the digital sampling period. $u_{err}(i)$ denotes the i-th sampled error signal after amplification by G_1, $u_{err}(n)$ is the average value of all sampled $u_{err}(i)$ in one frame as shown in Figure 2 [Figure 2: see original paper], and $u_o(n)$ is the n-th output (feedback) signal. Similarly, by digitizing Equation 1, we obtain:

$$u_{err}(i) = A\sin\left(\frac{2\pi}{\phi_0}\left(i_{in}(i)M_{in} - u_o(n)M_{fb}\right)\right) + \phi_{offset}G_1 + u_{offset}$$

The primary objective of PID algorithm design is calibration of the three aforementioned parameters. If these parameters are not adequately calibrated, system oscillations can occur, which may lead to extended lock (tracking) time or even loss of lock.

III. DIGITAL SQUID-FLL PERFORMANCE ANALYSIS

A. Basic Characterization of Digital SQUID-FLL System

In our simulation, we emulated typical conditions employed in laboratory tests, assuming that the SQUID is biased at a position with substantial voltage swing prior to flux locking. The current through TES $i_{in}(i)$ serves as the input reference for the SQUID input coil L_{in}. The default parameters used in the simulation, unless otherwise specified, are listed in Table 1 .

The rise times of TES signals are typically from several µs to several tens of ms [20, 21]. Consequently, the feedback algorithm design does not require consideration of future trend predictions. In the default settings, the input capacitance C_1 was set to 0, retaining only the P and I components. Considering prospective system design, the digital sampling time was established at 150 MSPS, with seven points sampled in each frame. The frame clock (feedback frequency) was approximately 21.4 MHz, and the effective system Nyquist bandwidth is approximately 10.7 MHz. In digital feedback, the error signal from the current frame is used to compute the feedback signal for the next frame, which results in a delayed feedback loop. This process is analogous to time-division multiplexing (TDM) SQUID readout logic, with the exception of row selection [22, 23]. In this configuration, the frame frequency equals the row selection frequency in TDM. The timing logic is illustrated in Figure 2. The average value of the error signal, $u_{err}(n)$, is calculated from the $u_{err}(i)$ to $u_{err}(i+6)$ values in the n-th frame, and the feedback signal $u_o(n)$ is then calculated for the next frame. It should be noted that our model does not account for other system delays, which typically amount to several hundred nanoseconds and may include transmission line delays. While these delays may reduce system bandwidth, they do not impact the model' s behavior.

Prior to SQUID locking, it is essential to adjust the locking work point. Typically, to ensure linear amplification with no offset, the lock point is selected at the zero point of the input flux ($_{in} = 0$) and the zero point of the output (feedback) flux ($_{fb} = 0$). The initial error signal is set to 0, and the bias signals $_{offset}$, u_{offset}, and settle time t_{set} are also set to 0. The results of the feedback locking are shown in Figure 3 [Figure 3: see original paper]. The absolute error signal does not exceed 10 µ $_0$, and the calculated relative error signal is less than 0.1%.

The locking conditions were simulated under different flux and voltage offset conditions. In typical circumstances, the response of the input flux dV_{SQUID}/d_{in} near the SQUID locking point must have the opposite polarity as the room-temperature amplifier gain to ensure that the SQUID locking point is maintained, as shown in Figures 4(a). In the event that the polarity of the room-temperature amplifier gain is identical to that of the SQUID response, a locking point offset phenomenon is observed, as illustrated in Figure 4 Figure 4: see original paper. To verify the independence of the FLL circuit from the shape of the SQUID V- response curve, as discussed in Section II.A, we simulate flux locking for different shapes of the SQUID V- curve, as shown in Figure 5 [Figure 5: see original paper].

B. Bandwidth and Slew Rate of Digital SQUID-FLL System

When designing a SQUID-FLL circuit, it is essential to consider rational design of the system bandwidth, particularly in multiplexing experiments. An FLL with small bandwidth may result in distortion of the TES signal, whereas larger bandwidth could introduce additional high-frequency noise, which would in turn affect the energy resolution of the TES. The effect of different feedback capacitors C_2 (integral component) and different shapes of V- transfer curves on bandwidth was simulated, with results shown in Figure 6 [Figure 6: see original paper]. In Figure 6, we consider the ideal case without accounting for digital circuit delays (t_{set} = 0), analogous to analog FLL. All SQUID V- curves have the same conversion coefficient dV_{SQUID}/d _{in} at the locking point and linear dynamic input range. The PID feedback is a time-domain simulation. By comparing it with the frequency-domain transfer function of the system, the correctness of the SQUID-FLL models can be verified. Based on the frequency-domain transfer function [17], the theoretical 3 dB system bandwidth can be obtained:

$$f_c = \frac{V_\phi G_1 M_{fb}}{2\pi R_1 C_2 R_{fb}}$$

where V_ = dV_{SQUID}/d _{in} denotes the conversion coefficient at the locking point. For example, when $C_2 = 2$ nF, the calculated value for the critical frequency f_c based on Equation 4 is 628 kHz, which is in accordance with the results of different V- transfer models displayed in Figure 6. From Equation 4, it can be observed that a multitude of factors influence bandwidth, all of which are linearly correlated. In room-temperature circuit design, the bandwidth can be determined by adjusting the preamplifier gain G_1, input resistance R_1, feedback capacitance C_2, and feedback resistance R_{fb}. It is crucial to acknowledge that G_1 represents an ideal linear gain in the simulation. In an actual design, the limitations of the operational amplifier' s gain bandwidth product (GBP) must be considered; therefore, this gain should not be excessively large for a system with large bandwidth. Furthermore, in practical design, system delays also reduce bandwidth, necessitating minimization of cable lengths.

If system delay is considered (t_{set} $\neq$ 0), the system bandwidth should satisfy Equation 5, with simulation results shown in Figure 7 [Figure 7: see original paper], where t_{sp} is the ADC sampling period, N_{sp} is the number of samples, and t_{fm} is the frame period.

$$f_c = \frac{V_\phi G_1 M_{fb} N_{sp} t_{sp}}{2\pi R_1 C_2 R_{fb} t_{fm}}$$

Further investigation was conducted on the system slew rate _{fb}/ t. When bandwidth is sufficiently large but slew rate is too small, signal distortion can also occur. The system slew rate is determined jointly by the bandwidth, the input range _{lin} of the SQUID' s open-loop linear gain, and the design of the FLL integral parameter, and is independent of frequency [18]. This relationship can be expressed as follows:

$$\frac{\partial \phi_{fb}}{\partial t} = \frac{\phi_{lin} N_{sp} t_{sp}}{2R_1 C_2 t_{fm}}$$

In our SQUID transmission model, _{lin} 0.3 $_0$, as shown at the top of Figure 6. Based on Equation 6, we calculated _{fb}/ t 1.5 $_0$/μs. The simulated result (t_{set} = 0) was approximately 1.5 $_0$/μs, as shown in Figure 8 [Figure 8: see original paper]. When the signal rise time exceeds 1.6 μs, the FLL is unable to accurately track the signal, resulting in distortion. It can be seen that when the SQUID transfer model is different, the shape of the tracked signal varies when distortion appears, but the value of the slew rate remains the same. All signals are distorted at rise times less than 1.6 μs, which is independent of the shape of the SQUID transfer model. For digital FLL, the slew rate also affects the signal-to-noise ratio (SNR). The noise spectral density S(f) of ADC or DAC should satisfy Equation 7:

$$S(f) = \frac{q}{\sqrt{12 \cdot \mathrm{BW}}}$$

where q is the least significant bit (LSB) voltage of ADC or DAC and BW is the Nyquist bandwidth of the system. We can calculate the equivalent current noise density S_I(f) corresponding to the input coil of SQUID according to Equation 8:

$$S_I(f) = \frac{S(f)}{G_1 V_\phi M_{in}}$$

For example, the equivalent current noise of a 16-bit ADC with 2 V full-scale range is 0.8 pA/√Hz referred to the input coil of SQUID, which is far less than the noise of TES (generally several tens to hundreds of pA/√Hz). The equivalent noise of a 16-bit DAC is 0.6 pA/√Hz when the feedback resistor is 10 kΩ as shown in Table 1. Thus, it is better to choose a large feedback resistor and high-resolution ADC and DAC for digital FLL.

The slew rate decreases when the frame frequency is reduced, as shown in Figure 9 [Figure 9: see original paper]. In theory, to track a faster signal, one can adjust the integration parameters, feedback resistance, and so forth to modify the bandwidth. According to Equations 5 and 6, the ideal linear relationship between slew rate and bandwidth is shown in Figure 10 [Figure 10: see original paper].

C. Noise Contribution in Digital FLL System

The TES detector achieves high energy resolution mainly due to its small thermal noise at low temperatures. In experiments, the noise primarily comprises TES Johnson noise and thermal fluctuation noise (TFN) [24]. The thermal noise of SQUID and the voltage noise of the preamplifier mainly constitute the system' s high-frequency noise. For digital FLL circuits, the quantization noise of the ADC and DAC devices contributes to the overall noise budget.

D. X-ray Pulse Signal Response

Considering that TES used for X-ray detection has a fast response time on the order of a few microseconds to several hundred microseconds, we used a pulse signal comprising white noise as input to simulate the response process of X-ray TES. If the Nyquist noise bandwidth is 1 MHz, the noise of the TES system was set to 50 pA/√Hz at 1 kHz with an RMS value of 22 µA (referred to the SQUID input coil), based on our testing results [25]. We used the sinusoidal-like SQUID-FLL model to demonstrate effective tracking of pulses with varying rise times, as illustrated in Figure 11 Figure 11: see original paper. Furthermore, a simulation was performed in which the rise time was set at 4.3 µs while the pulse amplitude was increased, with results shown in Figure 11(b). Distortion occurs when the signal amplitude exceeds 7.8 $_0$. The corresponding slew rate is approximately 1.45 $_0$/µs, which is consistent with the simulation results shown on the right side of Figure 8.

IV. CONCLUSION

A comprehensive behavioral simulation of the SQUID-FLL circuit was performed using different SQUID models in conjunction with the principles of digital PID magnetic flux feedback. We demonstrate that FLL design does not depend on the shape of the SQUID V- response by simulating SQUID transfer function models with three different shapes. A comprehensive list of parameters that must be considered when designing the SQUID-FLL system is presented in Table 1. Common scenarios of locking point adjustments during laboratory tuning were analyzed. The primary factors influencing the design of the system bandwidth f_c were examined, thereby providing valuable references for the design of SQUIDs and room-temperature readout electronics. Finally, the upper limit of the system slew rate was thoroughly analyzed and found to be approximately 1.5 $_0$/µs under default parameters in our model. The tracking capability of the system was validated with simulated X-ray pulse signals with different rise times (4.4 to 281 μs) and amplitudes (6 to 8 $_{0}$). We hope that these simulation results will serve as a reference for the design of high-performance digital PID flux feedback electronic and multiplexing readout systems.

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Note: Figure translations are in progress. See original paper for figures.