

Design of a ZYNQ-Based Beam Signal Data Acquisition System for the CiADS Room-Temperature Front-End Accelerator

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Abstract

The room-temperature front-end accelerator serves as the beam injector for the CiADS (China Initiative Accelerator Driven System) superconducting linear accelerator. During beam commissioning, the low-energy beam experiences the most pronounced space charge effects and RF non-linearities; consequently, the beam quality of the room-temperature front-end accelerator directly impacts the overall performance of CiADS. This paper describes a real-time acquisition and display system for room-temperature front-end beam signal data, implemented on a ZYNQ embedded platform. The platform acquires beam data converted by various beam signal detectors in real time via an external ADC acquisition board, while simultaneously performing online processing and network upload of the acquired data through the ZYNQ embedded platform. The data upload functionality is realized by porting the EPICS network transmission IOC software to the embedded operating system. Field application tests demonstrate that the system successfully acquires beam signal data from the room-temperature front-end and provides graphical display through a host computer interface, along with transmission of control parameters for internal and external trigger modes. The entire system exhibits high functional integration and ensures real-time, accurate data acquisition, providing crucial data support and technical assurance for subsequent beam physics experiments and beam diagnostics.

Full Text

Design of Beam Signal Data Acquisition System for the CiADS Room-Temperature Front-End Accelerator Based on ZYNQ

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Abstract: The room-temperature front-end accelerator serves as the beam injector for the CiADS (China Initiative Accelerator Driven System) superconducting linear accelerator. During beam commissioning, the low-energy beam experiences the most significant space charge effects and high-frequency nonlinearities, making the beam quality of the room-temperature front-end accelerator a critical determinant of overall CiADS performance. This paper presents a real-time beam signal data acquisition and display system based on the ZYNQ embedded platform. The platform captures beam data from various detectors in real time through an external ADC acquisition board, while simultaneously performing online processing and network transmission of the acquired data via the ZYNQ embedded platform. Data upload functionality is implemented by porting the EPICS network transmission IOC software into the embedded operating system. Field application tests demonstrate that the system correctly acquires beam signal data from the room-temperature front-end, provides graphical display through a host computer interface, and supports control parameters for both internal and external trigger modes. The integrated system offers real-time, accurate data acquisition and provides essential data support and technical assurance for subsequent beam physics experiments and diagnostics.

Keywords: Beam diagnostics; ZYNQ; Data acquisition system; EPICS

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CiADS aims to construct an Accelerator Driven Sub-critical System (ADS) facility for transmutation research, enabling scientific investigations into the stable, reliable, and long-term operation of superconducting linear accelerators, high-power spallation targets, and sub-critical reactor systems [1,2]. Large-scale accelerators require beam parameter acquisition and analysis during construction and commissioning. As the low-energy beam injector test platform for CiADS, the room-temperature front-end accelerator is essential for conducting beam pre-acceleration, control, and diagnostics experiments. The front-end test platform has completed overall construction and beam loading tests, comprising an Electron Cyclotron Resonance (ECR) ion source [3], Low Energy Beam

Transport line (LEBT), Radio Frequency Quadrupole (RFQ) accelerator, and Medium Energy Beam Transport line (MEBT) [4]. Multiple beam signal detectors installed throughout the front-end enable real-time beam observation, with data acquisition and analysis from these detectors providing critical support for both machine operational safety and beam physics research. This design focuses on acquiring, transmitting, and displaying beam intensity signals converted by beam signal detectors.

[Figure 1: see original paper] Design diagram of the room-temperature front-end accelerator

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2.1 Hardware Equipment

Beam signals include beam position, beam profile, and beam intensity. Beam intensity is a crucial parameter for verifying ion beam stability. The room-temperature front-end accelerator employs two types of beam intensity detectors: DC Current Transformers (DCCT) and AC Current Transformers (ACCT), both consisting of a current transformer (CT) probe head and front-end electronics. DCCT measures the DC component of the beam, while ACCT measures the AC component. Both detector types are manufactured by Bergoz. The front-end is equipped with one DCCT probe and two ACCT probes installed in the LEBT and MEBT sections to collect raw beam intensity information.

[Figure 2: see original paper] DCCT probe head and front-end electronics: (a) DCCT probe head, (b) Front panel of electronics, (c) Rear panel of electronics

The DCCT probe head is installed in the LEBT section of the room-temperature front-end accelerator. Figure (a) shows the DCCT probe head installed between solenoid magnets, while figures (b) and (c) display the front and rear panels of the accompanying electronics. The rear panel features a DB9 control connector (adjustable gain amplifier) for controlling the DCCT input signal range, enabling operators to measure signals across different scales.

The two ACCT probe heads are installed on opposite sides of the RFQ. As shown in Figure 3 [Figure 3: see original paper], the LEBT section uses a vacuum-type ACCT because the region before the RFQ requires a strict vacuum environment to avoid collisions with gas molecules and minimize energy loss. After the

RFQ, where beam energy has significantly increased and vacuum requirements are less stringent, a flange-type ACCT is selected for easier installation and maintenance.

[Figure 3: see original paper] ACCT probe head and front-end electronics

2.2.1 DCCT Principle

The DCCT is essentially a zero-flux transformer. As illustrated in Figure 4 [Figure 4: see original paper], the detector consists of two magnetic rings with identical dimensions and magnetic properties, wound with three types of coils. The excitation (modulation) coils are connected in series on both rings with equal turns per ring. A low-frequency oscillation signal from a crystal oscillator excites the two magnetic rings in opposite directions, driving them to saturation [5,6]. Without beam current, the excitation coils on both rings carry equal currents in opposite directions, generating equal and opposite magnetic fields, maintaining the detector in a zero-flux state with no compensation current and no output signal from the sensing coil. With beam current present, the sum of magnetic fields from excitation coils and beam current becomes non-zero. The synchronous demodulator then integrates and amplifies the second harmonic component of the excitation signal, feeding it into a feedback coil that generates compensating flux to offset the beam-generated flux, establishing a new zero-flux state. The average beam current can be calculated by measuring the current in the feedback coil [7-9].

[Figure 4: see original paper] DCCT probe head and signal processing electronics

2.2.2 ACCT Principle

ACCT operates based on electromagnetic induction law. The detector comprises a ferrite core encapsulated in a toroidal copper housing with wound coils. The beam passing through the core's circular aperture acts as the primary coil, while the secondary coil is wound on the core. When beam signals pass through the detector, the generated magnetic field couples through the toroidal core, inducing signals in the secondary coil. The measured current value is obtained based on the turns ratio [10].

[Figure 5: see original paper] Schematic diagram of simplified ACCT probe structure

3 Overall System Architecture Design

The data acquisition system architecture comprises three main components: data acquisition, data transmission, and data display. The acquisition component uses analog signal acquisition boards to collect beam data processed by CT detector front-end electronics. The transmission component transfers data from the PL side to the PS side via the AXI bus using DMA, where EPICS PV

variables are assembled and published over the network. The display component receives PV variable arrays from the PS-side IOC through host computer display controls, visualizing beam information via Phoebus-CSS software. The overall system structure is shown in Figure 6 [Figure 6: see original paper].

[Figure 6: see original paper] Block diagram of the data acquisition system structure

As shown in Figure 6, raw signals collected by DCCT and ACCT probes in the LEBT and MEBT sections are amplified, filtered, and converted through IV conversion by the front-end electronics system into standard -10V to 10V signals for the data acquisition chassis. The IV module is provided by the beam diagnostics detector team [11]. For room-temperature front-end beam signal acquisition, the AD7606C-18 board is employed, offering higher input range, more channels, and greater resolution. For other acquisition scenarios requiring high speed and low power, such as magnetic field strength measurement, SAR-type AD7960BCPZ is typically used. The high-speed ADC acquisition board and ZYNQ are connected via FMC (FPGA Mezzanine Card) connectors. Programming the PL and PS sides of the ZYNQ SOC in the data acquisition chassis enables beam signal acquisition and network publishing, with final display on the human-machine interface.

4 Hardware Electronics

The ZYNQ SOC consists of PL (Programmable Logic) and PS (Processing System) components. The PL is the FPGA portion providing programmable logic, while the PS is an embedded CPU capable of running Linux. PL and PS communicate and exchange commands through multiple AXI buses [12]. The hardware electronics design assigns data acquisition and trigger mode selection to the PL side, while the PS side handles command issuance and embedded system operation. The embedded system runs EPICS IOC software that transmits data to the control network for host computer acquisition and visualization [13,14]. The ZYNQ hardware system functional structure is shown in Figure 7 [Figure 7: see original paper].

[Figure 7: see original paper] Block diagram of the ZYNQ hardware system

The PL side encapsulates data acquisition and trigger mode selection modules through custom IP cores. The PS side sends commands to these modules and the AXI-DMA IP core via the AXI-Lite interface. When the PL-side data acquisition module receives a start command and specified acquisition length, it immediately controls the ADC operation while sending acquired data to the AXI-DMA IP core's S2MM port, which transfers the data through the AXI SmartConnect IP core to DDR on the PS side [15].

4.1.1 Data Acquisition Module The PL-side data acquisition module primarily issues control commands to the external AD7606C-18 and reads data

from eight channels after analog-to-digital conversion. The AD7606C-18 operates in bipolar single-ended input and parallel output mode for multi-detector data acquisition. As shown in the parallel mode timing diagram in Figure 8 [Figure 8: see original paper], the FPGA generates a CONVST rising edge signal to initiate sequential reading of all eight channels, during which BUSY goes high and falls after sampling completion. Users can read acquisition data when both CS and RD signals are low after BUSY falls [16].

[Figure 8: see original paper] AD7606C-18 parallel mode timing diagram

In the VIVADO implementation, a state machine sequentially reads the eight channel data. According to the timing diagram in Figure 8, two parallel frames are required to read each channel's data. As shown in Figure 9 [Figure 9: see original paper], taking Channel 1 as an example, data is read in two states: READ_{CH1} and READ_{CHIS}. The READ_{CH1} state reads the first ADC data frame (bits 2 to 17, MSB), while the READ_{CHIS} state reads the second frame (bits 1 and 0, LSB).

[Figure 9: see original paper] Reading Channel 1 data in the state machine

4.1.2 Trigger Mode Selection Module A chopper in the room-temperature front-end accelerator generates microsecond-scale time-structured beam bunches for component calibration. To enable researchers to precisely observe beam signals, the data acquisition system incorporates a trigger mode selection module for choosing between internal and external trigger modes. In external trigger mode, the system can receive external synchronization signals to enable simultaneous acquisition from different beamline sections.

[Figure 10: see original paper] Program flowchart of the trigger mode selection module

The PL-side trigger mode selection module flowchart is shown in Figure 10 [Figure 10: see original paper]. Before acquisition begins, the PS-side application issues a trigger start command and specifies the trigger mode. In the room-temperature front-end accelerator, Faraday Cup (FC) signals in LEBT and DCCT detector signals use internal trigger mode, while ACCT detectors on both sides of the RFQ and FC signals in MEBT employ external trigger mode for synchronized acquisition and diagnostics of different beam bunch signals.

4.2.1 System Development and Driver Porting The PS-side responsibilities include system customization and porting, DMA driver development, and IOC program design. The complete system image and related files are stored on the chassis SD card, from which the Ubuntu system automatically boots when power is applied. System customization and porting utilize Xilinx's Petalinux tool. After configuring the PL side in VIVADO, Petalinux generates the kernel, device tree, and root filesystem based on the hdf file. The device tree file enables kernel recognition of the DMA driver and completes DMA initialization and parameter configuration. Applications in the root filesystem call the DMA

driver to transfer acquired data to DDR. Figure 11 [Figure 11: see original paper] illustrates the application process of calling the DMA driver to complete data transmission.

[Figure 11: see original paper] DMA transfer function call process

4.2.2 EPICS Embedded System Design Data transmission to the host computer is based on the EPICS system architecture, enabling any EPICS-equipped device on the control network to access beam data. The data acquisition system's EPICS IOC program extracts data from DDR, packages it into PV variable arrays, and transmits them over Ethernet to the control network, where any OPI interface can directly access the PV variables. The EPICS software architecture is shown in Figure 12 [Figure 12: see original paper].

[Figure 12: see original paper] EPICS software architecture

5.1 System Interface

The control system interface serves as the human-machine interface and the “eyes” of physics experimenters. All low-level programs in the room-temperature front-end accelerator control system run on dedicated front-end servers, while upper-layer applications, particularly control interfaces, operate on central control room computers. Interface design must meet physics experiment requirements to maximize assistance for operators and experimenters in observing and analyzing experimental phenomena.

The data acquisition system's OPI program is developed using Phoebus-CSS software, which can retrieve PV variable arrays published by EPICS IOC from the local network. As shown in Figure 13 [Figure 13: see original paper], the host computer interface incorporates multiple graphical controls to assist physics researchers in debugging and analysis. Researchers can issue different commands to low-level hardware devices through graphical controls on the control interface to better observe beam information from the room-temperature front-end accelerator.

5.2 System Function Testing

[Figure 13: see original paper] Host computer system interface

The complete system has undergone both signal source simulation testing and on-site testing. Simulation tests used a signal generator to output $\pm 10V$, 5kHz and $\pm 10V$, 10kHz sine wave signals to the first channel of the data acquisition chassis. After connecting the serial debugging tool, powering on the system, mounting the DMA driver, and running the application, internal trigger mode was employed with a DMA transfer length of 128. Data was observed using VIVADO's ILA integrated logic analyzer via JTAG and the serial debugging tool. As shown in Figure 14 [Figure 14: see original paper], VIVADO's ILA correctly displayed the waveforms from the signal generator while the PS side

successfully received and displayed data from the PL side, confirming proper data acquisition and transmission.

[Figure 14: see original paper] Signal generator simulation results

On-site testing involved extracting a 20 keV continuous beam from the ECR ion source, which after matching and transport through LEBT was chopped by a chopper into 50 ns narrow pulse signals. These pulses entered the downstream RFQ cavity for acceleration to 2.1 MeV before entering MEBT. Outputs from the three CT detector front-end electronics in the room-temperature front-end were connected to the data acquisition chassis, with beam intensity information observed through the central control room's host computer interface.

[Figure 15: see original paper] Comparison of on-site test results

As shown in Figure 15 [Figure 15: see original paper], the upper portion displays oscilloscope measurements directly connected to CT front-end electronics outputs, while the lower portion shows the data acquisition chassis system interface. When beam passes through the DCCT detector, the host computer interface accurately displays the DC signal from the LEBT DCCT detector. When beam passes through ACCT detectors with the host computer set to external trigger mode, the interface completely displays pulse beam waveforms from both LEBT and MEBT ACCTs. Results demonstrate simultaneous three-channel data acquisition and successful data publication, with display results consistent with on-site oscilloscope measurements, meeting operational requirements.

Conclusion

The room-temperature front-end beam signal data acquisition system employs a ZYNQ platform with external ADC boards to achieve multi-detector data acquisition and network transmission. Through PL-side logic programming and PS-side embedded software design on the ZYNQ SOC, the system realizes synchronized acquisition, upload, and online display of beam signals from different beamline sections. The complete system has been deployed on-site, operating stably and reliably, providing strong technical support for room-temperature front-end beam quality optimization studies. As accelerator technology advances, the data acquisition system can incorporate higher-precision ADC boards to meet requirements for higher-frequency beam signals, while digital filtering algorithms and automatic calibration techniques can be added to the data processing section to enhance automated noise floor data processing capabilities, further improving system data acquisition and processing performance.

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