Pre-trigger Method for DRS4 Evaluation Board in Nuclear Detection Timing Measurement

Authors: He Zirui, Kuang Peng, Yu Xiaotian, Zhang Peng, Zhang Hongqiang, Wang Yingjie, Liu Fuyan, Wang Baoyi, Shan Jian, Cao Xingzhong, Liu Fuyan

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Abstract

The DRS4 (Domino Ring Sampler 4) chip based on Switched Capacitor Array (SCA) technology has become an important method for improving time measurement precision, due to its high sampling rate, high integration density, and low power consumption, particularly its capability for multi-channel high-precision time measurement. This paper proposes a pre-trigger selection method for effective events to address the main cause of low data processing efficiency in the dual-detector channel nuclear detection coincidence time measurement system based on the DRS4 evaluation board. By screening effective events in the DRS4 acquisition circuit, this method ensures efficient utilization of core signal processing resources. Measurements show that the coincidence counting rate of the DRS4 time measurement system based on the new trigger method can reach the processing limit of the DRS4 evaluation board, with a coincidence counting rate of 376 cps (Counts Per Second).

Full Text

Preamble

Research on pre-trigger Technique for DRS4 evaluation board in nuclear detection time measurement

HE Zirui1,2, KUANG Peng2,3, YU Xiaotian2,3, ZHANG Peng2,3, ZHANG Hongqiang2,3, WANG Yingjie2,3, LIU Fuyan2,3, WANG Baoyi2,3, SHAN Jian1, CAO Xingzhong2,3

1School of Electrical Engineering, University of South China, Hengyang 421001, China
2Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China

3Center for High Energy Physics, Henan Academy of Sciences, Zhengzhou 450046, China

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First author: He Zirui, male, born in 1999, graduated from Hunan City University in 2021, master student. His research field is positron annihilation spectroscopy.

Corresponding authors: LIU Fuyan, E-mail: liufy@ihep.ac.cn; SHAN Jian, E-mail: Shanj0666@163.com

Abstract

[Background]: The DRS4 (Domino Ring Sampler 4) chip, based on the Switched Capacitor Array (SCA) technology, has become an important method for enhancing the precision of time measurement due to its high sampling rate, high integration, and low power consumption. Particularly, is capable of achieving high-precision time measurement across multiple channels. [Purpose]: This study establishes a dual-channel nuclear signal coincidence time measurement system utilizing the DRS4 evaluation board, systematically investigates the key factors contributing to the low data processing efficiency of the system, and implements enhancements to the time measurement system. [Methods]: To address the issue of low data processing efficiency, an effective event pre-trigger selection method is introduced during the experiment. This method filters the valid events within the DRS4 acquisition circuit to ensure the efficient utilization of the circuit's core signal processing resources. [Results]: The redundant triggering of non-effective events within the evaluation board and the low-speed data transmission circuit are identified as the primary culprits for the reduced efficiency of the spectrometer system. The DRS4 time measurement system, equipped with the novel trigger method, has achieved a coincidence counting rate that reaches the processing threshold of the DRS4 evaluation board, with a rate of 376 cps (Counts Per Second). [Conclusion]: The adoption of the effective event pre-selection method has significantly enhanced the performance of the nuclear signal time measurement system based on the DRS4 evaluation board, offering a viable solution for the trigger logic selection in multi-channel nuclear signal time measurement systems.

Keywords: Time measurement, DRS4, Trigger selection, Coincidence count rate

Introduction

Waveform digitization technology serves as a critical electronic technique for front-end signal readout in nuclear physics experimental apparatus. By acquiring the initial signal waveforms output by detectors, it enables extraction of all physical information carried by the signals, including timing and amplitude

information [1,2,3]. Among these, high-precision time measurement is particularly crucial for obtaining physical information [4,5]. Digital waveform sampling technology can achieve higher-precision time measurement [5-8] and primarily follows two technical routes: waveform sampling based on fast analog-to-digital converters (FADC) and waveform sampling based on switched capacitor arrays (SCA). Traditional waveform digitization methods rely on high-speed analog-to-digital converters (FADC). However, as channel counts increase in large-scale nuclear and particle physics experiments, FADCs face limitations in power consumption, cost, and integration level, making them unsuitable for experiments requiring numerous channels [9]. The emerging switched capacitor array (SCA) waveform sampling technology, which operates by high-speed analog sampling and storage followed by digitization using appropriately-speed ADCs (Analog-to-Digital Converters), resolves the contradiction between high sampling rates and high-precision analog-to-digital conversion inherent in FADCs [10]. SCA chips inherently feature low power consumption and avoid the need for high-speed ADCs, thereby reducing overall system power consumption. With its low power consumption, low cost, and high channel density per chip, SCA-based waveform sampling technology has become an ideal alternative to high-speed FADC sampling [11].

The SCA+ADC technical approach has gradually gained widespread attention and has been adopted in detector readout systems for several major physics experiments. The Swiss MEG (MuE-Gamma) experiment utilized DRS (Domino Ring Sampler) chips and various waveform processing techniques to digitize, shape, filter, and integrate waveforms from different detectors such as calorimeter PMTs, achieving high-precision time and energy measurements [12]. The Mediterranean astrophysics ANTARES experiment employed ARS1 (Analogue Ring Sampler 1) chips to read out and digitize photomultiplier signals, enabling high-precision time measurement, light yield measurement, and pulse shape discrimination to facilitate neutrino event reconstruction and determine neutrino direction and energy [13].

In recent years, domestic applications of SCA-based waveform sampling technology have primarily employed the DRS4 chip produced by PSI [14]. The DRS4 chip represents a prominent implementation of SCA-based waveform sampling technology, offering a maximum sampling rate of 5 GS/s, an analog input bandwidth of 950 MHz, and extremely low power consumption, making it well-suited for high-speed sampling of laboratory analog signals [15]. However, it has one significant drawback: it cannot sample during data readout, resulting in substantial dead time [16]. This limitation restricts DRS4 chips primarily to waveform sampling systems with low count rates and high time resolution. In time measurement systems built with DRS4 evaluation boards, researchers have typically focused on timing methods for waveform reconstruction, interpolation algorithms, and digital pulse processing, while paying insufficient attention to systematic investigation of the performance limitations caused by redundant triggering and transmission circuit designs that lead to low data processing efficiency. This paper establishes a time measurement system based on the DRS4

evaluation board and conducts systematic experimental analysis of the primary factors causing its low data processing efficiency. To address this issue, an effective event pre-selection method is proposed and implemented experimentally.

1 Experimental Methods

The experimental system consists of two BaF2 detectors (BaF2 crystal dimensions of Φ30 mm × 20 mm, photomultiplier tube model Hamamatsu R3377), a high voltage power supply (HV), a DRS4 evaluation board, and a host computer. The electronic schematic diagram of the experiment is shown in Figure 1 [Figure 1: see original paper].

The anode signals from detectors A and B are fed into channels Ch1 and Ch2 of the DRS4 evaluation board, respectively. These two signals are processed by the DRS4 evaluation board and converted into a series of binary data transmitted via data cable to the host computer. In the host computer software, the signals from both detectors undergo algorithmic reconstruction and amplitude analysis to identify the start signal (1.28 MeV γ photon) and stop signal (0.511 MeV γ photon). Constant fraction timing is then applied, and the time difference between signals is calculated. After collecting and analyzing sufficient time difference data, the positron annihilation lifetime spectrum of the measured sample is obtained.

[Figure 1: see original paper]

The DRS4 chip serves as the core component of the aforementioned system, where detector signals sequentially undergo trigger discrimination, sampling digitization, and data transmission. The internal logic circuit schematic of the evaluation board is shown in Figure 2 [Figure 2: see original paper]. Signals are compared against reference levels provided by a DAC module via comparators. The compared signals then enter the FPGA, where logical judgment generates trigger signals. The FPGA controls the DRS4 to stop sampling by generating trigger signals and reads out the sampling cells to the ADC for digitization at a frequency of 33 MHz. During this readout process, the DRS4 cannot perform sampling, resulting in dead time. The digitized data is transmitted to the FPGA for processing and then sent to the host computer via USB 2.0. The experiment employs a pair of pure iron (Fe) standard samples with a 22Na (14.4 Ci) source configured in a "sandwich" structure, aligned linearly with the two detectors. Using this nuclear detection time measurement system based on the DRS4 evaluation board, the measured count rate for lifetime spectroscopy is only 45 cps (Counts Per Second), significantly lower than that of conventional analog spectrometers under equivalent conditions (~300 cps). The low transmission efficiency of the DRS4 evaluation board in nuclear detection time measurement systems arises primarily from two factors. The first and foremost is the limitation of the DRS4 evaluation board's trigger logic design, which causes frequent redundant triggering during sampling and acquisition of substantial invalid data. The second is the limitation of the data transmission circuit design,

which restricts data transfer speed, allowing only a certain level of acquired data volume without achieving higher transmission rates. The combined effect of these factors results in the low transmission efficiency of the DRS4 evaluation board in time measurement systems.

[Figure 2: see original paper]

To ensure efficient transmission of core signals, this paper implements a front-end pre-trigger circuit before signals are fed into the DRS4 evaluation board. By filtering valid events within the DRS4 acquisition circuit, this approach ensures efficient utilization of core signal processing resources, as illustrated in Figure 3 [Figure 3: see original paper]. The pre-trigger discrimination circuit consists of a Constant Fraction Discriminator (CFDD) and a coincidence unit. The analog CFDD module discriminates both stop and start signals separately, generating two signals. When these two signals fall within a 100 ns coincidence window, the coincidence unit generates a trigger signal. Upon receiving this trigger signal, the DRS4 evaluation board begins sampling the anode signals.

[Figure 3: see original paper]

This study investigates the causes of low count rates in DRS4 evaluation board-based nuclear detection time measurement systems from two factors: transmission speed and trigger logic of the DRS4 evaluation board. A pre-trigger-based nuclear detection time measurement system using the DRS4 evaluation board has been constructed to achieve efficient utilization of core signal processing resources.

The measurement system was evaluated using a signal generator to produce two pulse signals with a specific delay. The DRS4 evaluation board's signal acquisition process involves two sequential stages: sampling and readout digitization. The period during which the DRS4 stops sampling and reads out sampling cells to the ADC for digitization is termed dead time. During this interval, subsequent signals cannot trigger DRS4 sampling, leading to signal loss and causing inconsistency between the signal frequency generated by the signal generator and the count rate measured by the system. As shown in Figure 4 [Figure 4: see original paper], when the signal frequency ranges from 2 Hz to 500 Hz, signals can effectively trigger DRS4 sampling, resulting in a linear relationship between signal frequency and system count rate. As the signal frequency increases from 500 Hz to 5000 Hz, the relationship becomes non-linear due to some signals being unable to trigger DRS4 sampling during dead time and limitations in the DRS4 evaluation board's signal processing capability. The system count rate saturates at 510 cps. These results demonstrate that the system count rate is limited by both the DRS4 evaluation board's signal processing capability and its dead time, with a maximum achievable count rate of 510 cps.

[Figure 4: see original paper]

2.2 Pre-trigger Based System Performance Evaluation

Using positron annihilation lifetime measurement as the test case, the experiment employs a pair of standard Fe samples with a 22Na source configured in a "sandwich" structure placed between two detectors. By measuring the number of positron annihilation events per unit time as the system's coincidence count rate, the effect of pre-triggering on the processing performance of the signal time measurement system is evaluated; the schematic diagram is shown in Figure 3. Figure 5 [Figure 5: see original paper] presents the measurement results of pre-trigger influence patterns. It can be observed that for the system without pre-triggering, the coincidence count rate reaches its limit and stabilizes at approximately 50 cps after the 22Na source strength increases to 5.21 Ci. In contrast, the coincidence count rate of the pre-trigger-based system increases significantly with source strength, achieving a maximum of 376 cps at a source strength of 24 Ci. Additionally, the disparity in coincidence count rates between the two systems becomes increasingly pronounced as source strength grows. Figure 6 [Figure 6: see original paper] shows the growth ratio after adding pre-triggering under the same source strength (data points represent the growth ratio with/without pre-triggering, dashed line indicates the trend). As shown in Figure 6, when source strength increases from 0.41 Ci to 10.9 Ci, the growth ratio of the system's coincidence count rate after adding pre-triggering rises rapidly, eventually stabilizing at approximately 7.5 times after the source strength reaches 10.9 Ci. In systems without pre-triggering, redundant signals trigger the DRS4 evaluation board during the sampling process, resulting in acquired data containing numerous invalid events. After filtering by the host computer, only a small fraction of valid events can be retained. Consequently, the coincidence count rate of systems without pre-triggering, affected by redundant signal false triggers, initially rises with increasing source strength, reaches a maximum at 5.21 Ci, and subsequently plateaus. For systems employing pre-triggering, most invalid event acquisitions can be effectively avoided, enhancing the DRS4 evaluation board's processing performance for valid events. Due to limitations in the DRS4 evaluation board's processing capability, there exists an upper limit to the number of signals that can be acquired per unit time. Unlike signals from a signal generator, nuclear signals exhibit randomness with non-uniform time intervals. Constrained by the DRS4 evaluation board's processing capability, the number of nuclear signals acquired per unit time by the pre-trigger-based system may be lower than that measured by systems without pre-triggering. At a source strength of 24 Ci, the pre-trigger-based system achieves maximum processing performance for nuclear signals, with a coincidence count rate of 376 cps. These results demonstrate that employing pre-triggering to filter valid events in the DRS4 evaluation board's acquisition circuit can effectively ensure efficient utilization of core signal processing resources.

[Figure 5: see original paper]

[Figure 6: see original paper]

3 Conclusion

This paper establishes a nuclear detection time measurement system based on DRS4. The processing efficiency of this measurement system is primarily constrained by the trigger logic limitations of the DRS4 evaluation board, leading to redundant triggering issues that result in low effective event count rates. To address the problem of low-efficiency transmission of core data by the DRS4 evaluation board, a pre-trigger method is proposed to filter valid events and avoid redundant triggering of invalid events in the DRS4 evaluation board, enabling the measurement system's count rate to reach the processing limit of the DRS4 evaluation board. Through the effective event pre-selection method, the performance of the DRS4-based nuclear detection time measurement system is significantly improved, providing a viable solution for trigger logic discrimination in multi-channel nuclear detection time measurement systems.

4 References

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Note: Figure translations are in progress. See original paper for figures.