A low-noise, high-count-rate front-end readout ASIC for APD detectors in STCF ECAL

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Date: 2024-09-05T00:00:00+00:00

Abstract

This study presents a low-noise, high-count-rate front-end readout Application-Specific Integrated Circuit (ASIC) designed for the Electromagnetic Calorimeter (ECAL) of the Super Tau-Charm Facility (STCF). To address the high background count rate challenge of the STCF ECAL, this paper analyzes the temporal characteristics of signals at various nodes in the analog front-end readout circuit signal chain, and accordingly optimizes the system design to mitigate pile-up effects and elevate the count rate to the megahertz level. First, a Charge Sensitive Amplifier (CSA) with a fast reset path is designed, enabling rapid reset when the output reaches maximum amplitude and preventing the CSA from entering dead time due to pile-up saturation. Second, an improved high-order filter shaper with a baseline holder circuit is designed to enhance pile-up immunity and noise filtering performance. Finally, a high-speed peak sample-and-hold circuit with asynchronous FIFO buffer functionality is proposed for sampling, holding, and reading the signals output from the filter shaper. The ASIC is designed and fabricated using a standard commercial 1P6M 0.18 m mixed-signal CMOS process, with a chip area of 2.4 mm × 1.6 mm. Test results demonstrate that its dynamic range is 4–500 fC, with a nonlinearity error below 1.5%. For periodically distributed input signals, with a peaking time set to 360 ns, the count rate can reach 1.5 MHz/Ch, and the Equivalent Noise Charge (ENC) is 2500 e^-. When the peaking time is set to 120 ns, the ASIC can achieve a maximum acceptable count rate of 4 MHz/Ch. At a peaking time of 1.68 s with an additional 270 pF capacitor at the input, the minimum ENC is 1966 e^-, and the noise slope is 3.08 e^-/pF. For input charge greater than 200 fC, the time resolution is better than 125 ps. The average power consumption of the chip is 35 mW/Ch.

Full Text

Preamble

This study presents a low-noise, high-rate front-end readout application-specific integrated circuit (ASIC) designed for the electromagnetic calorimeter (ECAL) of the Super Tau-Charm Facility (STCF). To address the high background-count rate in the STCF ECAL, the temporal features of signals are analyzed node-by-node along the chain of the analog front-end circuit, and the system is optimized to mitigate pile-up effects and elevate the count rate to megahertz levels. First, a charge-sensitive amplifier (CSA) with a fast reset path is developed, enabling quick resetting when the output reaches maximum amplitude. This prevents the CSA from entering a pulse-dead zone due to amplifier saturation caused by pile-up. Second, a high-order shaper with baseline holder circuits is improved to enhance anti-pile-up capability while maintaining effective noise-filtering performance. Third, a high-speed peak detection and hold circuit with an asynchronous first-input-first-output buffer function is proposed to hold and read the piled-up signals of the shaper. The ASIC is designed and manufactured using a standard commercial 1P6M 0.18 µm mixed-signal CMOS process with a chip area of 2.4 mm × 1.6 mm. Measurement results demonstrate a dynamic range of 4–500 fC with a nonlinearity error below 1.5%. For periodically distributed input signals, a count rate of 1.5 MHz/Ch is achieved with a peak time of 360 ns, resulting in an equivalent noise charge (ENC) of 2500 e^-. The maximum count rate is 4 MHz/Ch at a peak time of 120 ns. At a peak time of 1.68 µs with a 270 pF external capacitance, the minimum ENC is 1966 e^-, and the noise slope is 3.08 e^-/pF. The timing resolution is better than 125 ps at an input charge of 200 fC. The power consumption is 35 mW/Ch.

Keywords: Readout electronics, APD, Charge measurement, High count rate, STCF.

Introduction

The Super Tau-Charm Facility (STCF) represents an important advancement in accelerator-based particle physics following the Beijing Electron-Positron Collider II (BEPC-II) in China. It has been proposed for searching for new physics beyond the Standard Model (SM) in the tau-charm energy region with a luminosity higher than 0.5×10^{35} $cm^{-2}s^{-1}$ [**?**]. Compared to BEPC-II, the luminosity of the STCF experiment is 100 times higher, resulting in a proportional increase in the event rate of its physical processes. An electromagnetic calorimeter (ECAL), a critical component of STCF detectors, is utilized to measure the energy of particles with high efficiency and resolution. Based on related studies and simulation results, the physical-event rate incident on the STCF ECAL is expected to reach 400 kHz. Moreover, owing to the high luminosity and narrow beam design of STCFs, the estimation and suppression of background events have become critical issues.

The background events encountered by the STCF ECAL were studied using Monte Carlo simulations, and the results indicated that the background-count rate measured by the ECAL was as high as 1 MHz [**?**]. In response to the high count rates resulting from the ultrahigh luminosity of the STCF experiment, pure cesium iodide (pCsI) was chosen as the scintillation crystal for the ECAL because of its fast response and excellent radiation resistance. To compensate for the lower yield of pCsI, large-area avalanche photodiodes (APDs) with internal gains have been selected as photodetector devices for the ECAL [**?**, **?**]. The detection unit, composed of pCsI and the APD, cannot inherently distinguish between particles produced by background and those produced by targeted physical processes. Therefore, the count rate of the front-end readout circuit must account for background events.

A charge-sensitive amplifier (CSA) is the most accurate preamplifier structure for charge measurements and is particularly well-suited for calorimeters aiming for high-energy resolution \cite{5–14}. The structure of analog readout circuits based on the low-noise CSA is shown in Fig. 1 [Figure 1: see original paper], where the detectors and readout circuits are AC coupled. The accumulation of signals presents a significant challenge for analog front-end readout circuits operating at high event rates. The factors limiting the circuit count rate include the decay time (Td) of the detector output-pulse current, rise time (trise) and reset time (trst) of the CSA, type and peak time (PT) of the filtering shaper, storage depth and dead time of the peak detect and hold circuit (PDH), and sampling rate of the analog-to-digital converter (ADC). For a selected detector, the pulse-current signal decay time is determined; for example, the luminous decay time of the pCsI scintillator selected for the STCF ECAL is approximately 30 ns. Therefore, targeted optimization of the CSA, shaper, and PDH circuits is essential in the design of a high-rate analog front-end readout ASIC to reduce the probability and impact of pulse pile-up, thereby increasing the event throughput of the front-end readout circuit \cite{15–21}.

In our previous work, we developed two low-noise readout ASICs, SECALROC1 and SECALROC2, to achieve high-precision energy and time measurements [**?**, **?**]. These ASICs were optimized for a count rate of 400 kHz. However, the count rate of the front-end readout circuit must be further improved considering the background events.

In this study, we present SECALROC3, a low-noise and high-rate front-end readout ASIC specifically designed for the STCF ECAL. Leveraging the characteristics of signals that can be piled up to a certain extent, we devised a CSA with a fast reset path, a high-order shaper with a baseline holder circuit, and a high-speed PDH circuit with asynchronous first-input-first-output buffering capability. This circuit enables the detection of piled-up signals from the shaper output, ensuring accurate identification even in situations with moderately piled-up signals. The proposed ASIC minimizes the effect of piled-up signals and achieves a counting rate of several megahertz per channel.

The remainder of this paper is organized as follows. Section II details the

ASIC architecture and circuit design. Experimental results are presented and discussed in Section III. Finally, Section IV provides a summary of the study.

II. ASIC Architecture and Circuit Design

A block diagram of SECALROC3 is shown in Fig. 2 [Figure 2: see original paper]. The proposed ASIC comprises six readout channels, including two dummy channels, a bandgap reference, bias circuits, a multiplexer, a single-ended to differential drive buffer, and a time-triggered signal buffer. Each channel consists of a low-noise CSA, a saturation-detection circuit, a fast-reset control circuit, an energy branch for measuring the input charge, and a time branch for measuring the time of arrival (TOA). The energy branch includes a pole-zero cancellation circuit, a high-order shaper with a baseline holder (BLH) circuit, and a PDH circuit. A pole-zero cancellation circuit can eliminate the undershoot of the shaper output and decrease the signal width [**?**, **?**]. The BLH is used to stabilize the output baseline by establishing a low-frequency feedback loop for the shaping circuits without introducing extra noise or instabilities. The PDH circuit detects the peak value of the output signal and obtains a nearly flat-topped signal, which preserves the peak-amplitude information for longer duration, enabling the ADC to perform conversion with more relaxed timing requirements or perform multiple readings on the same input signal. The time branch consists of a fast shaper, discriminator, and level shifter. The fast shaper decreases the signal width and increases the count rate of the time channel [**?**, **?**]. A hysteresis comparator generates a pulse signal, and the output pulse leading edge indicates the TOA. The level shifter converts the 3.3 V pulse signal to 1.8 V to match the power supply of the time-to-digital converter [**?**].

A. Charge-sensitive amplifier with fast-reset circuit

To maximize coverage of the outer surface of the pCsI crystal and capture more fluorescence, the STCF ECAL uses APD detectors (S8664-1010, Hamamatsu, Japan) with a large sensitive area of 10 mm $\times$ 10 mm. However, this substantial sensitive area introduces challenges for the front-end readout circuit in terms of noise and speed-performance optimization because of its large detector capacitance (typically CD = 270 pF) and leakage current (typically ID = 10 nA). The equivalent noise charge (ENC) was calculated using Eq. (1). The ENC contributions due to current parallel, thermal, and flicker noises are expressed in (2), (3), and (4), respectively [**?**].

$$ENC_t = \sqrt{ENC_i^2 + ENC_w^2 + ENC_f^2} \tag{1}$$

$$ENC_i^2 = \left(\frac{2qI_D}{q^2}\right) \cdot N_s \tag{2}$$

$$ENC_w^2 = \frac{4kT\gamma}{g_{m0}} \cdot \frac{(C_D + C_f + C_P)^2}{t_p} \cdot N_w \tag{3}$$

$$ENC_f^2 = \frac{K_{1/f}}{C_{ox}WL} \cdot \frac{(C_D + C_f + C_P)^2}{t_p^2} \cdot N_f \tag{4}$$

where Rf is the feedback resistance of the CSA (implemented by an n-MOSFET working in the subthreshold region), ID is the leakage current of the APD, tp is the peaking time of the shaper, gm0 is the transconductance of the input transistor M0, W and L are the width and length of the input transistor M0, respectively, CD is the capacitance of the APD detector, Cf is the feedback capacitor of the CSA, and CP is the parasitic capacitance excluding CD at the CSA input node. The parasitic capacitance CP is proportional to W and L. γ and K1/f are the thermal and flicker noise coefficients, respectively. Ns, Nw, and Nf are constants for parameter n of the shaper. To mitigate the impact of large capacitance on the readout circuit, a high-gain, wide-bandwidth, low-noise, single-ended input split-leg cascade amplifier with dual common-gate stages is proposed [**?**, **?**]. The input NMOS is optimized to operate in the moderate-inversion region (between strong and weak inversion) with a gate length (L) of 1 µm, gate width (W) of 16 mm (20 µm × 800 fingers), and bias current of 8.2 mA to achieve a high transconductance (gm0 = 125 mS) for reduced thermal noise [**?**].

As input-current pulses accumulate charge on feedback capacitor Cf, the output voltage of the CSA gradually increases, eventually leading to saturation. To prevent amplifier saturation and provide a stable DC operating point, a reset block must be connected in parallel to the feedback capacitor Cf. Two basic techniques have been implemented to discharge the feedback capacitance: switch reset and continuous discharge [**?**, **?**]. The switch-reset technique discharges the feedback capacitor by periodically opening a switch. The disadvantages of this solution are sampled noise and charge injection from the switch transistor. Additionally, each reset of the CSA introduces a negative signal to the shaper, thereby increasing the dead time of the readout circuits. Although a resettable shaper structure can overcome this negative signal, it increases system complexity [**?**].

The continuous-discharge technique can be applied using a resistor (or equivalent circuit) parallel to Cf to achieve continuous discharge of accumulated charge [**?**]. The output waveform of the CSA in this mode is shown in Fig. 3 [Figure 3: see original paper]. The rise time trise is affected by two factors: Td and TGBP. The time constant TGBP depends on the gain-bandwidth product (GBP) of the core amplifier [**?**]. The feedback resistor (Rf) must be sufficiently

large to reduce ballistic deficit effects while minimizing its parallel noise impact. Typically, an MOS transistor operating in triode or saturation region serves as the feedback resistor. This compact solution may enable control of feedback resistance; however, nonlinear effects must be considered. The long decay-time constant (τf = Rf $\times$ Cf) of the preamplifier output signal imposes limitations on count rate due to pulse pile-ups. When the resistance value of Rf is reduced to decrease the CSA reset time trst (approximately 4τf), the impact of ballistic deficit and noise contribution from Rf becomes non-negligible, affecting overall circuit noise performance. Therefore, a compromise between noise and count rate is necessary in Rf design.

The energy distribution of background events for the STCF ECAL is predominantly concentrated in the low-energy region below 1 MeV [**?**]. The magnitude of these event pulses is comparable to the equivalent noise of the front-end readout circuit. Thus, the influence of these background events manifests as an increase in the CSA output baseline, and the readout circuit cannot effectively detect these events. The event rate for higher-energy background events ($\geq$ 10 MeV) is significantly reduced [**?**]. According to the energy distribution and average event rate (Poisson distribution) of background events, the probability that background events of different energies occur within a 700 ns signal waveform can be estimated. For a barrel ECAL, the probability of more than one event greater than a 10 MeV background event within a 700 ns waveform width is only approximately 0.6%. Therefore, we can assume that a physical event will have only one larger background signal piled up with it. As shown in Fig. 3 [Figure 3: see original paper], the output signals of the CSA can be piled up to a certain extent, thus the circuit-receivable event rate can be increased. In this design, we added a saturation-detection circuit and fast-reset circuit for the CSA. When the CSA output reaches a preset saturation level due to event pile-up, a fast reset is launched to prevent the circuit from entering dead time.

A block diagram of the proposed CSA is presented in Fig. 4a [Figure 4: see original paper]. The core amplifier comprises two output branches formed by two source followers. One output (EOUT) connects to the energy-measurement channel, while the other output (TOUT) connects to the time-measurement channel. The continuous-reset feedback resistor Rf is positioned between the input and EOUT, interfacing with the subsequent pole-zero cancellation circuit. The feedback resistor Rf, implemented using the NMOS transistor M1, has a resistance value controlled by voltage RESCSA, with an adjustable equivalent resistance ranging from approximately 0.3 MΩ to 60 MΩ. Under the condition Cf = 500 fF, the decay time required for the CSA to recover to the baseline ranges from approximately 0.6 µs to 120 µs.

The fast-reset feedback circuit is positioned between the input and TOUT to minimize its effect on the energy-channel signal. This circuit includes switch transistors M2 and M3, controlled by FRST and NFRST (inverted signal of FRST) signals, along with a current-limiting resistor Rsw. The M3 transistor suppresses clock feed-through and charge-injection effects induced by M2. The

resistor Rsw restricts reset current during the fast-reset process, ensuring CSA stability [**?**]. The saturation-detection circuit employs a hysteresis comparator that generates a corresponding pulse signal when the CSA output voltage exceeds a certain threshold (near the saturation level). The circuit for generating FRST is shown in Fig. 4b [Figure 4: see original paper], incorporating the FREN signal to control the operation of the fast-reset circuit. When FREN=1, the TR signal is buffered and fed into a monostable circuit, producing a fixed-width (40 ns) pulse signal FRST (as well as NFRST) and completing the fast reset of the CSA. The fast-reset circuit operates only when the CSA is piled up near its maximum, and any detected events during the fast-reset operation are discarded to guarantee circuit noise performance.

B. High-order shaper with baseline holder circuit

In high-count-rate applications, the theoretically optimal peak time often falls short of meeting count-rate requirements. In such scenarios, noise performance must be compromised with count rate by employing a small adjustable peak time. For example, in our study, the theoretically optimal peak time ranges from 0.51 µs to 2.58 µs (varying with detector-leakage current and noise contribution from feedback resistor Rf). However, to satisfy the count-rate requirement of 1.5 MHz, the maximum peak time is set to 204 ns (choosing a shaper order of n=6). In addition to reducing peak time, similar to CSA output signals, shaper output signals can also pile up to a certain extent. Thus, detection of piled-up signals offers a solution for meeting higher count-rate requirements.

As depicted in Fig. 5a [Figure 5: see original paper], the width of the shaper output signal twidth is defined as the time range encompassing 1% to 1% of the maximum signal amplitude. The rise time trise represents the time required for signal amplitude to increase from 1% to its peak, whereas the fall time tfall represents the time required for amplitude to decrease from its peak value to 1%. The rise and fall times primarily depend on peak time tp and shaper characteristics (such as the number of real or complex poles). The peak-time points of two signals are t1 and t2, respectively, and the time interval between them is denoted as tdelay.

Conventionally, readout circuits operate with tdelay $\geq$ twidth, as shown in Fig. 5a [Figure 5: see original paper]. When tdelay $<$ twidth, signal pile-up occurs. Two typical pile-up scenarios for shaper-output signals are illustrated in Fig. 5b and Fig. 5c [Figure 5: see original paper]. In both cases, the two input signals have equal charges (E1 = E2). t1 and t2 represent the peak time points when the two signals are input individually, while tpk1 and tpk2 are the peak time points for the piled-up signal. Signals can still be considered effective when they increase by only 1% compared to the ideal peak-voltage amplitude. As shown in Fig. 5b [Figure 5: see original paper], when tdelay $\geq$ tdelay,th2 tfall, the voltage amplitude of the piled-up signal at peak point tpk1 equals the ideal peak-voltage amplitude. Additionally, the voltage amplitude at peak point tpk2 increases by only 1% compared to the ideal peak-voltage amplitude because the

tailing part of the first signal does not overlap with the peak of the second signal; both signals are considered effective. As shown in Fig. 5c [Figure 5: see original paper], when tdelay > tdelay,th1 trise, the voltage amplitude at peak point tpk1 increases by only 1% compared with the ideal peak-voltage amplitude because the leading part of the second signal does not overlap with the peak of the first signal, and the first signal can still be considered effective. Note that when the two input signals have different charges, tdelay,th2 and tdelay,th1 change according to the E1/E2 ratio [**?**]. Event timestamps can be obtained from the time channel; thus, tdelay between each signal is available. According to this time information, pile-up rejection (PUR) can be applied effectively in the back-end data-processing program to accept undistorted amplitudes and reject distorted amplitudes.

As shown in Fig. 6 [Figure 6: see original paper], the ratios of twidth to tp and tdelay,th2 to tp at E1 = E2 are depicted for different shaper orders. The values of twidth/tp and tdelay,th2/tp decrease significantly as the order n of the shaper increases. However, for $n \geq 5$, the decreasing trend gradually slows, and improvement becomes insignificant. This illustrates that higher-order shaper circuits are more suitable for high-count-rate applications. However, considering noise performance, with a fixed shaper output-signal width of twidth = 667 ns corresponding to a count rate of 1.5 MHz (periodically distributed input signals), the thermal-noise coefficient Nw/tp exhibits a smaller value in the range $4 \leq n \leq 6$. The shot-noise coefficient Ns × tp gradually decreases after $n \geq 2$. Thus, selecting a sixth-order shaper achieves noise optimization while meeting high count-rate requirements. In this configuration, the ratio of signal width to peak time is approximately 3.28, and the ratio of time interval between input signals to peak time is approximately 1.8. For the count-rate requirement of 1.5 MHz, without considering shaper-output signal pile-up, the maximum peak time is only 200 ns. However, allowing for output signal pile-up, this shaper can extend the maximum peak time to 370 ns, thereby mitigating degradation of noise performance.

The proposed CR-$(RC)^6$ semi-Gaussian high-order shaper is shown in Fig. 7a [Figure 7: see original paper]. The shaper comprises a CR-RC filter, multiple feedback (MFB) filter, Sallen–Key (SK) filter, and an RC filter. The front-end readout circuit collects electrons, resulting in a positive output signal from the CSA that subsequently produces a negative output signal in the CR-RC circuit. To guarantee a positive output signal and broaden the output range (with baseline voltage established by the CSA and maintained at approximately 0.8 V), the second stage employs an MFB filter structure to convert the signal output into a positive format. The SK filter is chosen for the third stage because of its properties as an in-phase proportional amplifier and its capacity for gain adjustment. The amplifiers for the CR-RC and MFB filters employ a single-ended input-output cascade structure similar to the CSA core amplifier, and individual transistor sizes are carefully tailored to ensure that DC voltages of both the CSA and filters are nearly identical. Additionally, utilizing an amplifier with identical construction to supply bias voltage at the negative terminal of the

SK stage ensures that DC voltages at both ends of the SK amplifier are balanced, thereby guaranteeing that the final output baseline remains stable around 0.8 V. The peak time is adjustable in this design and ranges from 120 ns to 1680 ns. A pole-zero cancellation (PZC) circuit eliminates undershoot of the shaper output and increases event rate. The pole-zero cancellation resistor (M1) forms a DC path between the CSA and shaper. In the event of CSA output signal pile-up, a DC current IIN flowing through the resistor network of the shaper induces baseline drift in the output, impacting amplitude-detection accuracy of the readout system. To address this issue, a BLH circuit generates IF to compensate for IIN, thereby suppressing baseline drift [**?**]. Fig. 7b [Figure 7: see original paper] shows the transfer function of the BLH circuit during operation (excluding M1 and C1a). For effective signal frequencies, the gain is approximately 113.4 dB. For low-frequency signals (below 1 Hz), the gain is approximately 60.5 dB, representing a reduction of 52.9 dB in low-frequency loop gain by the BLH circuit.

C. Peak-detection and holding circuit

The shaper output signal connects to the PDH, which detects and holds the peak voltage. The choice and operation of the PDH influence count rate and relate to PUR operation. Traditionally, PDH output signal width consists of three parts: writing time twrite, reading time tread, and reset time trst,pdh. When only one PDH circuit is used, if a second signal with higher (or lower) amplitude occurs in the same channel during ADC readout, the first (or second) amplitude will be lost; therefore, at least two levels of storage depth are required for high-count-rate applications. Two different approaches are commonly used: resetting the PDH for a fixed time after peak detection, or keeping the PDH reset until the shaper output falls below a fixed threshold again. Both approaches risk losing events, especially piled-up signals from the shaper.

To enhance the event rate received by the PDH circuit, storage depth must be increased and dead time reduced. This study employs three strategies to minimize dead time. First, two PDH submodules increase storage depth. While one module operates during the writing interval, another operates during the reading interval, ensuring one module is always waiting for the signal and eliminating dead time introduced by reading time tread. Second, reset time trst,pdh is concealed within the shaper peak time, effectively eliminating dead time caused by trst,pdh. Finally, the trigger signal from the time channel is utilized as a control signal, creating an event-driven analog memory. In this configuration, the PDH circuit exhibits minimal dead time for each detectable signal.

The proposed high-speed PDH circuit based on these principles is illustrated in Fig. 8a [Figure 8: see original paper]. The circuit comprises two submodules, PDHA and PDHB, a control module, and a holding capacitor CH. The PDHA and PDHB submodules employ peak-detection and holding circuits with a two-phase (read and write) configuration [**?**]. A folded cascade amplifier with rail-to-rail input dynamic range is used in the PDH. The DC gain A0, DC common-

mode rejection ratio (CMRR), and common-mode output reference Vo,cm of the amplifier are optimized to improve accuracy of peak-height measurement [**?**, **?**]. PDHRST serves as an external reset signal, DIS represents the trigger signal from the time channel, and WA (WB), RA (RB), and RSTA (RSTB) denote the write, read, and reset signals for PDHA (PDHB), respectively. In addition, MODEL and SYN serve as mode-control signals. When MODEL=1, the PDHA and PDHB submodules collaborate, where the amplifier of PDHA serves as the write amplifier and the amplifier of PDHB functions as a buffer (read amplifier), forming a continuous peak-detection and holding circuit [**?**]. The reset signal in this mode is supplied externally by PDHRST, enabling observation of the entire peak-sampling and holding process. This configuration is instrumental in testing circuit functionality and precision. Experimental results indicate that the proposed PDH operates within an input-signal range of 10 mV to 2 V with a percentage error below 7% and nonlinearity error of less than 1%.

When MODEL=0, the PDHA and PDHB submodules operate alternately and are controlled by a reset signal that transitions between their states. The reset signal is determined by the SYN signal, which provides flexibility to select either an external input PDHRST (SYN=1) or the trigger signal DIS from the time channel (SYN=0). Simulation results for the high-speed PDH circuit with SYN=0 are shown in Fig. 8b [Figure 8: see original paper]. Each rising edge of the DIS signal corresponds to the arrival of an event, generating a control signal that triggers one submodule to enter the writing state (while the other enters the reading state). The submodule in the writing state has a 45 ns reset process, followed by completion of peak sampling and holding of the current event. Simultaneously, the submodule in the reading state reads out the held voltage from the previous event, and the duration of the reading state depends on when the next signal arrives—that is, the time interval between the two signals tdelay. The entire PDH circuit functions as an event-driven, first-in-first-out analog memory. If the input signal is detectable by the time channel, the PDH circuit can successfully capture and store the peak values of shaper output signals. In this mode, the PDH circuit can detect piled-up signals from the shaper output, reducing the time interval between input signals from 3.28tp to 1.8tp, resulting in an 82% increase in count rate.

III. Experimental Results

A prototype ASIC chip, SECALROC3, was designed using a standard 0.18 µm CMOS process. Fig. 9a [Figure 9: see original paper] presents a microphotograph of the fabricated ASIC. The chip size is 2.02 mm × 1.41 mm. Each channel has an area of 0.2 mm × 0.7 mm. The power consumption is approximately 35 mW/Ch with a power supply of 3.3 V. The chip-measurement setup is illustrated in Fig. 9b [Figure 9: see original paper]. ASIC performance is evaluated using electrical tests. Input charges (QIN) are generated by coupling step voltages to a capacitance (Cinj = 1 pF), and the capacitance value is calibrated using a high-precision LCR meter. An input capacitor (CIN) is placed

on the test board to simulate APD detector capacitance. The signal generator produces differential signals; the negative signal is connected to Cinj, and the positive signal is inverted by the oscilloscope as the trigger signal.

First, a staircase step voltage with ten steps is generated by the signal generator, adjusting time intervals (tdelay) between steps to simulate input signals of different frequencies and adjusting step amplitudes (Vstep) to simulate different input signals. We performed tests on shaper and PDH output waveforms as well as piled-up signals to validate proposed circuit functionality and verify chip capability to handle event rates. Second, differential square waves with a frequency of 10 kHz are generated to evaluate dynamic range, linearity, noise, and time performance of the ASIC. Measurements are performed at different step-voltage amplitudes, and shaper and PDH output signals are acquired using an oscilloscope. Data are collected more than 1000 times, and mean values are recorded and analyzed to indicate dynamic range and linearity. Noise voltage is characterized by measuring the RMS value of pedestal voltage at the shaper output. ENC is used to evaluate noise performance. The rise/fall times (10%–90%) of step-voltage signals are approximately 1 ns. The time difference between leading edges of the trigger and time signals from each channel is defined as the TOA. At various voltage amplitudes, over 1000 TOA measurements are recorded and analyzed using an oscilloscope. These measurements are fitted to a Gaussian-distribution curve and the standard deviation is used to assess time resolution.

The fast-reset functionality of the CSA is tested, as shown in Fig. 10a [Figure 10: see original paper]. To simulate CSA output signal pile-up, the control voltage for the feedback resistor is set to RESCSA = 2.0 V (resulting in a CSA output-signal fall time of approximately 10 μs). The input-signal frequency is set to 1 MHz with a peak time of 240 ns. Test results reveal that without the fast-reset function, as CSA signals pile up for the same input-charge signal, the shaper output signal (red) responds incorrectly and disappears quickly until the CSA piles up to its maximum, causing the circuit to enter a pulse dead zone. With the fast-reset function enabled, a reverse signal is observed in the shaper output (blue), indicating that a fast-reset process occurs at this point. After the fast-reset process, the circuit responds normally to subsequent input signals, and the CSA escapes the pulse dead zone caused by pile-up. These results indicate that the proposed CSA enables controlled accumulation of its output signals, thereby preventing the circuit from entering a pulse dead zone and enhancing event-reception rate. Moreover, compared to a traditional CSA, the feedback resistor Rf of the proposed CSA can be increased to reduce ballistic deficit impact and noise contribution for the same count-rate requirement. Additionally, the shaper output baseline is monitored during testing, and no significant baseline change occurs, indicating that the BLH circuit works properly and maintains baseline stability even under high count rates.

Fig. 10b [Figure 10: see original paper] illustrates measurement results for time parameters of shaper output signals. With a peak time (tp) of 240 ns, the

overall signal width (twidth) is approximately 800 ns. The ratio of twidth to tp is approximately 3.33, consistent with the expected value of 3.28. Measurement results show that piled-up signals with time intervals of no less than 450 ns can be correctly processed by the proposed shaper. The ratio of time-interval threshold tdelay,th2 to peak time is approximately 1.875, in good agreement with the expected value of 1.8. As shown in Fig. 10b [Figure 10: see original paper], the PDH circuit can effectively capture and hold peak values of shaper output signals with varying amplitudes, as long as the signals are detectable in the time channel. The proposed PDH circuit can detect piled-up signals from the shaper and hold them until the next signal arrives. The overall PDH functionality works as an event-driven analog memory following the first-in-first-out principle. Consequently, the designed high-speed PDH circuit in conjunction with a high-order shaper reduces the time interval between input signals from 3.33tp to 1.875tp. This enhancement results in a 77.6% increase in front-end readout circuit count rate, allowing the entire circuit to operate at megahertz count rates.

As illustrated in Fig. 11a [Figure 11: see original paper], the gain of the shaper output signal is approximately 2.85 mV/fC with a peak time of 600 ns, and the nonlinearity error is less than 1.2%. Concurrently, the PDH output signal demonstrates a gain of approximately 2.72 mV/fC with a nonlinear error below 1.4%. The measured ENC of the ASIC at room temperature under varying input capacitances (0 pF and 270 pF) and different peak times is presented in Fig. 11b [Figure 11: see original paper], where test results are generally consistent with post-simulation results. When CIN = 0 pF, ENC remains below 1500 e^- across all peak times. In this case, thermal and flicker noises are small, and increasing peak time causes current parallel noise to contribute more significantly to overall noise. Consequently, an optimal ENC value of 1101 e^- is obtained at a peak time of 480 ns. When APD detector capacitance is added to the input (CIN = 270 pF), ENC remains below 3500 e^- for all peak times. ENC stabilizes at values below 2500 e^- for peak times equal to or greater than 360 ns, reaching a minimum of 1966 e^- at a 1.68 µs peak time. Because thermal noise of input MOSFET M0 is inversely proportional to shaper peak time, ENC decreases with increasing peak time. However, current parallel noise associated with CSA feedback resistance (M1) and leakage current is proportional to peak time, and the percentage of flicker noise gradually increases as peak time increases; thus, ENC does not decrease significantly from 600 ns to 1680 ns. Fig. 11c [Figure 11: see original paper] illustrates test results of ENC variation with input capacitance under different peak times, demonstrating a linear increase in ENC with augmented input capacitance. Thermal and flicker noises of M0 are proportional to CSA input capacitance, while parallel noise is independent of input capacitance. Thus, the noise slope of ENC versus external input capacitance is inversely proportional to peak time. Noise slopes range from 7.8 e^-/pF at 120 ns to 3.08 e^-/pF at 1680 ns. The low noise-slope performance enables potential use in other applications with detectors having large output capacitance (several tens to hundreds of pF) [**?**, **?**].

The TOA and time resolution are measured at thresholds of 20 fC and CIN = 270 pF, as shown in Fig. 11d [Figure 11: see original paper]. Time walk is approximately 14.32 ns for input charges ranging from 30 to 500 fC. Higher input-charge signals exhibit better time resolution than lower input-charge signals. Time resolution is better than 125 ps at an input charge of 200 fC. Table 1 presents a comparison between SECALROC3 and other ASIC chips for ECAL applications. This ASIC provides low noise and high count-rate performance with reasonable power consumption. Additionally, subnanosecond time-measurement accuracy is realized for subtrigger systems of ECAL [**?**], and precision timestamp measurement allows the ECAL to improve shower reconstruction, energy correction, and particle identification performance [**?**]. Compared with the waveform-recording processing method [**?**], the peak-detection and holding method can significantly reduce recorded data volume, data output interface design difficulty, and hardware resource consumption of data-processing circuitry. One limitation of this method is that it does not record complete signal information, potentially leading to certain events being discarded.

IV. Conclusion

This study presents a low-noise, high-rate front-end readout ASIC designed for STCF ECAL. To address the challenge of high background-event rates in the STCF ECAL, we analyzed time parameters of output signals at various nodes in the analog front-end readout circuit. By leveraging pile-up capability to a certain extent at different nodes, the circuit was optimized and improved to increase count rate to the MHz/Ch scale. Experimental results indicated that the circuit successfully detected piled-up signals from the shaper output and that the maximum count rate of the proposed ASIC can reach 4 MHz/Ch at a peak time of 120 ns. For a count rate meeting requirements of 1.5 MHz/Ch (periodically distributed input signals), the maximum peak time of the shaper increased from 203 ns to 360 ns compared with traditional readout circuits, resulting in an approximately 200 e^- reduction in ENC to approximately 2500 e^-. Both energy and time measurements were implemented in this ASIC, providing the possibility of achieving PUR and calibration in the backend data-processing program to improve measurement accuracy of the readout system.

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