Postprint: A Scalable Four-Channel Radio Digital Receiver System

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Abstract

In response to the current demands of radio observation equipment for digital receivers featuring high sampling rates, wide bandwidth, multi-channel amplitude-phase consistency, as well as high-speed direct sampling and time-domain data storage, a 4-channel digital receiver system solution based on core components such as ZYNQ SOC and ADS54J60 is proposed through investigation and analysis of the technical architectures and functionalities of digital processing systems in multiple radio observation facilities. The single channel can achieve a maximum sampling rate of 1 GSPS, featuring flexible scalability where the number of sampling channels can be increased by adding boards, capable of meeting the requirements of future large-scale expandable radio interferometric arrays. The system consists of three types of equipment: high-speed data acquisition cards, optical communication receiver cards, and servers. Based on SerDes high-speed serial interface technology, it currently implements direct sampling with 16-bit quantization precision and 300 MSPS, featuring 60 dB full-scale signal-to-noise ratio, 40 Gbps SFP+ data transmission bandwidth, and 1.5 GB/s PCIe communication bandwidth, capable of acquiring intermediate frequency analog signals within the range of 4.5~150 MHz. Currently, the system has completed hardware and software design and testing. In testing, a sinusoidal signal with a frequency of 10 MHz and amplitude of 125 mV was sampled, resulting in an amplitude difference of less than 1 mV and phase delay of less than 3.3 ns among the four channels. The system integrates a programmable SFP+ communication interface and multi-device synchronization mechanism, which can adapt to the needs of multi-element array synchronous acquisition, and can simultaneously store raw radio signal data, providing more detailed time-domain data for radio astronomy research.

Full Text

Four-Channel Scalable Radio Digital Receiver System

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Abstract

In response to the requirements for high sampling rates, wide bandwidth, multi-channel amplitude-phase consistency, high-speed direct sampling, and time-domain data storage in current radio observation equipment, this paper investigates and analyzes the technical architectures and functionalities of digital processing systems across multiple radio observation devices. We propose a four-channel digital receiver system solution based on core components such as the ZYNQ SOC and ADS54J60 ADC. The system achieves a maximum sampling rate of 1 GSPS per channel, offering flexible scalability that allows channel count expansion through additional cards to meet the demands of future large-scale radio interferometric arrays. The system comprises three hardware components: a high-speed data acquisition card, an optical communication receiving card, and a server. Based on SerDes high-speed serial interface technology, the system has achieved direct sampling with 16-bit quantization accuracy at 300 MSPS, providing a 60 dB full-scale signal-to-noise ratio, 40 Gbps SFP+ data transmission bandwidth, and 1.5 GB/s PCIe communication bandwidth. It can capture analog signals in the intermediate frequency range of 4.5–150 MHz. Both hardware and software design and testing have been completed. In our tests, we sampled a 10 MHz sine wave signal with an amplitude of 125 mV, achieving an inter-channel amplitude difference of less than 1 mV and a phase delay of less than 3.3 ns. The system integrates programmable SFP+ communication interfaces and a multi-machine synchronization mechanism to accommodate synchronous acquisition needs in multi-element arrays, while simultaneously storing raw radio signal data to provide more detailed time-domain information for radio astronomy research.

Keywords: high-speed data acquisition; FPGA; JESD204B; PCIe; SFP+

1. Introduction

Radio signal observation is an indispensable detection method in astrophysics, playing a crucial role in exploring cosmological questions such as the Big Bang and energy characteristics of the universe [1-2]. Although ground-based observations are limited by the atmosphere, there exists a radio observation window with wavelengths covering 0.1–10 m [3]. The atmosphere's radio window, combined with economical construction methods and mature technical approaches, makes ground-based observation the primary means of radio astronomy [4]. The radio signal acquisition and processing system is the core component of ground-based radio observation equipment [5].

Representative foreign radio signal acquisition and processing systems include the ROACH-2 and SNAP-2 platforms from UC Berkeley [6], with the latest hardware being the CASPER series receivers [8] that have been applied in many large radio telescopes. The 500 m FAST telescope and Shanghai Tianma telescope both use the DBBC2 system to build terminal systems [7], enabling 500 Mbps data recording and supporting milliarcsecond-resolution mapping of fainter radio sources. Domestic research has also explored radio signal acquisition and processing systems, including a 3 GSPS, 9 GHz bandwidth solar radio digital receiver [13], and ground-based low-frequency radio astronomical digital receivers [4]. However, existing systems face challenges when applied to radio observation equipment, including lack of independent intellectual property rights and incomplete satisfaction of requirements.

China is actively advancing projects such as the Square Kilometre Array (SKA) [15] and the "Tianlai" experiment [14], all focusing on low-frequency radio observation and creating urgent demand for low-frequency radio signal acquisition and processing systems. This paper addresses the performance and functional requirements for radio signal acquisition and processing systems, designing two core boards based on Field Programmable Gate Array (FPGA) and high-performance ADCs: a four-channel high-speed data acquisition card and an optical communication receiving card. These boards can be used to construct a large-scale data acquisition and processing system [Figure 1: see original paper], enabling flexible expansion of acquisition channels and processing scale by simply adding more cards and servers, making it suitable for large-scale radio interferometric array construction and iterative upgrades.

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2. System Overall Design

The large-scale data acquisition and processing system constructed by the high-speed data acquisition card and optical communication receiving card is shown in [Figure 1: see original paper]. The overall framework of our digital receiver system is illustrated in [Figure 2: see original paper], while [Figure 3: see original paper] shows the physical components and connections.

The system consists of three main parts: high-speed data acquisition card, optical communication receiving card, and server. The high-speed data acquisition card digitizes analog signals and performs signal processing, uploading data via SFP+ optical communication using the Aurora 64B66B protocol. The optical communication receiving card serves as an intermediate component connecting the acquisition cards to the server and can function as a dynamically configurable coprocessor to assist with data processing. The host computer software on the server controls the workflow of both cards. The optical receiving card connects to the server via PCIe Gen2.0 $×$8, with 1000 M optical cables for large-scale data transmission and 1000 M Ethernet cables for control interaction between cards.

The data flow proceeds as follows: the antenna system receives radio signals that are fed into the high-speed data acquisition card's analog input channels AIN1–AIN4. The ADC samples and quantizes these signals, with the digital data undergoing timing adjustment in the ZYNQ processing core before transmission via SFP+ to the optical receiving card. The receiving card caches the data in DDR memory, from which the host software extracts it for storage and post-processing. The system achieves four-channel synchronous sampling at 300 MSPS per channel, with reserved expansion interfaces for synchronization signals and external clock inputs to enable multi-node synchronization in array deployments.

This architecture separates analog-to-digital conversion from data processing, allowing acquisition cards to be deployed close to antennas to avoid signal distortion from long analog transmission paths. The SFP+ optical interface provides 10 Gbps serial rates with strong anti-interference capability and long-distance transmission, maximizing compatibility with existing data reception facilities.

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3. High-Speed Data Acquisition Card Design

3.1 Hardware Framework

The high-speed data acquisition card hardware comprises signal conditioning circuits, ADCs, clock manager, optical communication interface, storage interface, and power circuits. Each analog input channel has a dedicated signal conditioning circuit consisting of a 4.5–3000 MHz bandpass balun converter and filtering circuit that converts single-ended input signals to differential signals for the ADC [Figure 6: see original paper].

The ADS54J60 is a low-power, 16-bit, dual-channel ADC supporting sampling rates up to 1.2 GSPS. It provides excellent spurious-free dynamic range across wide input frequencies with -159 dBFS/Hz noise floor and integrated analog input buffers. The LMK04828 clock manager provides ultra-low noise clock signals meeting JESD204B requirements, with integrated VCOs supplying high-quality synchronous clocks to both ADCs, ZYNQ processor, and storage interfaces.

The ZYNQ-7000 SOC (xc7z100) serves as the main controller, providing abundant programmable resources including RAM, DSP48E1 blocks, and SerDes transceivers.

The hardware interface connections are shown in [Figure 7: see original paper], with dashed lines indicating the synchronous clock distribution from the LMK04828. The physical prototype is shown in [Figure 8: see original paper].

3.2 Software Design

The FPGA program framework is illustrated in [Figure 9: see original paper]. The design includes: - **Hier_{ADC} module**: Receives JESD204B data streams from ADCs, performs frame alignment, and passes data to CDC_{Buffer} - **AuroraBlock module**: Transmits processed data via SFP+ interface using Aurora 64B66B protocol - **Hier_{ZYNQ7} module**: Manages AXI-Lite bus control of all functional modules

The processing core's firmware includes FSBL (First Stage Boot Loader), Bitstream (FPGA configuration), and ARM application executable. The ARM A9 processor uses AXI bus to access and control functional modules, configuring the LMK04828 and ADS54J60 via AXI Quad SPI and AXI GPIO. The system program flow is shown in [Figure 10: see original paper] and [Figure 11: see original paper].

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4. Optical Communication Receiving Card and Host Software

The optical communication receiving card is implemented using the MiLianKe MZ7100FB development board. Data from acquisition cards arrives via SFP+ fiber, is received by the Aurora 64B66B interface module in the ZYNQ processor's programmable logic, and cached to DDR memory under AXI-DMA control. The server host interacts with the card via PCIe protocol, with host software configuring functional modules through the XDMA driver.

The FPGA program framework [Figure 12: see original paper] includes: - **hire_{aurora} module**: Receives fiber data and outputs valid data to AXI4-Stream - **Clock Convert module**: Performs clock domain conversion - **hire_{xdma} module**: Caches data to external DDR and sends interrupts to the server

The program execution flow [Figure 14: see original paper] uses a ping-pong buffer scheme: 128 MB DDR space is pre-allocated with separate read/write address spaces. After data caching, an interrupt signals the server, which reads data via the XDMA function module. The PCIe bandwidth test results are shown in [Figure 15: see original paper], demonstrating 1,450 MB/s communication bandwidth.

5. Tests and Experiments

5.1 Amplitude-Frequency Characteristics

A RIGOL DG4062 signal generator produced a linear sweep sine wave (10 kHz–50 MHz, 2000 mV amplitude) split into four identical signals fed to AIN1–AIN4. Sampled data recorded by host software was processed in MATLAB, showing a relatively flat frequency response in the 4.5–50 MHz band with approximately 6.5 dB attenuation relative to input [Figure 16: see original paper]. The theoretical sampling range covers 4.5–150 MHz, consistent with Nyquist sampling principles.

5.2 Amplitude-Phase Consistency

A 10 MHz, 2000 mV sine wave was split to all four channels. The test revealed a fixed 3.3 ns phase delay between ADCs. After correction, channels within the same ADC chip showed nearly identical amplitude and phase, with inter-channel phase delay less than one sampling clock period [Figure 17: see original paper].

5.3 Noise Power Spectral Density

With 10 mV input, the noise power spectral density distribution across four channels showed floor noise at -129 dBm/Hz, matching spectrum analyzer observations. Strong noise points at 75 MHz and 100 MHz likely result from VCO signal coupling into input channels [Figure 18: see original paper].

5.4 Distortion-Free Acquisition

Testing with fixed-frequency, variable-amplitude signals (4–4000 mV) at 10 MHz demonstrated a dynamic amplitude range of 4–4000 mV. Sampled data showed high 辨识度 despite noise, with filtering effectively removing noise impacts. The 4000 mV large signal showed no distortion [Figure 19: see original paper].

5.5 Power Spectrum Analysis

A 16 V, 10 MHz sine wave was split to all channels. MATLAB analysis of 65536-sample FFTs yielded the performance parameters shown in . The power spectrum analysis results are presented in [Figure 20: see original paper].

Table 1 System Performance Parameter Test Results

Parameter Type	Channel 1 (dB)	Channel 2 (dB)	Channel 3 (dB)	Channel 4 (dB)
Signal-to-Noise Ratio	58.01	59.48	63.00	62.87
Total Harmonic Distortion	-61.21	-61.23	-61.14	-60.92

Parameter Type	Channel 1 (dB)	Channel 2 (dB)	Channel 3 (dB)	Channel 4 (dB)
Spurious-Free Dynamic Range	59.87	61.70	47.49	50.15
Signal-to-Noise-and-Distortion Ratio	73.24	71.05	71.64	71.61

6. Conclusion

This paper presents a four-channel scalable radio digital receiver system designed using ADS54J60 ADCs, LMK04828 clock manager, and ZYNQ7000 SOC as core components. The system achieves 300 MSPS sampling at 16-bit quantization with 60 dB SNR, 40 Gbps SFP+ bandwidth, and 1.5 GB/s PCIe bandwidth. The FPGA+FPGA+Server architecture supports remote deployment and can leverage GPU parallel computing for accelerated preprocessing. The GPSDO-based multi-machine synchronization mechanism provides solutions for synchronous sampling challenges in multi-element arrays. This system can be applied to future large-scale scalable radio interferometric array data acquisition systems, providing detailed time-domain data for radio phenomenon analysis.

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Note: Figure translations are in progress. See original paper for figures.