Digital data acquisition system for complex nuclear reaction experiments

Authors: Weiliang Pu, Yanlin Ye, Jianling Lou, Jiahao Chen, Yanlin Ye

Date: 2023-12-20T00:00:00+00:00

Abstract

A digital data-acquisition system based on XIA LLC products was employed in a complex nuclear reaction experiment using radioactive ion beams. A flexible trigger system based on field-programmable gate array (FPGA) parametrization was developed to accommodate varying experimental scales. A user-friendly interface was implemented, enabling the conversion of script language expressions into FPGA internal control parameters. The proposed digital system can be integrated with a conventional analog d…

Full Text

Preamble

Digital Data Acquisition System for Complex Nuclear Reaction Experiments

Wei-Liang Pu[1], Yan-Lin Ye[1],†, Jian-Ling Lou[1],‡, and Jia-Hao Chen[1],[2]

[1]School of Physics and State Key Laboratory of Nuclear Physics and Technology, Peking University, Beijing 100871, China
[2]Institute of Applied Physics and Computational Mathematics, Beijing 100094, China

A digital data-acquisition system based on XIA LLC products was employed in a complex nuclear reaction experiment using radioactive ion beams. A flexible trigger system based on field-programmable gate array (FPGA) parametrization was developed to accommodate varying experimental scales. A user-friendly interface was implemented, enabling the conversion of script language expressions into FPGA internal control parameters. The proposed digital system can be integrated with a conventional analog data acquisition system to provide enhanced flexibility. The performance of the combined system was validated using experimental data.

Keywords: Digital data acquisition system, Trigger, Programmable logic, Timestamp

Introduction

Currently, one of the frontiers in nuclear physics research is the exploration of exotic structures in unstable nuclei [?, ?, ?, ?]. Experiments on unstable nuclei typically rely on secondary radioactive ion beams, which generally suffer from low intensity. Consequently, such experiments require increasingly sophisticated detection systems, leading to a larger number of electronic channels and more complex trigger systems [?, ?, ?, ?].

Traditionally, analog data acquisition systems have been implemented based on standards such as CAMAC and VME [?, ?, ?]. These conventional systems comprise multiple layers of electronic units, including preamplifiers, shaping amplifiers, analog-to-digital converters (ADCs) for analog signal channels, fast amplifiers, discriminators, and time-to-digital converters (TDCs) for timing signals. The ADC or TDC extracts (buffers) energy (amplitude) or timing information under control of the trigger system [?, ?]. The trigger is typically generated from the coincidence of selected fast signals corresponding to the physical process of interest.

In recent years, with advances in fast digitization techniques, digital data acquisition (DDAQ) systems have been developed and widely adopted. In a DDAQ system, sampling and digitization are performed directly on signals from the preamplifier. The sampling frequency must be sufficiently high (generally above 100 MHz) to preserve the original information transmitted by the analog signal [?, ?, ?, ?]. The energy (amplitude) and timing information of the preamplified signal can then be extracted using well-designed digital processing methods. This approach replaces hardware electronic layers between the preamplifier and digital system—such as the main amplifier, discriminator, ADC, and TDC—with digital processes, making the entire system significantly more compact. Moreover, signal processing functions and trigger formation logic become more flexible compared to electronic pulses due to digitization. DDAQ systems offer considerable advantages over conventional analog DAQ systems, particularly when dealing with multiple complex channel signals [?, ?, ?, ?, ?].

Although signal processing methods differ significantly between DDAQ and conventional DAQ, the trigger concept and logic remain fundamentally the same. Generally, a trigger is formed from several signal channels necessary to define specific physical processes while excluding irrelevant processes as much as possible. The trigger is essential for reducing DAQ system dead time and conserving data storage space [?]. Since trigger logic must be defined by the user and may vary between experiments, a flexible trigger system should be designed [?, ?, ?, ?]. This can be realized in DDAQ systems using the rich logic operation capabilities provided by field programmable gate arrays (FPGAs) [?, ?, ?, ?].

In a recent nuclear reaction experiment conducted at the Radioactive Ion Beam

Line at the Heavy Ion Research Facility in Lanzhou (HIRFL-RIBLL1) [**?**], we employed a DDAQ system based on hardware from XIA LLC [**?**] combined with a conventional DAQ system (VME). We provide a general description of this new combined DAQ system, which will be valuable for many similar experiments. In Section II, we describe the DDAQ system hardware. Section III details the configuration of the flexible trigger system. Section IV presents applications to experiments of different scales. Section V describes the method for combining a conventional VME system with the newly developed DDAQ (XIA) system. Experimental test results are presented in Section VI, followed by a summary.

II. Basic Composition of a DDAQ System

A. Major Components

The actual DDAQ system comprises five hardware components produced by XIA LLC [**?**]. The primary component is the Pixie-16 6U Compact PCI/PXI crate, which hosts other plugin units, supplies local power, and transmits digital signals between units. The second component is a PCI-8366/PXI-9369 crate controller, which serves as the commander for other modules and communicates with the computer. The computer sends commands to the DAQ system and retrieves data from module memory through the crate controller. The third component is the Pixie-16 acquisition module, which converts analog signals into digital data via sampling and extracts energy and time information from input signals according to predefined algebraic formulas [**?**]. Various Pixie-16 versions digitize analog signals at sampling rates of 100, 250, or 500 MHz, storing each sample in 12, 14, or 16 bits. The Pixie-16 acquisition module performs the functions of a shaping amplifier, discriminator, ADC, and TDC in traditional DAQ (e.g., VME) systems. The fourth component is the MicroZed-based Trigger IO (MZTIO) module containing the FPGA chip. The final component, the P16Trigger module, synchronizes triggers and clock signals across multiple crates [**?**].

The trigger system must combine selected fast source signals to generate the main trigger signal that prompts DAQ modules to extract and save data. A trigger source signal is generally a fast signal originating from a Pixie-16 acquisition module or MZTIO logic module (based on a commercial FPGA chip from Xilinx [**?**]). Several methods exist for forming and broadcasting the main trigger (see sections below). In our design, the main trigger appears as an external signal called a "module-validation trigger" [**?**]. Thus, all Pixie-16 acquisition modules can be activated by the same main trigger.

B. Flexible Configuration in FPGA

We designed and implemented a flexible framework for the FPGA, schematically shown in Fig. 1 [Figure 1: see original paper]. Logic units in the FPGA are represented as boxes, and arrows indicate the flow direction of digital signals. Trigger source signals originate from the input RJ45 connector on the left, pass

through four optional layers of logic units, and exit to right-side ports. The four logic-function layers are divided into two groups. The first group contains the first two layers configured with “or”-gates and “and”-gates. The second group contains the last two layers configured with down-scale units and programmable (“or”/“and”) gates. The expanding widths of arrows indicate increasing numbers of signal channels. The maximum number of input or output ports is 48, constrained by RJ45 connectors.

Each port can be programmed as input or output. Logic units in the same layer are identical and independent, functioning according to their own parameter configurations. Moreover, all logic units are optional, meaning each source signal may pass through selected complex logic units or simply bypass all layers without any logic operation. This flexibility is implemented using a mask unit (upper part of Fig. 1) in front of a logic gate and a multiplexer [**?**] in front of a downscaled unit (see the second group in the figure). Both masks and multiplexers filter input signals. The multiplexer has only a single output line, whereas a mask can send multiple outputs. Therefore, the “and”-gate or “or”-gate behind the mask unit can perform logic operations on multiple input source signals, while the downscaler and programmable “and”/“or”-gates can manipulate one input signal from each multiplexer.

Based on this configuration, the first group (layers 1 and 2) can perform almost all types of logic combinations for input source signals. In practice, the first layer is dedicated to “or” coincidence, while the second layer is dedicated to “and” coincidence. A real example is presented in Section II.C. Fig. 1 shows only three gates, but an actual FPGA module provides 16 gates, which is sufficient for typical nuclear reaction experiments. Moreover, by applying the mask, one “or”-gate in the first layer may select any input source signal from the 48 input ports. Similarly, one “and”-gate in the second layer may select input signals from the 48 input ports and 16 outputs from “or”-gates, leading to 64 choices defined by the corresponding mask. This explains why thicker arrows point to the “and”-gates compared to those pointing to the “or”-gates.

The second group serves the downscaling function. This is useful when some accompanying processes in an experiment are much more probable than targeted physical processes. Recording these high-rate accompanying processes must be suppressed to maintain high DAQ efficiency for processes of interest. For instance, if the accompanying rate is 50,000 Hz, a downscaling factor of 100 would reduce the output signal rate to 500 Hz, meaning one output for every 100 inputs. The fourth layer comprises programmable “or”/“and” gates. Each gate may receive two channels: one from the downscaler and the other directly from the second or earlier layer. Although only one unit is shown in the third and fourth layers (Fig. 1), four independent units are incorporated into each layer.

The above-described FPGA configuration is sufficiently flexible to meet trigger-logic requirements for general nuclear reaction experiments [**?**, **?**, **?**, **?**]. Trigger logic can be simply changed by editing parameter values for masks and multi-

plexers with the help of a Xillybus Lite IP core [**?**]. The numbers of manipulable parameters in the masks or multiplexers for each layer are listed in Table 1 .

C. Configuration with Script Language

An FPGA configuration file written in script language may comprise several lines of expression, such as those shown in Fig. 2 [Figure 2: see original paper]. Each line expresses a logic calculation based on digital signals, which may include logic "or" (|), logic "and" (&), fraction (/), etc. In the example (Fig. 2), the first line describes the logic "or" for source inputs from ports A3 and A7, with the result downscaled by a factor of 10 to form output D0. We denote the 48 input ports as A0–A15, B0–B15, and C0–C15. The second line shows that A2 outputs equal the complex logic result from signals D0, A0, A3, A4, A7, A12, B0, and B4. The third line is similar to the second line, but with outputs sent to port B14. Although the logic expression is complex and contains four layers, it can be converted into two layers expressed as "(A3|A0|A4|B0|B4)&(A7|A0|A4|B0|B4)&(A12|B0|B4)" in the software. This conversion is guaranteed by the distributive law [that is, A&(B|C) = (A&B)|(A&C)]. Obviously, the first layer considers the expression in parentheses and the second layer relates to the "&" operator. This structural conversion is illustrated schematically in Fig. 3 [Figure 3: see original paper].

The fourth line in Fig. 2 is an additional function that generates a 5-MHz clock signal at port C21, used to match timing between different DAQ systems such as VME and XIA systems (more details in Section IV). This is a periodic signal with logic "1" and "0," each occupying half the period. The frequency is defined using the configuration file (5 MHz as an example). The fifth line defines a scaler called S0 that counts the frequency of the "or"-coincidence of A3 and A7. This function records one of the trigger rates used to monitor the online experiment and normalize the corresponding cross section in data analysis.

The currently designed software can set up the FPGA in three steps: read the configuration file written in script language, convert its contents into FPGA configuration parameters, and write the parameters to FPGA memory. It functions as a compiler that converts script expressions into configuration files. Using this software, FPGA setup becomes easier to implement.

III. Application to Small, Medium, and Large DAQ Systems

The number of signal channels for a reaction experiment varies with the complexity of the actual detection system, which depends on the physical processes to be measured. We define a small-sized DAQ system as one where the total number of signal channels can be accommodated in three data acquisition modules (i.e., fewer than 48 channels). Medium size corresponds to a DAQ system using only one crate (i.e., fewer than 11 data acquisition modules or 176 channels). A large-size DAQ system uses multiple crates. Note that these definitions

can be adjusted by DAQ users.

For all three DAQ types, we employed a central structure to manage data acquisition. This structure divides modules into central and local modules, as schematically shown in Fig. 4 [Figure 4: see original paper]. The center module may be a Pixie-16 acquisition module or an FPGA logic module, depending on DAQ size, which generates the main trigger signal and controls data acquisition. Other Pixie-16 acquisition modules are regarded as local. The central structure for all three sizes operates in five steps for one data recording cycle: 1) the local Pixie-16 acquisition module generates a fast trigger source signal from the electrical analog signal; 2) the center module receives many trigger source signals; 3) the center module makes logical combinations of all received trigger source signals and generates the main trigger signal; 4) the center module sends the main trigger back to the local modules; 5) the local modules, according to time matching with the main trigger, process the local signal and store the data.

A. Small-Size DAQ

According to the XIA system design, a neighboring module can share the fast-trigger source signal without disturbing other modules (not using the overall connection lines on the crate backplane). For a small-sized DAQ, the three Pixie-16 acquisition modules (48 channels total) should be installed in neighboring slots, with the middle module serving as the center module and the side modules as local modules. In Step 2, the center module receives trigger source signals from the two local modules via dedicated neighboring connections. In Step 3, the middle (center) module combines trigger source signals into the main trigger according to a preset built-in function. This function was designed by XIA, allowing flexible parameter settings for logical operations. The main trigger can then be broadcast to all local modules via common lines on the crate backplane.

B. Medium-Size DAQ

For a medium-sized DAQ, a logic FPGA module should be included as the center module. Since up to ten trigger source signals may originate from local modules, they could interfere with each other if common connection lines on the crate backplane are used. To avoid this issue, Category 6 (Cat 6) cables were used to connect the front panels of local modules to the center module individually, enabling safe implementation of Step 2. This method is limited by the number of RJ45 connectors on the center logic module front panel (12), some of which must be used for other purposes. An alternative approach called “group connection” may be adopted for the RJ45 connectors. First, three neighboring local modules can be connected as a group via dedicated neighboring connection lines, and a grouped trigger source signal can be sent to the center according to built-in functions. This grouping is particularly reasonable when a single detector, such as a silicon strip or wire-plane detector, spans several 16-channel DAQ modules. Consequently, the center module receives fewer source signals from the front panel in Step 2, then broadcasts the main trigger signal to each

local module via common lines on the crate backplane in Step 4. Evidently, this method can only be applied to DAQ systems with a single crate.

C. Large-Size DAQ

For a large DAQ, several crates must be controlled by the same center module. The grouped trigger sources described above can still be used in Step 2. However, broadcasting the main trigger in Step 4 cannot be realized via the backplane of a single crate. Therefore, Step 4 is divided into two substeps. The first substep involves sending the main trigger through a Cat 6 cable to a relayed module in each crate. In the second substep, the relayed module broadcasts the main trigger through the backplane of its host crate. Although this solution is significantly complex and limited by the number of RJ45 connectors, it maintains synchronization between crates and modules while simplifying parameter settings across all modules. For even more complex DAQ systems, multiple logic FPGA modules with more complicated connection configurations and parameter settings are necessary.

D. Signal Timing Matching

As described in the Introduction, experimental data must be recorded and analyzed according to physical events. In other words, data from different signal channels should coincide such that they correspond to the same experimental event. However, signals in different channels may experience different processing times during detection, pre-amplification, analog signal transmission, digitization, and logic operations. Therefore, a trigger system should account for these differences. We assume that timing differences for analog signals have already been addressed by setting offsets based on measurements. Here, we consider only DAQ processes, which involve three steps. The first step matches trigger source signals within one module or from neighboring modules. Some jitter exists among signals due to fluctuations in detection and electronics systems, noise signals, signal-shape uncertainties, and minor variations in hardware products. Hence, the trigger source signal width is set to 400 ns to cover jitter. Additionally, source signals from modules with 250-MHz sampling rate should be delayed by approximately 60 ns to be consistent with modules having sample rates of 100 MHz or 500 MHz. The second step matches trigger source signals from different local modules. This is performed in the central logic module by setting offsets for each received source signal. Occasionally, this step can be ignored if the first step already provides sufficient matching. The third step matches data signals in local modules with the main trigger signal sent from the central module. The main trigger lags behind local source (or data) signals by approximately 200 ns, which can be compensated by applying a delay to local signals (see Fig. 4). Considering jitter in local signals, the main trigger signal width is generally set to 500 ns or longer to ensure good overlap with all valid data signals in local modules. Thus, to achieve good overlap of all local data signals with the wide main trigger signal, the delay time of local data signals

should be increased to 450 ns (200 + 250 ns).

IV. Combination of the DDAQ System with the Conventional DAQ System

Although DDAQ systems offer advantages as stated in the Introduction, conventional DAQ (e.g., VME) systems remain useful due to availability of numerous existing modules and crates. Therefore, when XIA modules are insufficient, XIA and VME systems can be used in combination [**?**, **?**]. However, for such mixed systems, event alignment (matching) between the two systems is essential. In a conventional DAQ system, data are stored according to the number of physical events (triggers), with each event containing information (energy, time, etc.) from all channels. In contrast, the XIA system successively records signal information from each channel with timestamps. Thus, a physical event corresponds to signal information distributed across several channel data packages that are correlated only by their timestamps.

Additionally, due to the fast signal processing capability of the XIA system, it can record high-rate signals, such as those from forward-angle detectors. The VME system may be applied to low-rate signals, such as those from large-angle detectors. Since each system has its own trigger settings and operation, the XIA system can record a high number of events compared to the VME system. Therefore, determining correspondence between VME event numbers and XIA timestamps is essential.

This problem can be resolved by recording timestamps in the VME system and aligning them in both systems [**?**, **?**]. In the XIA system, a timestamp represents the duration from the start of the data-recording run (data file). Typically, timing is represented by clock numbers. For example, in an XIA system, the clock frequency is the same as the sampling rate (e.g., 100 MHz, or a period of 10 ns). Thus, a timestamp of 200 indicates 2 µs from run-start time.

The following modifications were incorporated into the DAQ system to set and match timestamps, as schematically shown in Fig. 5 [Figure 5: see original paper]. First, we adopted a V830 scaler module (marked as SDC in Fig. 5) in the latching scaler mode of the VME system [**?**]. It records timestamps when the input signal is a periodic clock signal, as shown in Fig. 6 [Figure 6: see original paper]. For example, two VME triggers may randomly coincide with the 4th and 13th clock cycles. Then, the V830 scaler records numbers 4 and 13 into the corresponding event data, stamping VME events at 400 ns and 1300 ns when the clock frequency is 10 MHz. The clock signals are usually generated from the XIA-FPGA chip. Therefore, the clock frequency should be selected appropriately. An excessively high frequency may cause memory overflow and bit flipping in the V830 module, whereas a low frequency degrades time resolution in subsequent matching procedures. A clock rate of 5 MHz was used in the previous experiment (see section below).

To align timestamps in both VME and XIA systems, we set the VME main

trigger to be included in the XIA trigger series and recorded as one-channel data in the XIA system, as depicted in Fig. 5. This enables comparison of timestamps between XIA and VME systems for common trigger signals. Since processing time for a common trigger signal in either system is constant during the entire data acquisition run, the difference between timestamps from the two systems should also be constant. This conclusion remains valid even if run (file) starting times in both systems differ slightly due to manual control methods. Evidently, only the time offset needs to be determined to match the two systems. This offset can be easily fixed by scanning time differences in both systems for all common trigger signals at each offset setting, as shown in Fig. 7 [Figure 7: see original paper]. In fact, common trigger signals initiated by the VME system are randomly distributed in time. If the offset is incorrect, as indicated by the two upper lines in Fig. 7, the ratio of matched trigger number to total trigger number must be small. In contrast, the matched rate can approach 1.0 when the correct offset is applied (see lower panel of Fig. 7). To find the correct offset, we can simply step the offset through an estimated time range and check the matching rate. The match count increases when common trigger signals appear in both VME and XIA systems within a small time window, as indicated by the pair of diagonal dashed lines in the upper panel of Fig. 7. The width of this time window must be smaller than the average time interval between adjacent common trigger signals. This interval is approximately 10 ms in recent experiments. After determining the highest match rate (over 95% for our experiment), the offset can still be fine-tuned to obtain exact timing overlaps of corresponding trigger signals.

V. Experimental Test Results

The combined DAQ system was applied in a nuclear reaction experiment at the radioactive ion beamline of HIRFL-RIBLL1 [**?**]. Several beams, such as ^{14}C and ^{16}C, were used with beam intensities of approximately 5×10^4 pps.

In this experiment, multiple layers of silicon strip detectors were mounted at 0° to detect decay fragments at forward angles. An annular telescope comprising a layer of silicon strip detectors and an array of CsI(Tl) scintillators was installed to cover larger scattering angles. The essential trigger logic records events with multiple decay fragments hitting silicon strips in the zero-degree detectors, or any particle hitting the large-angle annular telescope. Since the number of single-hit events on the zero-degree detector was large, these events were downscaled by the DAQ corresponding to direct beam incidence to reduce total trigger rate. Therefore, each recorded event must belong to one of three types: 1) multiple hits in the zero-degree detector, 2) a single hit in the zero-degree detector but subjected to sampling, or 3) any hit in the annular detector. The counting rates for these three types were approximately 2×10^4, 3.5×10^4 (before downscaling), and below 100 Hz, respectively. Due to the fast capacity of the XIA system, type-1 and type-2 events were recorded by XIA, while type-3 events were recorded by the VME system and partially by the XIA system for

cross-DAQ verification (see next paragraph).

Owing to limited DAQ capacity, reducing the number of forward-angle single-hit events is important for maintaining high efficiency (high live-time rate) for multiple-hit events. Figure 8 [Figure 8: see original paper] shows the ratio of multiple-hit events to total recorded events, which increases with increasing downscale factor for single-hit events. We note that the trigger rate in the VME system associated with large-angle detection by annular telescopes is independent of the XIA system and thus was not affected by downscaling in the XIA system.

During the experiment, we maintained a live-time rate higher than 90% for the DDAQ system (after downscaling), whereas this rate was always ~100% for the VME system due to its very low trigger rate.

As described above, some data detected by the annular telescope were recorded by both VME and XIA systems, which can be used to verify correctness of timestamp matching between the two systems. Figure 9 [Figure 9: see original paper] shows a particle identification (PID) spectrum using energy loss ΔE detected by the first layer of the annular telescope (Si strip) and recorded by the VME system versus remaining energy E detected by the second layer (CsI(Tl)) and recorded by the XIA system. The clear PID curves for H and He isotopes demonstrate perfect matching of the two DAQ systems.

VI. Summary

DDAQ based on hardware products from XIA LLC was applied to a complex nuclear reaction experiment. A flexible FPGA logic configuration was implemented for trigger handling. Software was developed to convert simplified logic definitions in script language into system internal parameters. Moreover, the central structure (central and local modules) of DDAQ provides convenient solutions for small, medium, and large experiments. A practical method was established to combine the DDAQ (XIA) and conventional DAQ (VME) systems, which is particularly useful for the current transition from conventional DAQ to digital systems. The combined system was successfully applied to a complex nuclear reaction experiment using HIRFL-RIBLL1. The present work will be of interest to experimentalists adopting DDAQ in the coming years.

Acknowledgements

The authors thank Dr. Hong-Yi Wu for fruitful discussions and the experimental teams who supported application of the present DDAQ system.

Author Contributions

All authors contributed to study conception and design, as well as data collection and analysis. The present DDAQ application codes were implemented by Wei-Liang Pu. The first draft of the manuscript was written by Wei-Liang Pu and

all authors revised previous versions of the manuscript. All authors read and approved the final manuscript.

Data Availability Statement

The data that support the findings of this study are openly available at https://www.doi.org/10.57760/sciencedb.14278 and https://cstr.cn/31253.11.sciencedb.14278 via Science Data Bank.

Conflict of Interest

The authors declare that they have no competing interests.

References

[1] Y. Liu, Y.L. Ye, Nuclear clustering in light neutron-rich nuclei, Nucl. Sci. Tech 29, 184, (2018). 10.1007/s41365-018-0522-x
[2] Y.L. Ye, X.F. Yang, Y. Liu et al., Radioactive ion beam physics related to HIAF. Science in China Series A-Mathematics 50, 112003, (2020). 10.1360/SSPMA-2020-0282
[3] H. Hua, Y.L. Ye, X.F. Yang, Advancements in nuclear physics research using Beijing HI-13 tandem accelerator. Nucl. Tech. (in Chinese) 46(08), 51-62, (2023). 10.11889/j.0253-3219.2023.hjs.46.080004
[4] Y. Chen, Y.L. Ye, K. Wei, Progress and perspective of the research on exotic structures of unstable nuclei. Nucl. Tech. (in Chinese) 46(08) 189–194, (2023). 10.11889/j.0253-3219.2023.hjs.46.080020
[5] Y. Liu, Y.L Ye, J.L. Lou et al., Positive-parity linear-chain molecular band in ^{16}C. Phys. Rev. Lett. 124, 192501 (2020) 10.1103/PhysRevLett.124.192501
[6] K. Ma, Y.L Ye, C.J. Lin et al., New measurements of ^{4}He and proton decay from the resonant states in ^{19}Ne*. Chinese Phys. C 47, 114001 (2023) 10.1088/1674-1137/acc16f
[7] J.X. Han, Y.L Ye, J.L. Lou et al., A nuclear linear chain structure arises at carbon-14. Commun. Phys. 6 220 (2023). 10.1038/s42005-023-01342-6
[8] J.H. Chen, Y. L. Ye, K. Ma et. al., New evidence of a hoyle-like structure in ^{16}O. Science Bulletin 68, 1119–1126 (2023). 10.1016/j.scib.2023.04.031
[9] R.V. Ribas, A camac data acquisition system based on PC-Linux. Nucl. Instrum. methods Phys. Res. A 483, 830–832 (2002). 10.1016/S0168-9002(01)01950-7
[10] T. Prokscha, R. Scheuermann, U. Hartmann et al., A novel VME based μSR data acquisition system at PSI. Physica B Condensed Matter 404, 1007–1009 (2009) 10.1016/j.physb.2008.11.206
[11] H. Baba, T. Ichihara, T. Ohnishi et al., New data acquisition system for RIKEN Radioactive Isotope Beam Factory. Nucl. Instrum. Methods Phys. Res. A 616, 65–68 (2010) 10.1016/j.nima.2010.02.120
[12] Y.C. Liu, X.F. Yang, S.W. Bai et al., Control and data acquisition systems for collinear laser spectroscopy. Nucl. Sci. Tech. 34, 38 (2023).

10.1007/s41365-023-01197-0
[13] M.J Koskelo, I.J Koskelo, B Sielaff, Comparison of analog and digital signal processing systems using pulsers. Nucl. Instrum. Methods Phys. Res. A 422, 373–378 (1999). 10.1016/S0168-9002(98)00986-3
[14] S. Mitra, L. Wielopolski, G. Hendrey, Comparison of a digital and an analog signal processing system for neutron inelastic gamma-ray spectrometry. Appl. Radiat. Isotop. 61, 1463–1468 (2004) 10.1016/j.apradiso.2004.02.024
[15] J. Kamleitner, S. Coda, S. Gnesin et al., Comparative analysis of digital pulse processing methods at high count rates. Nucl. Instrum. Methods Phys. Res. A 736, 88–98 (2014) 10.1016/j.nima.2013.10.023
[16] D.W. Luo, H.Y. Wu, Z. H. Li et al., Performance of digital data acquisition system in gamma-ray spectroscopy. Nucl. Sci. Tech. 32, 79 (2021). 10.1007/s41365-021-00917-8
[17] C.J. Prokop, S.N. Liddick, B.L. Abromeit et. al., Digital data acquisition system at the National Superconducting Cyclotron Laboratory. Nucl. Instrum. Methods Phys. Res. A 741, 163–168 (2014) 10.1016/j.nima.2013.12.044
[18] R. Grzywacz, Applications of digital pulse processing in nuclear spectroscopy. Nucl. Instrum. Methods Phys. Res. B 204, 649–659 (2003) 10.1016/S0168-583X(02)02146-8
[19] S. Marrone, D. Cano-Ott, N. Colonna et al., Pulse-shape analysis of liquid scintillators for neutron studies. Nucl. Instrum. Methods Phys. Res. A 490, 299–307 (2002) 10.1016/S0168-9002(02)01063-X
[20] S.N. Liddick, I.G. Darby, R.K. Grzywacz, Algorithms for pulse shape analysis using silicon detectors. Nucl. Instrum. Methods Phys. Res. A 669, 70–78 (2012) 10.1016/j.nima.2011.12.034
[21] X. Wang, Z.H. Li, Z. Liu et al., An effective digital pulse-processing method for pile-up pulses in the decay studies of short-lived nuclei. Nucl. Instrum. Methods Phys. Res. A 971, 164068 (2020) 10.1016/j.nima.2020.164068
[22] The ATLAS Collaboration, Performance of the ATLAS Trigger System in 2010. Eur. Phys. J. C 72, 1849 (2012). 10.1140/epjc/s10052-011-1849-1
[23] P. Ottanelli, G. Pasquali, L. Baldesi et al., The Florence trigger-box (FTB) project: An FPGA-based configurable and scalable trigger system. Nucl. Instrum. Methods Phys. Res. A 1015, 165745 (2021) 10.1016/j.nima.2021.165745
[24] H.Y. Wu, Z.H. Li, H. Tan et al., A general-purpose digital data acquisition system (GDDAQ) at Peking University. Nucl. Instrum. Methods Phys. Res. A 975, 164200 (2020) 10.1016/j.nima.2020.164200
[25] R. Tanuma, H. Baba, K. Ninomiya et al., New FPGA-based trigger/DAQ system for MTV experiments (2014). TRIUMF. Phys. Part. Nuclei 10.1134/S1063779614011036
[26] D. Guo, Y.H. Qin, S. Xiao et al. An FPGA-based trigger System for CSHINE. Nucl. Sci. Tech. 33 162 (2022). 10.1007/s41365-022-01149-0
[27] Z. Sun, W.-L. Zhan, Z.-Y. Guo et al., RIBLL, the radioactive ion beamline in Lanzhou. Nucl. Instrum. Methods Phys. Res. A 503, 496–503 (2003) 10.1016/S0168-9002(03)01005-2
[28] https://www.xia.com
[29] W. Hennig, H. Tan, M. Walby et al., Clock and trigger synchronization

between several chasses of the digital data acquisition modules. Nucl. Instrum. Methods Phys. Res. B 261, 1000–1004 (2007) 10.1016/j.nimb.2007.04.181
[30] xilinx.com
[31] J. Hoolan, Telecommunications Engineer's Reference Book. Butterworth-Heinemann. (1993) 10.1016/B978-0-7506-1162-
[32] https://xillybus.com/xillybus-lite
[33] https://github.com/kinstaky/easy-config-logic
[34] A.V. Aho, M.S. Lam, R. Sethi et al., Compilers, Principles, Techniques, and Tools (2nd edition). Addison-Wesley. (2006).
[35] G. Wittwer, L. Legeard, G. Lebertre et al., who merged several separate data acquisition systems in GANIL. 14th IEEE-NPSS Real Time Conference (2005) 10.1109/RTC.2005.1547489
[36] H. Baba, T. Ichihara, T. Ohnishi et al., a time-stamping system for nuclear physics experiments at RIKEN RIBF. Nucl. Instrum. Methods Phys. Res. A 777, 75–79 (2015) 10.1016/j.nima.2014.12.051
[37] CAEN S.p.A., V820/V830 - 32 Channel Latching Scaler Family (CAEN 2015). https://www.caen.it/products/v830/

Note: Figure translations are in progress. See original paper for figures.