Total Ionizing Dose Effect Modeling Method for CMOS Digital Integrated Circuits

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Abstract

Simulating the total ionizing dose (TID) of an electrical system using transistor-level models can be difficult and expensive, particularly for digital integrated circuits (ICs). In this study, a method for modeling TID effects in complementary metal-oxide semiconductor (CMOS) digital ICs based on the input/output buffer information specification (IBIS) was proposed. The digital IC was first divided into three parts based on its internal structure: the input buffer, output buffer, and functional area. Each of these three parts was separately modeled. Using the IBIS model, the transistor V-I characteristic curves of the buffers were processed, and the physical parameters were extracted and modeled using VHDL-AMS. In the functional area, logic functions were modeled in VHDL according to the data sheet. A golden digital IC model was developed by combining the input buffer, output buffer, and functional area models. Furthermore, the golden ratio was reconstructed based on TID experimental data, enabling the assessment of TID effects on the threshold voltage, carrier mobility, and time series of the digital IC. TID experiments were conducted using a CMOS noninverting multiplexer, NC7SZ157, and the results were compared with the simulation results, which showed that the relative errors were less than 2% at each dose point. This confirms the practicality and accuracy of the proposed modeling method. The TID effect model for digital ICs developed using this modeling technique includes both the logical function of the IC and changes in electrical properties and functional degradation impacted by TID, which has potential applications in the design of radiation-hardening tolerance in digital ICs.

Full Text

Preamble

Total Ionizing Dose Effect Modeling Method for CMOS Digital Integrated Circuits

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Simulating the total ionizing dose (TID) effect in electrical systems using transistor-level models can be difficult and expensive, particularly for digital integrated circuits (ICs). In this study, we propose a method for modeling TID effects in complementary metal-oxide semiconductor (CMOS) digital ICs based on the Input/Output Buffer Information Specification (IBIS). The digital IC is first divided into three parts based on its internal structure: the input buffer, output buffer, and functional area, each of which is modeled separately. Using the IBIS model, the transistor V-I characteristic curves of the buffers are processed, and the physical parameters are extracted and modeled using VHDL-AMS. In the functional area, logic functions are modeled in VHDL according to the datasheet. A golden digital IC model is developed by combining the input buffer, output buffer, and functional area models. Furthermore, the golden model is reconstructed based on TID experimental data, enabling assessment of TID effects on threshold voltage, carrier mobility, and timing characteristics of the digital IC. TID experiments were conducted using a CMOS non-inverting multiplexer, NC7SZ157, and the results were compared with simulation results, showing relative errors of less than 2% at each dose point. This confirms the practicality and accuracy of the proposed modeling method. The TID effect model for digital ICs developed using this technique includes both the logical function of the IC and changes in electrical properties and functional degradation caused by TID, which has potential applications in the design of radiation-hardened digital ICs.

Keywords: CMOS digital integrated circuit, Total ionizing dose, IBIS model, Behavior-physical hybrid model, Physical parameters

Introduction

Many cosmic rays with different energy ranges exist in the universe. Cosmic ray particles include protons, neutrons, electrons, charged particles, photons, and other types of particles, with energies in the mega- to exa-volt range. The electrical characteristics of electronic components exposed to radiation are disturbed and degraded.

Among the different radiation effects, the total ionizing dose (TID) effect impacts the electrical characteristics of MOSFETs, generating changes in transconductance, leakage current, and threshold voltage drift. This is a cumulative

effect that cannot be avoided in orbit and is the principal factor influencing the service life of electrical components. Because spacecraft contain a significant number of MOSFETs and the TID effect is widespread in low Earth orbit (LEO), medium Earth orbit (MEO), geosynchronous Earth orbit (GEO), and deep-space exploration environments, the damage to MOSFET performance caused by the TID effect must be evaluated.

Currently, methods for evaluating the TID effect in electronic components primarily include experiments and model simulations. The former is dependent on the instrumentation environment and is costly, whereas the latter is a quick and inexpensive primary approach for assessing irradiation damage to a component.

Several significant advances have been made in research on the impact of TID on MOSFETs in computer science, ICs, and semiconductor technologies. References [1–9] studied the impact of TID on MOS components using semiconductor physics and technology computer-aided design (TCAD) software simulations. The impact of TID on the threshold voltage of MOS components was studied in [10–13]. According to these findings, TID mainly impacts threshold voltage drift caused by interface- and hole-trap charges formed in the oxide layer, as well as increases in leakage current and decreases in carrier mobility. To model the TID effect, references [14–17] developed models of MOSFET deterioration triggered by TID, and references [18–25] produced numerical models of the TID effect and analyzed I-V curves. Owing to rapid advancements in artificial intelligence, Jia et al. [26] applied neural networks to capture the electrical characteristics of transistors and developed a unique transistor model with more accurate DC characteristics than traditional models. SPICE models of TID and damage effects in MOSFETs were developed using macroscopic modeling approaches [27, 28], and simulation results confirmed the combined influence of these effects on the advanced degradation of MOSFET characteristics and CMOS circuits.

Because of high computational costs and limited circuit size for simulations, recent modeling and simulation approaches are not suitable for large-scale digital ICs. In this study, we propose a method for modeling the TID effect of CMOS digital ICs based on the Input/Output Buffer Information Specification (IBIS) model. This is a hybrid behavioral and physical level model that accurately represents both the logic functions of digital components and physical parameters of the TID effect on component ports. This is achieved using the VHDL-AMS language, which enables faster simulations of TID effects on large digital ICs compared to transistor-level modeling [29].

Methodology

The IBIS model is a file format used to describe various input and output buffer characteristics of a component [30]. An IBIS file is composed of three core parts: file header, component description, and model description, all of which provide data to effectively identify all input, output, and I/O-type buffers of a device. The file header includes information such as the IBIS version, file name,

and other critical information. The component description includes package parameters, pin mappings, component names, and other key information. Finally, the model description provides the buffer type, threshold level, and four different types of V-I data tables: pullup, pulldown, power clamp, and GND clamp. Moreover, it includes V-T data tables showing the rising and falling edges of buffer state changes. This format combines radiation electronics and signal transmission information to accurately describe the behavior of component buffers.

Overview of the Method

The internal structures of digital components are shown in Figure 1: see original paper, where an input signal from outside the component first passes through the input buffer, then through the internal logic circuit, and is transmitted to the external circuit through the output buffer. Properly expressing the actual input-output connection of a component requires accurate description of both the internal logic and electrical properties of the input-output buffer.

Consequently, we mapped the structure shown in Figure 1: see original paper to the hybrid behavioral-physical model structure of the CMOS digital IC, as shown in Figure 1: see original paper. In this hybrid model, the CMOS digital IC is separated into three parts: input buffer, functional region, and output buffer. The functional region describes the logic function of a digital integrated circuit and is modeled using VHDL language based on component Boolean expressions and data from the datasheet. The input and output buffers provide the physical characteristics of the digital IC ports, which are modeled using VHDL-AMS for the port-transistor physical properties of the digital IC.

The input and output buffers of a CMOS digital IC are both equipped with electrostatic discharge (ESD) protection circuits, which typically consist of clamp diodes and ground-gate NMOS (GGNMOS) components. Diodes are extensively used in low-voltage ESD protection. The input buffer includes an ESD protection circuit with upper- and lower-clamp diodes DP1 and DN1, respectively, as shown in Figure 1: see original paper. These diodes were physically reconstructed using a reference approach identical to the one used to model the output buffer, based on the electrical characteristic curves of the clamp diodes derived from the IBIS model data. The hybrid model perfectly satisfies our demand for modeling the TID effect of a CMOS digital IC because it can operate effectively at various voltages without any operating point limitations and can integrate the TID effect model of a MOSFET.

I/O-port circuits are more sensitive to TID effects than core circuits. This is because I/O-port circuits typically include components such as input buffers and output drivers, which are often designed with small dimensions and thin-film structures, making them more susceptible to radiation. Additionally, a large contact area and concentration of electric fields between the port circuits and external devices further increase the probability of radiation-induced ionization

effects.

Therefore, this study focuses on the TID effect on the input/output ports of a component. The aim is to estimate the degradation of electrical characteristics of the output port caused by the TID effect by applying a hybrid model that considers the TID effect on MOSFETs with ports.

[Figure 2: see original paper] shows the modeling method of the TID effect for digital components based on the IBIS model, which can be divided into three phases: modeling the golden effect, modeling the TID effect, and simulation and analysis. The details of each phase are as follows:

(1) Modeling of the Golden Effect. This phase is divided into three sub-phases. In the first sub-phase, the input buffer data within the IBIS model of the digital device were preprocessed to produce characteristic curve data representing the V-I characteristics of the diodes in the input buffer. Subsequently, the physical characteristic parameters of the diodes in the input buffer were extracted using their physical equations. In the second sub-phase, the output buffer data within the IBIS model of the digital component were processed to generate characteristic curve data representing the V-I characteristics of the transistors in the output buffer. The physical characteristic parameters of the transistors in the output buffer were extracted using their physical equations.

After the first and second sub-phases, the specific parameter values of the diodes and transistors in the I/O buffer can be obtained. The characteristic parameters were then described as input and output buffer models using VHDL-AMS. Based on the datasheet of the digital component, the logical function of the component is described as a functional model in the third sub-phase using VHDL.

By the end of the first phase, the three previously mentioned models were integrated into the golden model of the digital component, which is based on the input and output buffer models, as well as the functional model. The resulting model takes the form of an executable program file that can implement the behavioral function of the digital component while also reflecting the physical characteristics of the ports. The delay information in the golden model was obtained by consulting the device datasheet.

(2) Modeling of the TID Effect. The second phase of the proposed TID effect-modeling method is the reconstruction of the golden model generated in the first phase. In this phase, TID variables are added to the golden model based on the influence of TID effects on CMOS digital components, including threshold voltage drift, carrier mobility degradation, and timing degradation, to describe the impact of TID on CMOS digital components and create a complete TID effect model of the digital component.

The threshold voltage and carrier mobility for the TID effect were extracted from measured V-I curves, whereas the delay information for the TID effect was obtained from measured V-T curves.

(3) Simulation and Analysis. Simulation and comparative analysis of the

TID model constituted the third phase. In this phase, the TID model was loaded into the SystemVision simulation environment, and simulation results were generated. The simulation results were then compared with experimental results to verify the accuracy of the modeled results and feasibility of the proposed method.

Data Pre-Processing and Feature Extraction

1. Characteristic Curve of the Clamp Diode at the Input Port The power-clamp data within the IBIS model describe the voltage-current relationship of the input port when input voltage V_{in} surpasses the component supply voltage V_{CC}. During this period, as shown in Figure 3: see original paper, the input port ground-clamp diode reverses to cutoff, whereas the power-supply clamp diode conducts forward.

Given that the reverse current of the diode is significantly smaller than its forward conduction current and that the input buffer inverter-gate leakage current is negligible, it can be assumed that this dataset corresponds to the V-I characteristic curve of the power-supply clamp diode. Notably, the IBIS model indicates that voltage V_{table} within the power-clamp data table adheres to the following relationship:

$$V_{table} = V_{CC} - V_{in}$$

where V_{CC} is the power supply voltage and V_{in} is the voltage of the input pin. When analyzing the V-I characteristics of a power-supply clamp diode, the corresponding voltage V should be obtained using the following transformation:

$$V = V_{in} - V_{CC} = -V_{table}$$

Similarly, the GND Clamp refers to the voltage and current characteristics of the input pins when the input voltage is below the GND level. During this moment, the power-clamp diode reverses, and the ground-clamp diode conducts forward (Figure 3: see original paper). Consequently, the GND Clamp data represent the V-I characteristic curve of the ground-clamp diode.

Voltage V_{table} in the GND Clamp data table has the following relationship according to the IBIS model:

$$V_{table} = V_{in} - V_{GND}$$

where V_{GND} is the voltage of the ground. Thus, to extract the V-I characteristics of the ground-clamp diode, voltage V must be obtained using the following transformation:

$$V = V_{GND} - V_{in} = -V_{table}$$

2. Characteristic Curve of the Transistor at the Output Port The driver inverter and ESD-protection circuit are the major components of the output port of a digital component. Different types of output buffers exist, such as push-pull, I/O, and open-drain buffers. Each buffer type has a different circuit structure and function, resulting in different V-I curves. An illustration of the fundamental push-pull output is presented along with an explanation of methods to extract the transistor characteristic curve for the port circuit. Notably, this extraction approach is also applicable to other buffer types with minor modifications as required.

The pullup curve shows the voltage-current relationship of a pin when the output state is set to one. The pull-up PMOS is enabled at this time, whereas the pulldown NMOS is disabled. A scan voltage in the range of $-V_{CC}$ to $2V_{CC}$ was applied to the output pin to obtain the voltage-current relationship. According to the IBIS model, voltage V_{table} described in the pullup datasheet is defined as:

$$V_{table} = V_{CC} - V_{out}$$

To extract the output characteristics of the pullup PMOS, the V-I data must be obtained within the $-V_{CC}$ to V_{CC} range of the output pin voltage V_{out}, which corresponds to the $2V_{CC}$ to 0 V interval of the pullup curve. Figure 3: see original paper shows the state of the output port during this period.

In addition, the IBIS output-buffer model pulldown data can be used to determine the pulldown curves of NMOS and power-clamp diodes. The pulldown curves show the relationship between voltage and current of the pin when the output state is set to zero. During this period, the pullup PMOS is disabled, and the pulldown NMOS is enabled. Subsequently, scan voltages ranging from $-V_{CC}$ to $2V_{CC}$ were applied to the output pin to determine the voltage-current relationship. The data between 0 and $2V_{CC}$ is captured on the pulldown curve. The voltage and current at the output pin were observed at this stage, as shown in Figure 3: see original paper.

Feature Extraction

1. Extract Model Parameters of Clamp Diode In the previous section, we discussed a method for obtaining the electrical characteristics of transistors using the IBIS model. The following section focuses on the method for selecting a suitable physical model of the transistor for parameter extraction.

The model equation for a diode based on semiconductor physics [31] can be expressed as follows:

$$I_D = I_s(e^{\frac{V_D}{nV_T}} - 1)$$

where I_s represents the reverse-saturation current with a typical value ranging from 10×10^{-6} A to 20×10^{-6} A; V_D is the junction voltage, which equals the diode terminal voltage minus the parasitic resistance drop; V_T is the thermal voltage constant with a typical value of 25.8 mV at 25°C; and n represents the emission coefficient.

The reverse-saturation current I_s, emission coefficient n, and parasitic resistance R govern the DC behavior of a diode. Modeling only the essential parameters while leaving other parameters at their default values is acceptable.

To obtain the values of parasitic resistance R, emission coefficient n, and reverse-saturation current I_s, reference point coordinates were first selected from the forward characteristic curve of the diode. These coordinates were substituted into the diode equation to determine the parameter values.

In this study, a classic digital component CMOS non-inverting multiplexer, NC7SZ157, was used as an example to demonstrate the modeling process. The golden parameter values of the diode for NC7SZ157 were obtained using the diode characteristic parameter-extraction technique along with a datasheet search, as listed in . These values were established as part of this study. Notably, when analyzing the IBIS model of NC7SZ157, the power-clamp diode was not included. Therefore, only the ground-clamp diodes are listed in . The input model parameters for the TID effect were extracted using the same method based on measured IBIS experimental data.

2. Extract Model Parameters of a MOSFET (i) Threshold Voltage V_{th}

The threshold voltage is the turning point for formation of the inversion layer in MOS components, and a conduction channel is formed when the gate voltage exceeds the threshold voltage. Numerous methods exist for extracting MOSFET threshold voltage, such as linear extraction, constant current, leakage current second-order derivative, transconductance extraction, Y-function, and beta-function methods [32, 33]. In this study, the linear extrapolation method was chosen for threshold voltage extraction because of its suitability for components with different channel lengths and its ability to make full use of transistor output characteristics.

The linear extrapolation method is based on the principle that when V_{ds} is small, MOSFET output characteristics can be expressed as:

$$I_{ds} = \frac{W}{L}\mu_n C_{ox}(V_{gs} - V_{th})V_{ds}$$

where W is the gate width, μ_n is the carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and L is the gate length. For a given V_{ds}, drain current I_{ds} depends linearly on gate voltage V_{gs}. The straight line with the steepest slope can be identified by extrapolating the component transfer characteristics. The intersection of this line with the horizontal axis (V_{gs}) indicates the threshold

voltage. The point with maximum slope is chosen because subthreshold current dominates when V_{gs} is small, whereas carrier mobility decreases with increasing gate voltage when V_{gs} is large.

(ii) Saturation Voltage V_{sat}, Saturation Current I_{sat}, Conductance Parameter K_n, and Channel-Length Modulation Coefficient V_A
When the MOSFET operates in the linear region, the relationship between drain voltage and current is as follows [10]:

$$I_{ds} = \frac{W}{L}\mu_n C_{ox}\frac{(2(V_{gs}-V_{th})-A_{bulk}V_{ds})}{1+\frac{V_{ds}}{E_c L}}$$

where A_{bulk} is the body charge effect coefficient and E_c is the critical electric field for velocity saturation.

To extract the values of saturation voltage V_{sat}, saturation current I_{sat}, conductance parameter K_n, and channel-length modulation coefficient V_A, reference point coordinates are selected from the linear region of the output characteristic curve of the MOS transistor. These coordinates are substituted into the equation to obtain parameter values.

Consequently, the parameters associated with the short-channel model of the MOSFET were successfully extracted. The extracted NC7SZ157 output buffer golden model parameters are listed in ($V_{gs} = 3.3$V). The output model parameters for TID effect were extracted using the same method based on measured IBIS experimental data.

Modeling the TID Effect of a CMOS Digital IC

1. Effect of Ionizing Radiation on the Electrical Properties of MOS Components The TID effect causes two types of charge traps to form within the oxide of MOS components [34, 37]: fixed oxide charge (N_{ot}) and interface-trapped charge (N_{it}). These charges are responsible for changes in the electrical behavior of components, resulting in events such as threshold voltage drift and carrier mobility degradation.

According to recent studies, the threshold voltages of NMOS and PMOS tend to decrease with increasing TID. However, NMOS exhibits a rebound effect at higher doses [35]. In addition, the TID effect results in decreased carrier mobility of the MOS device and hence decreased transconductance. Because carrier mobility attenuation profoundly affects MOS device transconductance and current-handling capability, this effect requires careful consideration when analyzing TID effects in MOS devices [36, 37].

Changes in threshold voltage and carrier mobility can affect the conduction resistance of the transistor at the component output, increasing the transition time. This occurs during a rising-edge transition when the NMOS transistor is

gradually turned off and the PMOS transistor is gradually turned on. The transition time of the waveform is related to the conduction resistance of the PMOS transistor and the size of the load capacitor. The TID effect causes negative drift in the threshold voltage of the PMOS and a decrease in channel carrier mobility, which increases the on-state resistance, leading to an increased time constant of the RC circuit formed by this equivalent resistance, port parasitic capacitance, or load capacitance, and a longer rise time. During a falling-edge transition, the PMOS transistor gradually turns off, the NMOS transistor gradually turns on, and the parasitic or load capacitance is discharged through the NMOS transistor. TID irradiation can cause both the threshold voltage and carrier mobility of the NMOS transistor to decrease, and because the effects of these two parameters on conduction resistance are opposite, their mutual cancellation results in a less pronounced change in the falling-edge waveform compared to the PMOS transistor with varying TID.

2. Behavior-Physical Hybrid Model of CMOS Digital IC In this study, a CMOS non-inverting multiplexer, NC7SZ157, was used as a case study to illustrate the process of creating a hybrid model, as shown in Figure 1: see original paper and [Figure 2: see original paper]. The golden functional area, input buffer, and output buffer models of NC7SZ157 were developed as the first steps of this process.

(i) Modeling of Functional Area

The functional domain of the behavioral-physical hybrid model of the digital IC pertains to the description of the logic function of the component being investigated along with its digital behavior. The complexity of this module varies depending on the function and size of the device being studied. Constructing the model as a separate and callable module facilitates readability and future modifications, which is highly recommended. To illustrate this concept, the NC7SZ157 datasheet was used to describe the functional area in VHDL, as indicated in Algorithm 1. The input ports in Algorithm 1 are denoted as S, I0, and I1, respectively, while Z denotes the output port of NC7SZ157.

Algorithm 1: Behavior model of functional for NC7SZ157

```
1 Define an entity called "multiplexer," which has inputs S, I1 and I0, and output Z of type
2 Begin the architecture "behav" for the entity "multiplexer"
3 Beginning a process sensitive to changes in the signals S, I1, and I0
4 If the value of signal S equals a high-level '1', then
5 Assign the value of the signal I1 to the output Z. If the value of the signal S equals the
6 Assign the value of the signal I0 to the output Z
7 End the architecture
```

(ii) Modeling of Input Port

Based on the model parameters in , a physical model of the input port for NC7SZ157 was designed using VHDL-AMS, as shown in Algorithm 2.

Algorithm 2: Physical model of input port for NC7SZ157

```
1 We define the electrical terminals VCC, P_{in}, n1, n2, and out,
2 Instantiate an entity called "Diode" with the name Diode1
3 Set generic parameters for Diode1: Isat = 2.18E-28, R = 1.14, n = 1.0
4 Instantiate an entity called "Inductor" with the name L_{pkg}
5 By setting the generic parameters for L_{pkg}: L = 1.01E-9
6 Instantiate an entity called "Resistor" with the name R_{pkg}
7 By setting the generic parameters for R_{pkg}: R = 32E-3
8 Instantiate an entity called "Capacitor" with the name C_{pkg}
9 By setting the generic parameters for C_{pkg}: C = 0.13E-12
10 Connecting ADC to n2 and out
```

(iii) Modeling of Output Port

The physical model of the output port for NC7SZ157 was designed using VHDL-AMS, as shown in Algorithm 3, based on the model parameters listed in .

Algorithm 3: Physical model of output port for NC7SZ157

```
1 We define the electrical terminals as VCC, P_{in}, P_{out}, and out,
2 Instantiate an entity called "PMOS" with the name PMOS1
3 Set generic parameters for PMOS: Vth = -0.6, B = -20, Kn = 0.01496, Va = -11.62, Abulk = 1
4 Instantiate an entity called "NMOS" with the name NMOS1
5 We set the generic parameters for the NMOS: Vth = 0.5, B = 5.5, Kn = 0.02191, Va = 40.66,
6 Instantiate an entity called "Diode" with the name Diode1
7 Set generic parameters for Diode1: Isat = 6.59E-11, R = 21, n = 2
8 Instantiate an entity called "Diode" with the name Diode2
9 Set generic parameters for Diode2: Isat = 5.918E-14, R = 0.2158, n = 1.14
10 Instantiate an entity called "Inductor" with the name L_{pkg}
11 By setting the generic parameters for L_{pkg}: L = 0.91E-9
12 Instantiate an entity called "Resistor" with the name R_{pkg}
13 By setting the generic parameters for R_{pkg}: R = 32E-3
14 Instantiate an entity called "Capacitor" with the name C_{pkg}
15 By setting the generic parameters for C_{pkg}: C = 0.13E-12
16 The DAC is connected to Do and P_{in}
```

The functional area should be combined with the input and output port models to form a golden model of the component. Figure 4: see original paper shows the simulation results of the golden model using SystemVision software. The golden delay can be obtained from the component datasheet (the propagation delays from I0, I1, and S to Z are 3.2 ns). The propagation delay is defined as the measurement starting when 50% of the rising or falling edge of the input signal arrives and ending when 50% of the rising or falling edge of the output signal is reached, as shown in [Figure 4: see original paper]. The simulation parameters are as follows: input I0 is set to state '0' , I1 is set to state '1' , the input clock is set to 50 MHz, and the output load is set to 1 kΩ. A comparison of the datasheet and simulation results confirms that the logic function of the developed model is accurate and that the model is capable of reproducing the analog electrical characteristics of the port.

3. Time Degradation Modeling To accurately simulate the impact of TID on digital combinational and sequential logic, timing degradation must be considered, which can cause changes in circuit propagation delay and even disrupt sequential logic function. As shown in Algorithm 4, it is necessary to reconstruct the functional domain of the hybrid model and introduce pin-to-pin signal propagation delay to model the propagation delay.

Algorithm 4: Timing degradation model of the functional area for NC7SZ157

```
1 If the value of signal S equals a high-level '1', then
2 Check whether signal I1 has changed (i.e., if it has had an event): The current value of I
3 If the signal S changes, then Assign the current value of I1 to signal Z after a delay of
4 If neither I1 nor S change, then The current value of I1 is assigned to signal Z. End the
5 If the value of the signal S equals the low level '0', then
6 Check whether signal I0 has changed (i.e., if it has had an event): The current value of I
7 If the signal S changes, then Assign the current value of I0 to signal Z after a delay of
8 If neither I0 nor S change, then The current value of I0 is assigned to signal Z. End the
```

In Algorithm 4, `delay_{I1}`, `delay_{I0}`, and `delay_s` are introduced as three parameters representing the pin-to-pin signal propagation delay from input ports I1, I0, and S to output port Z. The pre-radiation delay can be obtained from the component data. TID experiment results show that the propagation delay of NC7SZ157 in the S-Z path is 3.2 ns at 0 krad(Si), 3.9 ns at 50 krad(Si), and 4.3 ns at 100 krad(Si). The simulation results are presented in Figure 4: see original paper.

From Figure 4: see original paper, it is clear that the signal transmission delay gradually increases as TID increases. It can be concluded that the above model accurately represents the radiation-induced timing degradation of the component. Therefore, the proposed modeling method is feasible.

4. Modeling TID Effect of Output Port The effect of TID on the output port can be modeled by considering two key factors: the TID-induced effect on the threshold voltage and carrier mobility of the port transistor, as described in the introduction regarding TID effects on digital devices. To demonstrate the feasibility of this modeling approach, a CMOS output inverter circuit was constructed, as shown in Figure 5: see original paper, in the SystemVision simulation environment.

In Figure 5: see original paper, the load capacitance C_1 and resistance R_1 were set to 2 pF and 1 kΩ, respectively. The simulation results shown in Figure 5: see original paper demonstrate that the electrical characteristics of the pull-up PMOS can be changed by adjusting the threshold voltage and carrier mobility. The conduction cases one through four reflect an increase in the threshold voltage of the PMOS and a decrease in the carrier mobility of the PMOS. It can be observed that with an increase in threshold voltage and a decrease in carrier mobility of the pull-up PMOS, the PMOS on-resistance increases, leading to an

increase in the rise time of the level at the output pin V_{out} and a decrease in the high-level amplitude. Therefore, inclusion of the TID effect on the output pin threshold voltage and carrier mobility in the model allows representation of TID-related variation in CMOS device port characteristics.

It is noteworthy that the four conduction cases shown in Figure 5: see original paper are intended to verify the TID effect modeling method, in which the threshold voltage (V_{th}) and conductance parameters (k_n) are added to the port. During modeling of the TID effect, the threshold voltage (V_{th}) and conductance parameter (k_n) of the device at different dose points were extracted by measuring the transfer characteristic curve of the transistor at the port in TID experiments. Subsequently, the extracted V_{th} and k_n are used as generic parameters for Algorithm 3 to obtain simulation results for the TID effect at the port, as shown in [Figure 7: see original paper].

Experiments and Results

Experimental Setup

To verify the TID effect modeling method for CMOS digital ICs proposed in this study, an experimental circuit for a CMOS non-inverting multiplexer, NC7SZ157, was set up. Subsequently, the TID experiment was conducted at the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences. The experimental board and TID experimental environment are shown in [Figure 6: see original paper]. The experimental conditions are presented in .

When measuring experimental data, the I0 pin of NC7SZ157 was set to '0', the I1 pin was set to '1', and a 40 kHz square wave signal was applied to the S pin to measure the IBIS model and V-T waveform data of the output port Z at different dose points. The IBIS model primarily includes the V-I curves of the port diode and transistor, which are used to extract the characteristic parameters of the diode and transistor and are substituted into Algorithms 2 and 3 as generic parameters for simulations. The V-T curve was compared with simulation results, as shown in [Figure 7: see original paper]. It can be observed that the rise time t_r and fall time t_f of both simulation and experimental results increase with increasing TID. The rise time t_r and fall time t_f refer to the times required for the output voltage of a component to change from 10% to 90% and from 90% to 10%, respectively.

The edge times of the experimental results are compared with those of the simulation results in . It can be seen that t_r and t_f increase with increasing TID. The relative error between experimental and simulation results was calculated using the V-T data shown in [Figure 7: see original paper]. The relative error is defined as the average ratio of the difference between experimental and simulation results to the experimental results for voltage values within one period. The obtained relative errors were 0.2%, 0.6%, and 1.4% for dose points 0 krad(Si), 50 krad(Si), and 100 krad(Si), respectively.

The results show that the model accurately reflects the effect of TID on the CMOS digital IC. also shows that the experimental results at 50 krad(Si) are close to the simulation results at 0 krad(Si) and that the experimental results at 100 krad(Si) are close to the simulation results at 50 krad(Si). This was due to the limited accuracy of the SystemVision simulation environment. In future studies, we aim to enhance the accuracy of the model and simulation to achieve a closer match between simulation and experimental results.

In addition, all simulations were completed in less than 1 s, indicating the high efficiency of the model.

Conclusion

This study proposes a three-phase TID effect modeling method for CMOS ICs based on the IBIS model to address problems raised by transistor-level modeling when evaluating TID effects in digital ICs. In the first phase, a golden model of a digital IC was developed. The transistor characteristic curves of the input and output buffers were processed using the IBIS model of the component, and the physical parameters of the input and output ports were extracted using diode and MOS physical equations. The VHDL language was used to model the functional areas of the components according to the truth table in the datasheet. The golden digital IC model was developed by combining the port and functional area models. In the second phase, the golden model was reconstructed based on TID effects on CMOS threshold voltage drift, carrier mobility degradation, and timing degradation to form the final TID effect model of the digital IC. In the third phase, TID effect experiments were conducted using a CMOS non-inverting multiplexer, NC7SZ157, as an example. The 40 kHz waveform information of the NC7SZ157 output was measured at 0 krad(Si), 50 krad(Si), and 100 krad(Si), and the IBIS model was obtained to extract feature parameters. The TID effect model was then loaded into the SystemVision environment for simulation. Finally, simulation and experimental results were compared, which indicated that the relative error between simulation and experimental results at each dose point was less than 2%. Thus, the feasibility and accuracy of the proposed modeling method were confirmed. The TID effect of other CMOS digital ICs can be simulated using this modeling method to evaluate their ability to tolerate TID effects.

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Note: Figure translations are in progress. See original paper for figures.