Research and Practice on Radiation Effects Assessment Methods for Design Hardening of Aerospace Integrated Circuits Postprint

Authors: Zheng Hongchao, Wang Liang, Li Zhe, Guo Gang, Zhao Yuanfu

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Abstract

Aerospace integrated circuits are core components of space electronic systems, and radiation hardening technology is the core technology that ensures the reliable operation of aerospace integrated circuits in space environments. As circuit feature sizes shrink to the nanometer scale, single-event effects have gradually become the primary factor limiting the radiation hardness capability of aerospace integrated circuits. The team from Beijing Microelectronics Technology Institute has adopted design hardening as the technical route for the development of radiation-hardened aerospace integrated circuits. Based on extensive single-event test data obtained from heavy ion accelerators, they have proposed new test and evaluation methods for single-event effects in new processes and devices, conducted research on test and analysis techniques and radiation effect mechanisms, provided accurate fundamental information for hardening technology research, verified the effectiveness of design hardening techniques, revealed the mechanisms of single-event radiation damage, provided guidance for optimizing hardening, and ultimately provided critical support for the formation of highly reliable, long-life aerospace integrated circuit products.

Full Text

Preamble

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Development and Application of a Radiation Effect Evaluation Method for Aerospace Integrated Circuits Hardened by Design

ZHENG Hongchao[1],[2], WANG Liang[1],[2], LI Zhe[1],[2], GUO Gang[3], ZHAO Yuanfu[1],[2]

[1](Beijing Microelectronics Technology Institute, Beijing 100076, China)

[2](Laboratory of Science and Technology on Radiation-Hardened Integrated Circuits, China Aerospace Science and Technology Corporation, Beijing 100076, China)

[3](Institute of Nuclear Physics, China Institute of Atomic Energy, Beijing 102413, China)

Abstract

Aerospace integrated circuits are core components of space electronic systems, and radiation hardening technology is the key to ensuring their reliable operation in space environments. As integrated circuit feature sizes shrink to the nanometer scale, single-event effects have gradually become the most critical factor limiting the radiation-hardened performance of aerospace integrated circuits. The Beijing Microelectronics Technology Institute team has adopted radiation-hardened-by-design as the technical route for developing radiation-hardened aerospace integrated circuits. Based on extensive single-event test data obtained from heavy-ion accelerators, the team has proposed new evaluation methods for single-event effects in novel processes and devices, conducted research on testing techniques and radiation effect mechanisms, and provided accurate foundational information for hardening technology research. This work has validated the effectiveness of design-hardening techniques, revealed single-event radiation damage mechanisms, and offered guidance for optimization, ultimately providing critical support for the development of high-reliability, long-lifetime aerospace integrated circuit products.

Keywords: Aerospace integrated circuit, Single-event effect, Radiation hardened by design, Radiation test

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Integrated circuits in spacecraft electronic systems experience radiation effects in space environments, including single-event effects, total ionizing dose effects, and displacement damage. With advances in semiconductor technology and shrinking device feature sizes, single-event effects have become the dominant radiation effect impacting spacecraft electronic systems. Statistics show that single-event effects account for 68.9% of operational anomalies in low-orbit satellites. In 2012, Los Alamos National Laboratory observed an FPGA on a satellite, finding that single-event events occurred at an average rate of 14.4 times per day, severely affecting normal satellite operations and flight safety.

Single-event effects occur when individual protons or heavy ions traverse an integrated circuit, depositing charge along their track through direct ionization, nuclear reactions, or secondary particles produced by elastic collisions, thereby causing circuit malfunctions. Based on their consequences, these effects can be classified into two categories: "functional" errors that change digital logic states or analog signals, such as single-event upsets (SEU), single-event transients (SET), and single-event functional interrupts; and "electrical" errors caused by transient conductive channels formed in parasitic transistors, leading to latchup or burnout, such as single-event latchup, single-event burnout, and single-event gate rupture.

Currently, there are three primary hardening approaches against single-event effects in integrated circuits: shielding hardening, process hardening, and design hardening. Shielding hardening uses packaging materials to absorb and block radiation, which can reduce electron and proton radiation but is ineffective against heavy-ion single-event effects. Process hardening employs specialized processes or modifications to standard process lines to achieve hardening without compromising normal performance, but at higher cost. Design hardening, implemented on standard commercial process lines through layout-level, circuit-level, and system-level techniques, reduces single-event effect probability through temporal and spatial redundancy. This approach effectively improves single-event hardening capability at lower cost, though it requires additional chip area and power consumption. Unlike the United States, which primarily relies on process hardening for aerospace integrated circuits, China's radiation-hardened process technology lags significantly behind international levels and cannot meet the demands of increasingly complex space missions. However, the gap between China's commercial process lines and foreign radiation-hardened process lines is relatively small. Therefore, the Beijing Microelectronics Technology Institute team pioneered a design-hardening technical route in China, achieving independent controllability of aerospace integrated circuits based on commercial processes. The team established standard cell libraries and I/O libraries, as well as IPs including phase-locked loops, SRAM (Static Random Access Memory), and high-speed interfaces, building an ultra-deep submicron and nanometer-scale radiation-hardened integrated circuit development platform. The prerequisite for developing design-hardening solutions is understanding radiation effect mechanisms, particularly single-event effects. Heavy-ion testing and evaluation methods based on ground-based single-event simulation facilities are critical enablers for design hardening.

Domestic integrated circuit single-event performance evaluation is typically conducted at the HI-13 terminal of the Beijing Tandem Accelerator Nuclear Physics National Laboratory or the TR5 terminal of the Lanzhou Heavy Ion Accelerator National Laboratory to obtain target circuits' single-event error cross-sections and linear energy transfer (LET) thresholds. These results are then used to estimate in-orbit single-event error rates based on orbital parameters, environmental models, and sensitive volume models. Existing industry standards for single-event testing only specify general procedures without providing specific

test methods for different circuit types. With process advances, complex circuits featuring high-speed signals, embedded large-capacity memory, and system-on-chip architectures require new testing methods and techniques to provide foundational information for radiation-hardening technology through experimental means.

This paper summarizes the team's technical breakthroughs over more than a decade, presents single-event hardening techniques proposed for radiation-hardened design, elaborates on research achievements in radiation effect evaluation methods and testing techniques for aerospace integrated circuits based on domestic accelerators, and presents research conclusions.

Case Studies in Single-Event Hardening Design for Integrated Circuits

Radiation-hardened-by-design against single-event effects can employ layout-level structures such as well contact guard rings and layout separation to improve single-event latchup hardening capability and reduce multiple-bit upset (MBU) and multiple-cell upset (MCU) probabilities. Circuit-level techniques include spatio-temporal redundancy structures such as DICE (Dual Interlocked Storage Cell) to improve SET and SEU hardening capability. System-level hardening includes error detection and correction coding and triple modular redundancy. However, with nanometer process advances, single-event testing has revealed that these traditional hardening methods are insufficient for effectively mitigating SET, MBU, and MCU. Consequently, the team has proposed improved optimized designs for memory elements sensitive to upsets, such as flip-flops and memory cells.

1.1 Single-Event Hardening Design Case 1—Flip-Flop Design Hardening

In very large-scale integrated circuits, combinational logic circuits are predominant and most susceptible to single-event effects that generate SETs, which can propagate to sequential elements such as flip-flops and cause functional failures. Redundant Delay Filter (RDF) is a common structure for filtering external SETs, as shown in Figure 1: see original paper. However, radiation test results indicate that under conditions of shrinking nanometer process dimensions, increasing circuit scale, and higher operating frequencies, there remains a significant probability of capturing large SETs.

The team designed a novel flip-flop circuit structure called RDFD (Redundant Delay Filter DICE) that combines RDF with dual DICE [9], as shown in Figure 1: see original paper. This structure employs DICE to improve SEU hardening threshold and utilizes RDF to desynchronize SETs introduced at the front end under dual independent outputs, preventing them from overwriting the dual-modular-redundant DICE latch and thus significantly reducing the flip-flop's SET capture probability.

1.2 Single-Event Hardening Design Case 2—Memory Design Hardening

Memory is a critical component in very large-scale integrated circuits for storing instructions or performing computations. The DICE structure is a commonly used circuit-level method for memory SEU hardening, but its weakness lies in the existence of SEU-sensitive node pairs. With process advances, the charge-sharing region from a single event can simultaneously cover sensitive node pairs, or cover them during ion oblique incidence. Therefore, sensitive node pairs should be properly laid out during cell layout design.

The team proposed an Error Quenching Double DICE (EQDD) memory cell layout hardening technique [10]. This approach utilizes the charge-sharing quenching effect between non-sensitive nodes within the same DICE cell to reduce SET impact range, then employs cross-layout design between adjacent DICE cells, as shown in [Figure 2: see original paper]. By increasing the spacing between two sensitive nodes within the same DICE, this technique effectively reduces the probability of SEU occurrence in DICE sensitive node pairs and improves MBU and MCU hardening capability without increasing overall memory layout area.

Single-Event Effect Evaluation Methods

The team has developed multi-core processors (CPUs), ten-million-gate application-specific integrated circuits (ASICs), and gigahertz high-speed high-precision analog-to-digital converters (ADCs) on the radiation-hardened-by-design platform. Evaluating advanced-process integrated circuits, high-speed circuits, and complex chips is key to obtaining radiation effect mechanisms and effectively assessing product radiation-hardened capability. Through years of effort and exploration, the team has proposed single-event evaluation test methods for new processes, structures, and effects.

2.1 Evaluation Method for Single-Event Soft Errors in Complex Large-Scale Circuits

Complex large-scale circuits such as CPUs and ASICs have multiple operating modes and test vectors. Exhaustive testing of all modes would require over 100 hours of single-event accelerator time per circuit, which is impractical and inefficient. Therefore, a method to identify the worst-case operating mode for single-event characterization is needed.

In 2008, the team first utilized Design for Test (DFT) to evaluate single-event soft error performance in complex large-scale circuits. By conservatively assuming that any SEU occurring in a memory cell would cause functional interruption, this approach obtains single-event soft error performance metrics for complex circuits. Common built-in self-test designs typically include flip-flop scan chains and Memory Built-In Self Test (MBIST) modes. [Figure 3: see original

paper] shows the single-event error Weibull curves for an ASIC under testability and different functional modes. The single-event error cross-section under DFT mode is more conservative and can characterize the worst-case single-event soft error performance of complex circuits.

The MBIST method uses multiplexers (MUX) to switch ASICs from functional mode to DFT mode, enabling detection of SEUs in all internal SRAMs. A generator simulates SRAM write and read operations, while a comparator determines whether soft errors have occurred, as shown in [Figure 4: see original paper]. Since written data will overwrite SEUs and cause error loss, the team proposed an effective irradiation fluence calculation method, as shown in [Figure 5: see original paper] [11]. For each SRAM address, the effective irradiation time for SEU is the duration between the first write operation and the last read operation within each write cycle. By summing the effective irradiation times for all SRAM addresses and calculating their proportion ( ) of total irradiation time, the total irradiation fluence (ϕT) multiplied by yields the effective total irradiation fluence (ϕE). Additional irradiation fluence (ϕT - ϕE) must be applied to the target circuit to calibrate SEU detection, solving the accuracy issues of the MBIST method in SEU testing.

2.2 Evaluation Method for High-Speed Signals

New-generation communication satellites require real-time processing of massive data acquired on-orbit, necessitating single-event testing of gigahertz ADCs and bus controllers. High-speed signals can be categorized into parallel and serial types. High-speed parallel signals are typically tested in static or low-speed dynamic modes that cannot cover full-scale voltage output patterns. In 2012, the team proposed a high-speed signal single-event upset analysis technique based on folding interpolation [12]. By providing high-frequency input and clock signals with a specific frequency difference, a low-frequency full-scale sampling matrix is obtained at the output, as shown in [Figure 6: see original paper]. Dual FIFO high-speed buffering enables continuous SEU processing, with captured SEU patterns shown in [Figure 7: see original paper].

High-speed serial signals, commonly used in bus data transmission, are susceptible to single-event functional interrupts (SEFI) and SEUs, producing various error types at the receiver. Single-event bit error rate is a critical metric for high-speed serial signals. Traditional statistical methods that directly compare code patterns are prone to misjudgment and accuracy issues. In 2018, the team proposed a classification algorithm for statistically analyzing single-event interrupt and upset bit error rates [13], as shown in Equation (1), where FER and UER represent in-orbit error rates for single-event interrupts and upsets, respectively, and TRST is the number of code words corresponding to system reset time.

The total daily error rate is calculated as: (FER $\times$ TRST + UER $\times$ 1 bit) / Total Data per day. FER is calculated based on the number of unrecover-

able single-event functional interrupts. UER encompasses three types of upsets: single-bit errors (S1), multi-bit errors (S2), and self-recovering errors (S3). The SEU bit error count is calculated as shown in Equation (2), where Tburst is the number of code words corresponding to self-recovery time.

$$SEU = S1 + S2(i) + S3 \times Tburst$$

2.3 Evaluation Method for Flip-Chip Packaged Circuits

With increasing clock frequencies and pin counts in aerospace circuits, flip-chip packaging with high density, high performance, and high reliability has been widely applied in advanced circuits such as CPUs, FPGAs, and ASICs. Flip-chip circuits typically have substrate thicknesses exceeding several hundred micrometers. The range of heavy ions produced by medium-low-energy accelerators generally cannot penetrate the substrate for testing. Foreign approaches use high-energy accelerators to produce ultra-high-energy heavy ions above 10 GeV to increase range while reducing ion LET values, thereby penetrating flip-chip circuits. However, domestic high-energy accelerator beam time is limited and cannot meet the demands of large-scale circuit testing. After years of exploration, the team has proposed a single-event testing procedure for flip-chip circuits based on medium-low-energy accelerators.

Flip-chip circuits require substrate thinning before single-event testing to control substrate thickness. The effective LET value of ions reaching the chip active region must be calculated to ensure the entire penetration process through the active region remains on the right side of the Bragg peak, guaranteeing test accuracy. [Figure 8: see original paper] shows SEU cross-sections for two ASIC circuits with the same process but different packaging. The SEU cross-section for chlorine ion (Cl) irradiation of flip-chip circuits is smaller than that for silicon ion (Si) because the effective LET value of Cl ions after incidence crosses the left side of the Bragg peak, while Si ions remain on the right side with higher effective LET, as shown in [Figure 9: see original paper].

2.4 Proton Single-Event Evaluation Method

The maximum LET value of protons in silicon through direct ionization is approximately 0.538 $MeV \cdot cm^2/mg$ [14], which is insufficient to affect hardened integrated circuits. However, nuclear reactions between protons and target materials produce secondary heavy ions with LET values up to 14 $MeV \cdot cm^2/mg$ (with silicon) and even 37 $MeV \cdot cm^2/mg$ (with tungsten). Considering that nanometer integrated circuits generally have low single-event soft error LET thresholds, proton single-event effects cannot be ignored. Before the establishment of the intermediate-energy proton single-event test terminal at the China Institute of Atomic Energy, domestic proton test beam time was limited and energy adjustment was difficult. The mechanism of proton single-event effects lacked experimental data support and verification, and no testing method standards existed, necessitating preliminary research on evaluation techniques.

In 2016, the team first experimentally verified that nanometer SRAMs could experience SEUs caused by direct ionization from low-energy protons. The SEU cross-section of non-hardened SRAMs formed a curve similar to the Bragg peak, as shown in [Figure 10: see original paper]. Through comparative analysis with heavy-ion test results, the team found that proton SEUs in hardened SRAMs primarily originated from secondary heavy ions produced by nuclear reactions, as shown in [Figure 11: see original paper].

Single-Event Effect Testing and Analysis Techniques

To improve single-event testing efficiency and data analysis capability, the team has also developed efficient test system equipment based on accelerators and proposed new test data analysis methods.

3.1 Matrix Automatic Measurement Control System

To meet the demands of high-efficiency testing for batch single-event testing, the team developed a matrix automatic measurement control system for HI-13 [15], as shown in [Figure 12: see original paper]. The system's core components are a matrix controller and relay matrix network. Through host computer programs, it can achieve second-level switching between different test systems, automatically completing reset, test, and save commands. The system also standardizes power supply and communication links, enabling simultaneous control of up to 30 test systems for single-event testing. The on-site installation at HI-13 is shown in [Figure 13: see original paper]. The vacuum chamber simultaneously contains single-event test systems for CPUs, ASICs, ADCs, SRAMs, and BUS circuits. Through a translation stage, each circuit can be sequentially aligned with the irradiation port, and combined with the control system, rapid single-event testing of different circuits can be achieved.

[Figure 14: see original paper] shows the SEU cross-section of a flip-flop operating at 100 MHz under three pattern types: "all-0," "all-1," and "01 alternating." The "all-1" and "01 alternating" patterns exhibit obvious single-event multi-upset (SEMU) phenomena, indicating that single-event events occurred in global signal modules such as clock trees, providing guidance for designers to improve hardening design.

3.2 Time-Domain Analysis Method

Traditional single-event test data processing methods plot SEU cross-sections as Weibull curves for analysis. [Figure 14: see original paper] shows single-event Weibull curves for a flip-flop circuit operating at 100 MHz measured under three pattern types [9]. The team observed that SEU data varied abnormally between different modes, with results differing by an order of magnitude. Curve analysis alone cannot distinguish SEU distribution characteristics in the time domain or locate error sources. Therefore, the team proposed a time-domain analysis method that can differentiate SEUs, as shown in [Figure 15: see original paper].

At each LET ion value, SEU error counts can be plotted as a function of test time, revealing the temporal distribution characteristics of SEUs.

Since 2005, when the team first conducted single-event testing at a tandem accelerator, they have accumulated over 1,100 hours of single-event beam time over 18 years, completing testing on more than 500 circuits. This work has provided invaluable experimental data support for radiation-hardened design technology research, proposed multiple evaluation methods and testing techniques, pioneered a radiation-hardened-by-design technical route with Chinese characteristics, built a complete product portfolio of aerospace integrated circuits, and developed the capability to provide systematic chip solutions for aerospace engineering. Key core circuits have operated normally on-orbit for many years, solving single-event failure problems that plagued aerospace applications and contributing significantly to the long-term stable operation of space vehicles.

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Author Contributions

ZHENG Hongchao and WANG Liang were responsible for methodology and investigation; ZHENG Hongchao and LI Zhe were responsible for systems and testing; GUO Gang and ZHAO Yuanfu were responsible for conceptualization.

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