Towards real-time digital pulse process algorithms for CsI(Tl) detector array at External Target Facility in HIRFL-CSR Postprint

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Abstract

A fully digital data acquisition system based on a field-programmable gate array (FPGA) was developed for a CsI(Tl) array at the External Target Facility (ETF)in the Heavy Ion Research Facility in Lanzhou(HIRFL). To process the CsI(Tl) signals generated by γ-rays and light-charged ions, a scheme for digital pulse processing algorithms is proposed. Every step in the algorithms was benchmarked using standard γ and α sources. The scheme, which included a moving average filter, baseline restoration, leading-edge discrimination, moving window deconvolution and digital charge comparison was subsequently implemented on the FPGA. A good energy resolution of 5.7% for 1.33 MeV γ rays and excellent α-γ identification using the digital charge comparison method were achieved, which satisfies CsI(Tl) array performance requirements.

Full Text

Preamble

Towards Real-Time Digital Pulse Processing Algorithms for the CsI(Tl) Detector Array at the External Target Facility in HIRFL-CSR

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A fully digital data acquisition system based on a field-programmable gate array (FPGA) was developed for the CsI(Tl) array at the External Target Facility (ETF) of the Heavy Ion Research Facility in Lanzhou (HIRFL). To process CsI(Tl) signals generated by γ-rays and light-charged ions, a scheme for digital pulse processing algorithms is proposed. Each step in the algorithms was benchmarked using standard γ and α sources. The scheme, which included a moving average filter, baseline restoration, leading-edge discrimination, moving window deconvolution, and digital charge comparison, was subsequently implemented on the FPGA. An energy resolution of 5.7% for 1.33 MeV γ rays and excellent α-γ identification using the digital charge comparison method were achieved, satisfying the performance requirements of the CsI(Tl) array.

Keywords: CsI(Tl) array, on-line digital algorithms, moving average filter, moving window deconvolution, on-line particle identification algorithms

Introduction

The structure of atomic nuclei near drip lines is one of the most fascinating fields for nuclear physicists and has continuously attracted researchers to build large facilities for experimental studies [1, 2]. One such facility is the External Target Facility (ETF) at the Heavy Ion Research Facility in Lanzhou (HIRFL) [3]. The ETF is a large integrated experimental platform for nuclear physics research that comprises several detector systems and can provide complete kinematic measurements of nuclear reactions at intermediate and high energies [3–7]. The CsI(Tl) array, consisting of 1024 CsI(Tl) detectors, is one of the most important detector systems in the ETF, capable of measuring γ-rays up to 10 MeV in the center-of-mass frame [8]. This design—an inorganic scintillation array with high granularity—is also used in many other detector arrays, such as DALI2 at RIKEN [9, 10] and CALIFA at FAIR [11, 12], and enables relatively good energy resolution for γ-rays owing to its excellent angular resolution [10].

In combination with silicon strip detectors, the CsI(Tl) array at the ETF can also measure light-charged particles. However, the energy loss of light-charged particles in CsI(Tl) crystals is several tens of times greater than that of γ-rays. To satisfy the highly dynamic requirements of these measurements, the electronic system was updated. High-granularity detectors require highly integrated electronics [13–16]. The traditional solution, also known as the previous scheme of the CsI(Tl) array, uses application-specific integrated circuit (ASIC) chips for signal processing [17]. However, these chips are highly customized and difficult to extend. Waveform digitization based on flash analog-to-digital converters (ADC) has been developed for over two decades, where analog signals extracted from the detector or charge-sensitive amplifier (CSA) are directly digitized, enabling minimal signal information loss using a much simpler circuit. Other advantages include higher sustained count rates, flexibility through various digital pulse processing (DPP) algorithms, and compact structures that facilitate the development of highly integrated systems. Owing to these advantages, a fully digital technique was chosen as the solution for the new measurement system for the CsI(Tl) array.

However, this scheme has one drawback: digitization of the entire waveform generates a significant amount of data. For a single-channel signal digitized by a 14-bit flash ADC with a sampling frequency of 50 MS/s, the data rate is approximately 83.4 MByte/s. When this flash ADC is used for the CsI(Tl) array at the ETF, the total data volume becomes extremely large, potentially overloading the transmission bandwidth of the Data Acquisition (DAQ) system. Zero suppression should therefore be performed after waveform digitization to reduce data transmission pressure. Using DPP algorithms in the onboard FPGA to extract specific waveform information, such as amplitude and arrival time, can reduce the entire waveform sampling dataset to a few physical quantities, further decreasing data volume. Moreover, due to conflicts between the FPGA's limited computational resources and the large number of detector channels, the new electronic system may require a compromise in precision with relatively simple DPP algorithms, which are the focus of this study.

The remainder of this paper is organized as follows: Section II concentrates on general considerations regarding which procedures should be executed in the FPGA and in what order. Section III lists the specific DPP algorithms for each procedure and discusses the rationale for algorithm selection through bench testing. Section IV presents the final DPP algorithm scheme in the FPGA and discusses performance after implementing all algorithms. Section V summarizes the study findings and outlines future research directions.

II. General Consideration of DPP Algorithms

In nuclear physics, signals from detectors are completely random, indicating that DPPs for the CsI(Tl) array should perform well in the time domain [18]. As a calorimeter, the critical physical quantity measured by the CsI(Tl) array is the energy of incident gamma rays or light ions. Thus, the method for obtaining energy information from the recorded detector waveform is the most critical aspect of this study, and energy resolution is a key criterion for DPP algorithms. Additional algorithms such as smoothing filters and baseline recovery were used to achieve good signal-to-noise ratio (SNR) values and energy resolution. Signal arrival-time information is responsible for generating a system trigger and helps reduce background noise by selecting appropriate time windows for off-line data analysis [19].

CsI(Tl) crystals have been used for many years to identify light ions and gamma rays through pulse-shape analysis because the response of CsI(Tl) crystals varies with different particle types, resulting in different waveform shapes [20–24]. In the case of a CsI(Tl) array with high spatial coverage and large granularity, gamma rays and light ions can strike different detector elements simultaneously and form different hit clusters. When the energy spectrum is reconstructed using algorithms such as the add-back technique, the spectra from charged particles and gamma rays may become superimposed. Thus, clear separation of gamma rays and charged particles can produce a good gamma energy spectrum with lower background from charged particles. Pulse-shape analysis can improve particle identification (PID) performance compared to the traditional ΔE-E method [25].

In some situations, when the atomic number Z of the measured ions is less than four, pulse shape analysis can also help simplify the detector setup because the CsI(Tl) detector can perform identification by itself [26–28]. Considering these advantages, on-line algorithms for pulse shape analysis are also in demand.

[Figure 1: see original paper]

Overall, in this study, DPP algorithms are organized in the FPGA as shown in Figure 1. The final outputs are the arrival time, energy, and quantities representing the incident particle PID results. Each process shown in Figure 1 is described in detail in the following sections.

III. Algorithm Selections with Off-Line Analysis

To identify suitable algorithms for each process shown in Figure 1, a test bench including a CsI(Tl) array element and the DAQ system was set up. The DAQ system is an intermediate development product of the CsI(Tl) array that contains a CSA module and a DAQ board. A 14-bit flash ADC with a sampling rate of 50 MS/s was embedded in the DAQ board to digitize signals from the CSA module. The DAQ board can operate in two modes: raw waveform mode, where flash ADC data are recorded directly into PC memory, and algorithm mode, where data are processed by algorithms in the FPGA with only results recorded. Because the DPP algorithms were not specified, the test bench was operated in raw waveform mode to select appropriate algorithms for the CsI(Tl) array. The criteria for selecting suitable algorithms are based on the trade-off between performance, FPGA resource consumption, and execution speed. The flash ADC sampling rate was set to 25 MS/s in the FPGA because the data volume was too large for raw waveform mode.

A. Smooth Filter

Because detector signals are always distorted by random noise, the goal of this procedure is to reduce high-frequency noise while not significantly altering the detector signals to preserve signal characteristics and improve SNR. This procedure was performed first because it may slightly alter the raw waveform and affect the performance of other procedures.

The moving average filter (MAF) is the most commonly used smooth filter in the time domain due to its simplicity, ease of implementation, and rapid execution speed. In addition to these advantages, it offers the lowest noise for a given edge sharpness among any linear filter [18]. Other optional filters include Savitzky–Golay [29], binomial [28, 30], Whittaker [31], and Kalman filters [32, 33]. Although these smooth filters perform well in multiple fields such as Raman and Mössbauer spectroscopy, their complex algorithms make them difficult to implement in the FPGA. For this reason, the MAF was chosen as the smooth filter for the CsI(Tl) array.

The only parameter for MAF is the number of samples averaged. Its value should be chosen carefully because as the value increases, noise decreases while edges become less sharp. The aforementioned test bench, operated using cosmic rays, was used to acquire raw waveform data, and MAF algorithms were executed with different parameter values in off-line analysis. The results are presented in Figure 2 [Figure 2: see original paper]. The reason for using powers of two for parameter values is that division is simpler to implement in the FPGA using only shift operations. Finally, due to its good performance in high-frequency noise reduction and minimal waveform changes, the parameter value was set to 8.

B. Baseline Restoration

In many cases, the baseline is assumed constant at all times, enabling the baseline value to be measured at any time while the DAQ system was idle during the experiment. However, this assumption is only valid when the signal length is short and the count rate is relatively low. This is certainly not the case here because the CSA signal extracted has a long tail. A good solution is to use optimal filters [34]; however, complicated arithmetic discourages further development. To simplify the procedure, it was assumed that the baseline remained constant within each selected dataset, which contained only one signal waveform with several baseline data points in front. This baseline data can subsequently be used to calculate the baseline value of each individual event. Reference [35] showed that two values—the average and median of the baseline data—can be used to evaluate the baseline level. The method for obtaining average baseline data is straightforward. The median is the exact middle quantity in the baseline dataset when ordered. Reference [35] showed that the median is a better estimate of the baseline level than the average over a wide range of count rate loads.

The other two methods, called "averaging over the selection set" and "averaging over the flat chunk selection set" respectively, are also introduced in [35]. These two methods are identical in procedure but differ in data selection. Further details regarding both methods can be found in [35], and the main procedures are summarized in the flowchart shown in Figure 3 [Figure 3: see original paper]. Over a wide range of count rate loads, these two methods provide better baseline estimates than either the average or median alone.

In this case, because the baseline dataset has already been selected, the procedure listed in Figure 3 can be processed directly. Therefore, both methods are treated as a single method and are hereafter called iterative methods.

There are three methods: the average of the baseline dataset, median of the baseline dataset, and the iterative method. To evaluate performance, baseline samples in the data used in the previous section were processed using these methods. The results of baseline restorations are shown in Figure 4 [Figure 4: see original paper]. The discrete and continuous histograms are displayed using the median and average methods, respectively, because the data types for these two methods are “int” and “float.” The histogram obtained using the iterative method is similar to that obtained using the median method. The only difference is the width of each discrete part, which equals twice the minimum difference parameter set in the algorithm (δz in Figure 3; here the value is 0.1; further details can be found in [35]). Gaussian functions were used to fit the envelopes of the three histograms; the results are listed in Table 1 . Because the data are all integers for the median method, the most probable value (MPV) of the histogram is treated as zero and not the mean fitting parameter. From a comparison of the MPVs of the three methods, it can be concluded that all three methods are good estimators of baseline levels and therefore fully meet performance requirements.

Algorithm complexity subsequently becomes the focus of selection criteria. The iterative method was the most complex of the three methods. However, this method is powerful because it can continue to provide reasonable baseline values when signal samples are also included in the dataset [35]. The median method is simpler, although the data ranking algorithm is not “FPGA friendly.” Therefore, for the CsI(Tl) array DAQ system, the average method is preferred.

C. Arrival Time

According to the ETF design scheme, the CsI(Tl) array was intended to generate a trigger for the entire system. With complete digitization of the input waveform and the powerful calculation capability of the FPGA, the CsI(Tl) array trigger signal can be generated and controlled by software. This simplifies the electronic system by eliminating the need for additional electronics such as splitters and time discriminators.

An ETF trigger system consists of 2-level trigger generators [36]. At the front end, primary trigger signals are generated according to signal shapes and logical relationships between readout elements of a particular detector included in the trigger system. These primary trigger signals are subsequently fed into the global trigger logical unit to generate an event trigger signal for the entire system according to physical interests. To improve logic operation effectiveness for signals with different delay times and time jitter, each primary trigger signal can be delayed and widened separately in a global trigger logical unit. From this perspective, time resolution is not the key element for the CsI(Tl) array.

Several methods are available to determine signal arrival time. Common methods, identical to those in analog schemes, are leading-edge discrimination (LED) and constant fraction discrimination (CFD). LED is the simplest method; however, it has large time jitter due to the time-walk effect. To achieve better performance, correction should be performed, which is a significant task for the FPGA programmer. Therefore, CFD was introduced to eliminate the time walk effect. There are two methods for implementing this algorithm in an FPGA: constant-fraction zero-crossing (CFDzc) and digital constant-fraction discrimination (dCFD) [37]. CFDzc is a digital version of the classic analog CFD [38], whereas dCFD is similar to LED with a different threshold value equal to a constant fraction of the signal amplitude [39]. Better performance in terms of time resolution was obtained with the CFDzc method than with the dCFD method [40]. Other methods exist for determining signal arrival time, such as the RC-CR^2 filter [41] and pulse-shape fitting; however, utilization of these algorithms is resource-intensive in the FPGA and considered outside the scope of this research.

Because time resolution is not the key criterion for the CsI(Tl) array, the LED method without interpolation was chosen to determine arrival time, considering the expected high computational resource consumption of energy extraction and PID procedures. Figure 5 [Figure 5: see original paper] shows the relationship between waveform amplitude and arrival time using previous data. The arrival time is the difference between the reference time and the time when the first sample point exceeds the threshold. The time reference was selected as the point at which the ADC waveform passed through 90% of its full amplitude at the leading edge. Linear interpolation was used to reduce reference time jitter. A clear dependency between waveform amplitude and arrival time is shown in Figure 5. Another phenomenon is that the lower the waveform amplitude, the greater the time jitter. This occurs because low amplitude causes the leading edge of the waveform to become flat, making it difficult to determine when the waveform crosses the threshold and the time reference. Although time jitter is as large as approximately 3 µs when waveform amplitudes are extremely small, this may not be problematic because a threshold can be set in the FPGA to determine which signals are recorded. The time jitter of waveforms with relatively large amplitudes was approximately 342 ns (the σ value with a Gaussian fit).

Further analysis can be performed with time-walk correction, which was not implemented in the FPGA in the proposed scheme. A cubic polynomial, shown in Figure 5 with a red solid line, was used to fit the 2D histogram. The arrival time histograms with and without time-walk correction are shown in Figure 6 [Figure 6: see original paper]. Good correction can be obtained for small waveforms, and the time jitter is approximately 344 ns (the σ value with a Gaussian fit), which is almost identical to the value obtained for large waveforms.

D. Energy

In general, two quantities are used to extract energy loss from the detector: signal amplitude and total charge. These quantities were measured using ADCs and charge-to-digital converters (QDCs) in conventional DAQ systems. Using a digital approach, these measurements are replaced by appropriate algorithms in the FPGA. However, the signal extracted from the CSA was too wide, indicating that the digital QDC method was not suitable for the CsI(Tl) array.

The most direct approach to extract signal amplitude is to determine the maximum (positive signal) or minimum (negative signal) of the waveform. However, measured amplitudes were significantly influenced by noise. To improve energy resolution, digital filters—which perform the same function as shaping amplifiers in analog measurement systems—were used to shape the signal before amplitude extraction. Theoretically, the best signal shape that maximizes SNR is the infinite-width cusp [42]; however, a practical filter of this type is the finite-width cusp filter that limits amplitude measurement of a single signal to a specific time. The algorithm uses a different function instead of an infinite exponential function and performs truncation [43, 44], which means performance is reduced. Other commonly used shaping filters include a series of trapezoidal CR-RC filters [45–51] and CR-RC filters [52–54]. To identify a suitable shaping filter, γ-rays produced by a ^{60}Co source were measured on a test bench operating in waveform mode, and recorded data were processed with various digital filters. Waveforms before and after applying shaping filters are shown in Figure 7 [Figure 7: see original paper]. All parameters in each filter were optimized through repeated trials. Energy resolutions of the full-energy peaks for 1.33 MeV γ-rays were calculated as the criterion, and results are shown in Table 2 . Energy resolutions achieved by each filter were comparable, with the finite cusp filter performing slightly better. This is because the noise in the output test was extremely low, and SNR values did not improve significantly. It should be noted that the noise level in the test is of the same order of magnitude as that of the ETF, indicating that all filters meet requirements in terms of performance.

Reference [55] concludes that the family of trapezoidal filters offers good performance and simpler implementation among many shaping filters, which influenced this choice. Many algorithms exist for implementing trapezoidal filters, of which moving-window deconvolution (MWD) [49–51] is the simplest for FPGA implementation. Therefore, the MWD filter was selected as the shaping filter for the CsI(Tl) array, and the corresponding ^{60}Co energy spectrum is indicated by the red dashed line in Figure 12 [Figure 12: see original paper].

E. PID Algorithms

As previously mentioned, performing pulse shape analysis for the CsI(Tl) array can reduce the background of charged particles in the γ-ray energy spectrum and improve PID performance when combined with the ΔE-E method. The basis of pulse shape analysis is that the ratio of fast and slow components of light generated by the CsI(Tl) crystal depends on the type of incident particles, resulting in different output waveform shapes. Multiple methods exist for extracting these differences, among which digital charge comparison [56–59] and rise-time comparison methods [59, 60] are widely used and straightforward to implement in the FPGA. Another method worth focusing on is reconstructive particle identification (RPID) [51]. One reason is that this method was developed for CALIFA, whose construction is similar to the CsI(Tl) array. The RPID method can be successfully migrated into the DAQ system with significant potential. Another reason is that RPID can directly extract the fast and slow components of the CsI(Tl) crystal, thereby achieving improved performance.

To compare these PID algorithms, a triple α source (^{244}Cm, ^{239}Pu, and ^{241}Am) and a ^{60}Co source were used separately to irradiate the elemental detector of the CsI(Tl) array under identical conditions. The CsI(Tl) crystal envelope was pierced with a small hole to allow α-particles to access the crystal. For the digital charge comparison method, because input signals are extracted from the CSA, which results in information on incident particles being contained in the leading edges of digitized waveforms, both time windows for charge integration were set to include the leading edge of the waveform with the same starting point, as shown in Figure 8 [Figure 8: see original paper]. The starting point is determined using the dCFD method without interpolation. The integration window size was determined through repeated trials. For the rise-time comparison method, rise time is defined as the time frame between points where waveforms cross 12.5% and 87.5% of full amplitude in the leading edges. Because method performance correlates with time accuracy, linear interpolation was used to determine cross-points. For the RPID method, some parameters are identical to those of the MWD filter previously described, with three additional parameters: the fast and slow decay times of the CsI(Tl) crystal and the time window for the second MWD procedure. The fast and slow decay times are in accordance with [51] because they are almost constant. The length of the second time window was determined through repeated trials.

Two-dimensional PID spectra for each method are shown in Figure 9 [Figure 9: see original paper]. Superficially, α and γ-rays are well identified for all three methods. The spectrum in Figure 9(a) illustrates that rise time and waveform amplitude are weakly correlated and can be considered independent. The red dashed lines in Figures 9(b) and 9(c) indicate that spectra approach zero when both horizontal and vertical axes are reduced. These relationships indicate that PID parameters listed in Table 3 can be used to convert two-dimensional spectra into one-dimensional histograms, and the figure-of-merit (FoM), as defined in [61, 62], can be used to quantify separation performance of the PID methods. These one-dimensional histograms are shown in Figure 10 [Figure 10: see original paper] and relevant FoMs are illustrated. Although data in low-energy regions, which can make FoM values larger than those in beam experiments, were not included, the FoM values shown in Figure 10 remain good references for evaluating these three methods.

Of the three methods, rise-time comparison achieved the worst score, consistent with results in [28]. This is because the accuracy of rise time deteriorated as input signal amplitude decreased. Surprisingly, the RPID method does not work as well as the digital charge comparison method. One reason is the approximate treatments in the algorithm implementation process, such as calculating the exponential function. Moreover, it was identified that the decay time of the fast component in the CsI(Tl) array depends on the type of incident particles (more precisely, on the average energy density deposited in the crystal) [22, 63] and even on the total energy of particles [20, 21], while the slow component decay time does not. If this is the case, RPID may not be an accurate method because of the underlying assumption of constant decay time. However, this remains sufficient for separation of γ-rays and light-charged particles.

Overall, the aforementioned descriptions support the conclusion that the digital charge comparison method is preferred due to its good performance and ease of FPGA implementation. Performance of the RPID method lags slightly; however, the complexity of this algorithm rules this option out. The rise-time comparison method had the worst performance among the three methods; however, the result remains acceptable, making it an alternative option to the digital charge comparison method.

IV. Final Scheme and Performance of DPP Algorithms in the FPGA

Considering these points, the final DPP algorithm scheme, which includes a moving average filter, baseline restoration, leading-edge discrimination, moving window deconvolution, and digital charge comparison, is formed. Thus, the diagram in Figure 1 can be improved as shown in Figure 11 [Figure 11: see original paper]. All DPP algorithms are “FPGA friendly,” and further simplification can be achieved for the MAF and MWD by converting the algorithms to recursive form. The algorithms were implemented in the DAQ system FPGA, completing the algorithm mode. The sampling rate was reset to 50 MS/s because the amount of data is significantly reduced. Subsequently, all procedures in Figure 11 were retested in this mode with the same radioactive sources used in Section III.E.

The energy spectra are shown in Figures 12 and 13. A small shift can be observed between the two energy spectra of the ^{60}Co source compared to the result obtained in raw waveform mode. This is due to rounding operations in the FPGA algorithm and changes in DAQ system sampling frequencies. However, the energy resolutions for the 1.33 MeV full-energy peak are almost unchanged.

The performance of PID with the on-line algorithms is shown in Figure 14 [Figure 14: see original paper]. Compared with the same results obtained from raw waveform mode shown in Figure 10, almost identical positions where peaks of PID parameters are located can be found using the rise-time and charge comparison methods. There is a slight improvement in the FoM parameter when comparing charge comparison methods. This is due to improvement in DAQ system sampling frequency. For the rise-time method, the FoM parameter shows little difference. The reason for this is the rounding operation for the final result in the FPGA. Therefore, it can be concluded that only minimal performance difference exists between on-line and off-line DPP algorithms.

Table 4 lists key performance metrics for the proposed algorithm. Good energy resolutions and PID performance are achieved, indicating that the on-line algorithms in the FPGA are well formed, and the final DPP algorithm scheme can adequately meet requirements.

V. Summary

In this study, a scheme for DPP algorithms was developed for the CsI(Tl) array at the ETF. A test bench with α and γ sources was constructed to determine algorithms for each step, resulting in the following final scheme: moving average filter, baseline restoration, leading-edge discrimination, moving window deconvolution, and digital charge comparison. Subsequently, the DAQ system algorithm mode was completed using these DPP algorithms. It was identified that performance does not change significantly between on-line and off-line algorithms. With the algorithm mode, good performance in energy spectrum and PID, as listed in Table 4, is achieved, which indicates that the proposed DPP algorithm scheme meets requirements to upgrade the CsI(Tl) array DAQ system at the ETF of HIRFL-CSR.

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Note: Figure translations are in progress. See original paper for figures.