A low dead time vernier delay line TDC implemented in an actel flash-based FPGA Postprint

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Date: 2023-06-18T00:00:00+00:00

Abstract

In this paper, a high precision vernier delay line (VDL) TDC (Time-to-Digital Convertor) in an actel flash-based Field-Programmable-Gate-Arrays A3PE1500 is implemented, achieving a resolution of 16.4-ps root mean square value or 42-ps averaged bin size. The TDC has a dead time of about 200 ns while the dynamic range is 655.36 s. The double delay lines method is employed to cut the dead time in half to improve its performance. As the bin size of the TDC is dependent on temperature, a compensation algorithm is adopted as temperature drift correction, and the TDC shows satisfying performance in a temperature range from –5°C to +55°C.

Full Text

Preamble

A Low Dead Time Vernier Delay Line TDC Implemented in an Actel Flash-Based FPGA

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Abstract
This paper presents a high-precision vernier delay line (VDL) time-to-digital converter (TDC) implemented in an Actel flash-based FPGA A3PE1500, achieving a resolution of 16.4 ps root mean square (RMS) and an average bin size of 42 ps. The TDC features a dead time of approximately 200 ns and a dynamic range of

655.36 s. A double delay lines method is employed to halve the dead time and improve performance. Since the TDC bin size is temperature-dependent, a compensation algorithm is adopted for temperature drift correction, demonstrating satisfactory performance across a temperature range from –5°C to +55°C.

Key words
Time measurement, Vernier, Time-to-digital converter, Double delay lines, Compensation

Introduction

Time-to-digital converters (TDCs) implemented in field-programmable gate arrays (FPGAs) offer a flexible, low-cost solution for measuring time-of-flight (TOF) in particle physics and plasma experiments. In SRAM-based FPGAs, the delay line interpolating method employing dedicated carry elements can achieve 50 ps resolution with 10 ns dead time. In Actel flash-based FPGAs, using buffers as delay elements yields 540 ps resolution, which can be improved to 130 ps by eliminating buffers and utilizing only routing lines.

Single-event effects (SEE) testing has demonstrated that Actel flash-based FPGAs exhibit superior single-event immunity compared to SRAM FPGAs, making them suitable for space missions requiring radiation tolerance. However, unlike SRAM FPGAs, flash-based FPGAs lack dedicated carry lines, and the shortest delay through a logic block is hundreds of picoseconds. Consequently, achieving dozen-picosecond resolution using time interpolating methods is challenging in flash-based FPGAs.

The Vernier Delay Line (VDL) method has been utilized in various time-to-digital converter application-specific integrated circuits (ASICs). Unlike vernier TDCs using crystal oscillators of different frequencies, TDCs employing vernier tapped delay lines provide higher resolution, larger dynamic range, and shorter dead time. Since the propagation delay of vernier elements depends on temperature and voltage, voltage control circuits and delay-locked loops (DLL) are integrated to ensure TDC bin size stability. However, such circuits are not available in FPGAs, resulting in few reports of FPGA-based vernier delay line TDCs.

This paper implements a high-resolution TDC combining the VDL method and time interpolating technique in an Actel flash-based FPGA A3PE1500. A “double delay lines” method is employed to halve the dead time, and a temperature compensation algorithm enables operation across a wide temperature range. The architecture design and performance tests are described below.

2.1 Vernier Time Interpolating Architecture

The FPGA core of the A3PE1500 consists of 38,400 VersaTiles that can be configured as three-input logic functions, D-flip-flops, or latches through programming appropriate flash switch interconnections. VersaTiles exhibit propagation

delays when used as different combinatorial cells. In our design, the propagation delay difference between AND3 and MUX2 units serves as VDL elements, theoretically forming a Vernier TDC with an average bin size of less than 50 ps.

The VDL block diagram is shown in Fig.1. The architecture employs a time-stamp vernier TDC based on a coarse counter and interpolator units formed by VDL. Simulation results indicate that the propagation delay difference between AND3 and MUX2 units leads to a minimum bin size of approximately 50 ps. The leading signal for the vernier lines is the "hit" pulse, while the lagging signal is generated by a D-flip-flop fed by the hit pulse and master clock. The interval measured by the vernier delay line is actually the time between the hit event and the subsequent clock rising edge.

With a master clock period of 10 ns, the time-stamp TDC provides a wide measurement range of approximately 655.36 s using a 16-bit coarse time counter, expandable by increasing the counter bit width. The encoder unit converts the fine time information from the VDL into 9-bit data. The Read-Out FIFO stores integrated TDC data, including 16-bit coarse time data, 9-bit fine time data, and TDC channel ID. "Read En" serves as the read enable signal for the coarse counter latches and encoder unit.

[Figure 1: see original paper]

Figure 2 shows the timing diagram for generating the "Read En" pulse. When a hit signal arrives, a D-flip-flop at the proximal clock rising edge generates the lagging signal. At the next clock rising edge, another D-flip-flop latches the lagging signal to output a reverse pulse. Both the lagging signal and reverse pulse feed into an AND2 gate, producing a "Read En" signal. This generated signal, synchronous to the hit signal with one clock period duration, can be used as the coarse counter reading enable signal and fed to the encoder unit for VDL output fine data reading enable and FIFO writing enable after several clock periods of delay.

[Figure 2: see original paper]

2.2 Double Delay Lines Method

The dead time in vernier delay line TDCs is maximally required for the lagging signal to overtake the leading signal, depending on the number of delay cells and single-cell propagation delay. A single vernier delay line covering a 10 ns clock period contains approximately 300 propagation delay combinatorial cells, resulting in dead time close to 200 ns.

A "double delay lines" method is employed to achieve shorter dead time. As shown in Fig.3, because the clocks feeding the two VDLs have the same frequency with inverted phase, the lagging signals for both delay lines are generated with a half-clock-period time difference. Both vernier delay lines cover slightly more than half a clock period, reducing the required number of cells by half and decreasing dead time to 100 ns.

Each hit signal is measured by both delay lines, but only one of the two output codes is selected as the valid time information based on the fine time data from both vernier delay lines. The clocks for the double delay lines are generated using two methods: two internal PLL cores of the FPGA with inverted phases, and both rising and falling edges of the master clock. Test results compare TDC performance between these two clock generation methods.

[Figure 3: see original paper]

3 Test Results

In 2012, a prototype incorporating a vernier delay line TDC in an Actel flash-based FPGA was designed and tested. Figure 4(a) shows the TDC board with a Universal Serial Bus (USB) port, while Fig.4(b) illustrates the testing block diagram.

[Figure 4: see original paper]

3.1 Bin Size and Differential Non-Linearity

In this design, the TDC bin size equals the propagation delay difference between AND3 and MUX2 units. Differential non-linearity (DNL) primarily results from disproportionate widths of vernier delay chain cells. DNL is defined as the deviation of bin size from its ideal least significant bit (LSB) value, while integral non-linearity (INL) represents the deviation of the input/output curve from the ideal transfer characteristic—a straight line fitting the curve best. The code-density test method was adopted to characterize TDC non-linearity.

Figure 5 presents code-density test results for a single-chain vernier TDC. Since non-linearity repeats every 10 ns, a look-up table (LUT) can be constructed from INL information to compensate TDC outputs. Figure 5(a) shows bin size information for a single vernier delay chain in the A3PE1500, with an average of approximately 42 ps. The first bin, larger than others, causes the worst TDC non-linearity. This oversized bin results from the D-flip-flop generating lagging signals. When the hit signal arrives coincident with the clock rising edge, an ambiguous state occurs, producing a slower rising edge for the lagging signal. In code-density tests, these slower lagging signals accumulate in one bin, creating an ultra-wide bin. Due to this 135 ps bin, DNL ranges from –1 to +2.2 LSB, and INL ranges from –1.4 to +3.7 LSB.

Figure 6 shows waveforms of the slower lagging signal. Bin size and non-linearity information for the vernier TDC using the double delay lines method are presented in Fig.7. The two lines cover slightly more than half a clock period, so hit signals arriving at the clock rising edge are tapped at both the start and end of one chain. By selecting the correct time information, the ultra-wide bin is eliminated from the TDC channel. DNL for the double delay lines vernier TDC ranges from –1 to +0.9 LSB, while INL ranges from –1 to +3.4 LSB. INL

non-uniformity results from disparity in average bin size between the two delay lines.

[Figure 5: see original paper]
[Figure 6: see original paper]
[Figure 7: see original paper]

3.2 Time Measurement Resolution

Resolution, a critical parameter for time measurement systems, can be obtained through "cable delay testing." However, cable length is limited because long cables attenuate input signals and slow the leading edge, introducing measurement errors. For measuring various time intervals, a dual-channel arbitrary function generator (Tektronix AFG3252) is employed to obtain resolution. Since the generator's two channels output correlated signals with adjustable delays, a wide range of time intervals can be tested.

An INL look-up table corrects INL errors. The single vernier delay line TDC exhibits resolution exceeding 50 ps RMS before INL compensation, improving to approximately 20 ps RMS after compensation. Figure 8 shows the time resolution of the vernier delay line TDC. When paired input hits originate from the same delay line, resolution is optimal; RMS degrades when outputting time codes from different delay lines. The two clocks generated by integrated FPGA PLLs exhibit stacked clock noise, resulting in worse resolution. Meanwhile, for the double delay lines TDC employing both rising and falling edges of the master clock, RMS remains around 20 ps. The single delay line vernier TDC performs similarly, though RMS increases by a few additional picoseconds. Thus, the double vernier delay lines TDC using both clock edges achieves the best time measurement performance.

The double vernier delay lines eliminate the ultra-wide bin from the TDC channel, yielding approximately 3.7 ps RMS improvement compared to the single delay line TDC (Fig.8(c)). When the time interval between paired input pulses falls within one clock cycle, measurement resolution is similarly constrained. Figure 9 shows time resolutions for intervals from 0 ns to 20 ns in 1 ns steps. All RMS curves repeat every 10 ns, equal to the clock period.

When the measured time interval equals N×T (where T is one clock period), the double delay lines TDC with inverted-phase clocks exhibits RMS below 20 ps after INL compensation. However, RMS degrades when measuring other time intervals. In other words, the TDC provides optimal precision when selecting output time codes from the delay line where the hit signal arrives at the clock rising edge. The double delay lines TDC using both clock edges demonstrates the best overall performance.

[Figure 8: see original paper]
[Figure 9: see original paper]

3.3 Bin Size Drifts

Vernier element delay times drift with ambient temperature changes. Bin size tests were conducted in a temperature control chamber (Fig.10). As ambient temperature varies from –5°C to +55°C, the TDC's average bin size increases from 39.8 ps to 44.5 ps. Cell delay varies linearly with temperature, yielding a calculated slope of approximately 0.0807 ps/°C. The functional relationship LSB = 39.6 ps + 0.0807 ps/°C × (T + 5°C) is obtained.

When the operating environment temperature changes rapidly, random errors can reach hundreds of picoseconds without temperature drift correction. Therefore, a compensation mechanism is necessary to correct tap delay for a given operating temperature. While look-up tables are typically regenerated using substantial memory space when ambient temperature changes, our temperature compensation algorithm requires only a single look-up table generated at –5°C.

The algorithm proceeds as follows: First, time information for each hit is corrected using the –5°C look-up table. Second, since TDC bin size varies with temperature, the LSB at the operating temperature is calculated, and a ratio is obtained by dividing this calculated LSB value by the –5°C value. Finally, time information is further corrected by multiplying by this LSB ratio.

Figure 11 shows resolution at different temperatures for 0 ns time intervals. RMS remains below 18 ps when using look-up tables generated at each temperature, while resolution degrades slightly when using the temperature drift compensation algorithm with the –5°C look-up table. This occurs because more vernier elements are occupied at lower temperatures due to smaller bin sizes, including more bin information. RMS increases modestly as operating temperature deviates from –5°C, but remains below 22 ps at worst. Thus, the temperature drift compensation algorithm offers better accuracy and convenience.

[Figure 10: see original paper]
[Figure 11: see original paper]

4.1 Coarse Counter

The 16-bit coarse counter operating at 100 MHz contributes a dynamic range of 655.36 s. Since Actel flash-based FPGAs lack dedicated carry lines, counters are formed from combinatorial cells. The counter's carry delay, contributed by cell propagation and routing line delays, must be confined within one clock cycle. Layout constraints aim to minimize routing delays by placing all counter combinatorial cells in a compact FPGA region.

4.2 Dead Time

To meet practical application requirements, the double delay lines method reduces vernier delay line TDC dead time. Using both edges of the master clock

decreases maximum dead time to 100 ns. The TDC channel disables during hit measurement. Dead time also exhibits temperature dependence, increasing by 10% when ambient temperature rises by 50°C.

4.3 Bin Size and Logic Resource Occupancy

TDC bin size depends on the time difference between the two macros selected as vernier cells. Bin sizes below 40 ps can be achieved by reselecting delay elements. However, shorter delay cells require more elements, increase dead time, complicate encoder logic, and demand higher clock frequencies. More elements increase logic resource occupancy, while higher clock frequencies risk timing integrity. Operating at 100 MHz, a two-channel vernier TDC using AND3 and MUX2 macros consumes approximately 25% of the A3PE1500's logic resources.

5 Conclusion

This paper reports a vernier delay line TDC based on time interpolating methods and implemented in an Actel ProASIC3E FPGA. A "double delay lines" method halves dead time and improves time measurement performance. A temperature drift compensation algorithm corrects for temperature variations, achieving 100 ns dead time, 655.36 s dynamic range, 16.4 ps RMS resolution, and 42 ps average bin size across a –5°C to +55°C temperature range.

Acknowledgments

The authors thank Tielong Zhang of the Department of Geophysics and Planetary Sciences at USTC and Stanislav Barabash of the Swedish Institute of Space Physics for helpful discussions and suggestions.

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Note: Figure translations are in progress. See original paper for figures.