Influence of channel length and layout on TID for 0.18 m NMOS transistors (Postprint)

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Abstract

Different channel lengths and layouts on 0.18 m NMOS transistors are designed for investigating the dependence of short channel effects (SCEs) on the width of shallow trench isolation (STI) devices and designing in radiation hardness. Results show that, prior to irradiation, the devices exhibited near–ideal I–V characteristics, with no significant SCEs. Following irradiation, no noticeable shift of threshold voltage is observed, radiation–induced edge–leakage current, however, exhibits significant sensitivity on TID. Moreover, radiation–enhanced drain induced barrier lowering (DIBL) and channel length modulation (CLM) effects are observed on short–channel NMOS transistors. Comparing to stripe–gate layout, enclosed–gate layout has excellent radiation tolerance.

Full Text

Preamble

Influence of Channel Length and Layout on TID for 0.18 m NMOS Transistors

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Abstract

We designed 0.18 m NMOS transistors with different channel lengths and layouts to investigate the dependence of short-channel effects (SCEs) on shallow trench isolation (STI) width and to develop radiation-hardened designs. Prior to irradiation, the devices exhibited near-ideal I-V characteristics with no significant SCEs. Following irradiation, no noticeable threshold voltage shift was observed; however, radiation-induced edge leakage current exhibited significant sensitivity to total ionizing dose (TID). Moreover, radiation-enhanced drain-induced barrier lowering (DIBL) and channel length modulation (CLM) effects were observed in short-channel NMOS transistors. Compared to stripe-gate layout, enclosed-gate layout demonstrates excellent radiation tolerance.

Key words: SCEs, DIBL, CLM, Enclosed-layout

Introduction

As channel length scales, the depletion regions of source and drain become comparable to the channel length, making some effects that were ignored in large-size MOS transistors—such as channel length modulation and drain-induced barrier lowering—become increasingly important. This necessitates dedicated research into these phenomena. Radiation-enhanced SCEs and DIBL effects in 0.6 m MOS transistors were reported by Luo Yihong and co-workers in 2010[4]. G.U. Youk and colleagues reported radiation-enhanced SCEs in devices with 0.35 m and 0.4 m channel lengths[5]. The influence of channel length on total ionizing dose effects in 0.18 m NMOS transistors has been reported by Hu Zhiyuan and colleagues[6,7]. In this work, we designed devices with different W/L ratios and gate layouts to investigate radiation-enhanced SCEs and compare the radiation tolerance of stripe-gate and enclosed-gate configurations.

2 Experimental Details

The NMOS transistors studied in this work were fabricated using a 0.18 m CMOS process with STI. The gate oxide thickness is 3.981 nm. Test chips were designed and fabricated, including stripe-gate layouts with channel lengths (L) of 20 m, 1.2 m, 0.5 m, and 0.18 m (all with width W = 20 m), and enclosed-gate layouts with L = 1.2 m and 0.18 m (W = 20 m). The operating voltage is 1.8 V. Devices were irradiated in a ^{60}Co gamma irradiation chamber at the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences. During exposure, the gates were biased at 1.8 V while all other pins were grounded. I-V characteristics were measured prior to irradiation and after incremental irradiation steps up to 100 krad(Si), 200 krad(Si), 300 krad(Si), and 500 krad(Si). All measurements were performed within 20 minutes after each exposure.

3 Results and Discussion

According to literature, susceptibility of gate oxide is reduced as its thickness scales; therefore, threshold voltage shift has not been a major concern. Although STI has become the dominant isolation technology for advanced CMOS processes, it remains sensitive to TID.

A. Radiation-Induced Leakage

The test transistors were irradiated up to a total dose of 500 krad(Si). [Figure 1: see original paper] shows the ID-VG characteristics for devices with different channel lengths. As can be seen, curves obtained after a total dose of 100 krad(Si) exhibit pronounced subthreshold leakage. When the total ionizing dose accumulated to 500 krad(Si), the drain current at VG = 0 V increased by approximately 5 orders of magnitude compared to the pre-irradiation value. The radiation-induced excess leakage current shows weak gate control, indicating that leakage is mainly due to parasitic transistors along the trench oxides[7,8]. Positive charge trapped in the lateral STI oxide can invert the channel and open a conductive path for leakage current between source and drain, turning on the parasitic transistors. As total dose increases, more oxide-trapped charges accumulate in the STI oxide, enhancing the leakage current. Since this leakage current is small compared to the main transistor current, it influences the subthreshold region of the ID-VG curve but not the above-threshold region, as shown in [Figure 1: see original paper].

B. Radiation-Enhanced Channel Length Modulation

[Figure 2: see original paper] shows the ID-VD characteristics of parasitic transistors with stripe-gate layout. Noticeable radiation-induced channel length modulation (CLM) effect was observed up to 500 krad(Si) for L = 20 m, while for L = 0.18 m it appeared at only 100 krad(Si), demonstrating radiation-enhanced CLM effects.

So we have, in saturation[9], where n is electron mobility, COX is unit area of gate oxide capacitance, W is gate width, L is channel length, VG is gate voltage, VT is threshold voltage, VD is drain voltage, and λ (λ = ((1 - Leff/L)/VD)) is the channel-length modulation coefficient. This phenomenon results in a nonzero slope in the ID-VD characteristic and hence a nonideal current source between drain and source in saturation.

[Figure 3: see original paper] shows the slope in the ID-VD characteristic as a function of total dose for parasitic transistors. Following irradiation, the slope increases, with shorter channel lengths exhibiting more severe effects. As previously mentioned, leakage current only influences the subthreshold region of the main transistor, which is related to the parasitic transistors, explaining the slope changes.

As is well known, the point at which the local density of inversion layer charge equals zero gradually moves toward the source as VD increases. We assume that Leff = L when VD = VG - VT, so Leff is eliminated as VD increases, i.e., Leff is eliminated as VT decreases.

Prior to irradiation, the threshold voltages of parasitic transistors are large enough to keep them off. Following irradiation, positive charges trapped in the lateral STI oxide create oxide-trapped charges, resulting in a negative shift of VT for parasitic transistors and eventual elimination of Leff. The shorter the channel length, the more serious the CLM effects. This phenomenon was found only in parasitic transistors and does not influence the effective channel length of main transistors, so it need not be heavily considered in analog integrated circuits where transistors operate primarily in saturation.

C. Effects of Drain Bias During Measurement

In short-channel NMOS transistors, punchthrough caused by drain-induced barrier lowering (DIBL) occurs at the surface or in the bulk. At the trench oxides, radiation-induced charge can escalate device punchthrough in three different ways[5]. [Figure 4: see original paper] illustrates pre- and post-irradiation ID-VG characteristics for devices with W/L = 20 m/20 m, 20 m/1.2 m, 20 m/0.5 m, and 20 m/0.18 m at different drain biases. As channel length shortens, pre-irradiation current-voltage curves show slight DIBL effects in the subthreshold region while exhibiting significant DIBL effects in saturation. Following irradiation, the subthreshold regions of the transistors show substantial radiation-induced DIBL effects, as seen in (a), (b), (c), and (d). This can be explained by charge sharing with the source and drain junctions.

On one hand, irradiation-induced positive oxide charges are quickly trapped in the STI oxide at the transistor edge. These charges raise the nearby body potential, lowering the potential barrier between drain and source and resulting in bulk punchthrough. On the other hand, positive charge trapped in the lateral STI oxide accumulates and eventually builds up a depletion region along the trench oxides, called parasitic depletion regions. The parasitic depletion region shortens the effective channel length through interactions with the drain and source depletion regions, meeting them around the corner and thus enhancing DIBL effects[5,10].

D. Stripe-Gate and Enclosed-Gate Layout Versus TID

As discussed in part A, the effect of total-dose irradiation on standard-edged NMOS transistors is to increase off-state leakage current. This increased leakage is caused by inversion of parasitic transistors at the gate oxide/isolation oxide interface. We designed devices with enclosed-gate layout to eliminate this leakage. This layout technique, which has no active diffusion edges overlapped by polysilicon that separate source and drain, can eliminate edge leakage by removing parasitic transistors between drain and source. Precisely because there are no active diffusion edges or parasitic transistors in the enclosed-gate layout, no radiation-induced leakage current was observed.

As seen in [Figure 5: see original paper], compared to stripe-gate layout transistors, almost no leakage current was observed on enclosed-gate layout transistors after a total dose of 500 krad(Si). Regarding TID effects in enclosed-gate layout, literature[4] has reported work on bulk silicon 0.6 m NMOS devices, showing excellent radiation tolerance. Our work further proves that this method is efficacious for 0.18 m NMOS transistors.

4 Conclusion

The study of TID response in transistors with different gate lengths and layouts in a 0.18 m commercial CMOS technology has demonstrated radiation-enhanced CLM and DIBL effects as the main characteristic degradation mechanisms. The subthreshold region is more sensitive than the saturation region when exposed to gamma irradiation, so this should be considered more carefully in digital integrated circuits than in analog integrated circuits. The slope of the ID-VD characteristic of parasitic transistors continuously increases as total ionizing dose increases, exhibiting a typical channel length modulation effect. The slope is approximately 3 orders of magnitude higher than the corresponding pre-irradiation value for a gate length of 0.18 m, and even more for long-channel devices (20 m).

Enhanced DIBL is attributed to: (1) raised nearby body potential lowering the potential barrier between drain and source; and (2) interaction between parasitic depletion region and the drain/source depletion regions. The enclosed-gate layout demonstrates excellent radiation tolerance by eliminating parasitic transistors between drain and source.

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Note: Figure translations are in progress. See original paper for figures.