A Prototype of beam position and phase measurement electronics for the LINAC in ADS (Postprint)

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Full Text

Preamble

A Prototype of Beam Position and Phase Measurement Electronics for the LINAC in ADS

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Abstract
This article presents a prototype of beam position and phase measurement (BPPM) electronics designed for the LINAC in China's Accelerator Driven Subcritical System (ADS). The signals received from the Beam Position Monitor (BPM) detectors are narrow pulses with a repetition frequency of 162.5 MHz and a dynamic range exceeding 40 dB. Based on high-speed, high-resolution Analog-to-Digital conversion technique, the input RF signals are directly converted to In-phase and Quadrature-phase (IQ) streams through under-sampling, which simplifies both the analog and digital processing circuits. All signal processing is integrated in a single FPGA, enabling real-time calculation of beam position, phase, and current. A series of simulations and tests have been conducted to evaluate the performance. Initial test results indicate that this prototype achieves a phase resolution better than 0.1 degree and a position resolution better than 20 m over a 40 dB dynamic range with a bandwidth of 780 kHz, which is well beyond the application requirements.

Keywords: Beam position and phase measurement, RF signal IQ under-sampling, Analog-to-digital conversion

Introduction

The Accelerator Driven Sub-critical System (ADS) is capable of transmuting radioactive nuclear wastes while simultaneously producing energy in a clean and safe manner, making it a very important research domain in China [1]. As a key component of ADS, a high-intensity proton LINAC is required to produce high-power proton beams. To guarantee high beam quality, measurement of beam position, phase, and current is indispensable.

The beam position and current can be calculated from the signal amplitudes of the four BPM detectors as shown in Eqs. (1), (2), and (3) [2]:

$$Y = K_Y \frac{V_A - V_B}{V_A + V_B} - Y_{\text{offset}} \quad (1)$$

$$X = K_X \frac{V_C - V_D}{V_C + V_D} - X_{\text{offset}} \quad (2)$$

where X and Y are the positions in the X and Y axes; I is the beam current; V_A, V_B, V_C, and V_D are amplitudes of the four induction signals; K_X, K_Y, and K_I are position and current coefficients.

The induction signals from the BPM detectors are periodic narrow pulses with a repetition frequency of 162.5 MHz. Considering that the signal energy is located at 162.5 MHz and its integral multiples, the relative amplitudes of the narrow pulses can be obtained from the signal amplitudes at 325 MHz, because they are proportional to each other.

Most beam measurement systems in China and abroad are single-function—for example, measuring only phase or only position [3–11]. In the LINAC of ADS, however, both high-resolution beam position and phase measurements are demanded within a single system. The position and phase resolutions are required to be better than 0.2 mm and $±$0.5 degree in the input amplitude range of –38 to –4 dBm. In the phase measurement, a Master Oscillator (MO) signal (162.5 MHz sine wave) is used as a reference.

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2. Measurement Principle

The mainstream methods for position and phase measurements are based on IQ analysis. With orthogonal I and Q information, beam phase and amplitude can be calculated [3] as shown in Eqs. (4) and (5):

Traditional IQ analysis methods are based on analog demodulation, such as the RF phase monitor system in the BEPCII LINAC [5,6]. This method requires complex analog manipulation, and performance is easily deteriorated by noise, non-linearity, and mismatches of the analog circuits [7]. With the development of A/D conversion and digital signal processing techniques, the Intermediate-Frequency (IF) IQ sampling technique was developed. In this approach, the RF signal is first down-converted to an IF signal by analog manipulation, then digitized with a sampling clock at four times the IF signal frequency ($f_s = 4f_{IF}$) to directly obtain the I and Q streams. This makes the Digital Signal Processing (DSP) algorithm quite simple and reduces the complexity of analog circuits [8–10]. Another method, digital IQ demodulation, directly digitizes the input RF signal after amplification and filtering, with all signal processing conducted in the digital domain. It is remarkable for its simplest analog circuits but requires rather complicated DSP algorithms [4,11].

This BPPM electronics is designed based on the method of RF signal IQ undersampling (RFIQUS), in which the RF signal is directly converted to a digital IF signal after simple analog manipulation. By adjusting the sampling clock frequency, we can obtain four samples within one IF period—i.e., I and Q points. This method simplifies both the analog circuits and DSP algorithms, thus achieving better system simplicity [12].

In the RFIQUS method, the sampling clock frequency should be carefully selected according to Eq. (6), where N and K are integers.

In this BPPM electronics, the measurement is conducted using the second harmonics of the induction signals (325 MHz). Meanwhile, the MO signal (162.5 MHz) also needs to be measured as the phase reference, which means the electronics must process signals with two different frequencies. For the 325 MHz signal, f_s is set to 100 MHz ($K = 3$ and $N = 1$). Fig. 1 illustrates the basic IQ under-sampling procedure in the frequency domain. As shown in Fig. 1(a), through under-sampling, the 325 MHz RF signal is equivalently down-converted to a 25 MHz digital IF signal whose frequency is centered in the Nyquist zone. We performed simulations to verify the validity of this method using the Matlab platform. As shown in Fig. 2(a), there exist exactly four samples (I, Q, –I, –Q) in one period of the IF signal. For the 162.5 MHz MO signal (as shown in Fig. 2(b)), by discarding half of the samples, a 12.5 MHz IF signal can also be obtained with four samples within one period, and now the equivalent sampling rate is decreased from 100 MHz to 50 MHz. The sampling procedure for the MO signal in the frequency domain is shown in Fig. 1(b).

The above analysis and simulations indicate that the 325 MHz RF signal and 162.5 MHz MO signal can be converted to I and Q streams simultaneously with the same sampling clock, after which the position and phase can be further calculated.

[Figure 1: see original paper] Under-sampling procedure in frequency domain. (a) 325 MHz RF signal, (b) 162.5 MHz MO signal

[Figure 2: see original paper] Simulation of the under-sampling process in time domain; the solid lines refer to the input RF signals; the dashed lines are the digital IF signals.

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3. System Architecture

This BPPM electronics consists of two hardware modules: the Analog Front End (AFE) and the Digital Processing Board (DPB), which are packaged within two PXI-6U modules, as shown in Fig. 3. The RF and MO signals are first filtered and amplified in the analog signal manipulation circuits, then under-sampled in the A/D conversion parts to I and Q streams, which are transferred to the DPB. All digital signal processing is integrated in a single FPGA on the DPB. The calculated results are transferred through the PXI bus to a Single Board Computer (SBC) located in Slot 0 of the chassis for further data analysis and display.

[Figure 3: see original paper] Block diagram of the BPPM electronics.

3.1 Analog Manipulation Circuits

As mentioned above, the input signals from the BPM detectors are narrow pulses with a repetition frequency of 162.5 MHz. As shown in Fig. 4(a), the first Band Pass Filter (BPF) is used to extract the 325 MHz RF signal (the

second harmonic component of the pulses), and the other two BPFs are used to suppress out-of-band noise and spurious frequency components. To guarantee good system performance over a large dynamic range, the 325 MHz RF signal is amplified by an Auto Gain Control (AGC) circuit to fit the full-scale range of the A/D Converter (ADC). The AGC consists of cascaded gain blocks and RF attenuators, achieving a variable gain of more than 40 dB. For the MO signal, the manipulation circuits are quite similar, except for a smaller input dynamic range, as shown in Fig. 4(b). Moreover, the MO signal is split into two paths—one as the reference for the system clock and the other used for phase calculation.

Simulations have been conducted to estimate the performance of the manipulation circuits for the 325 MHz RF signal using Agilent Advanced Design System software. As shown in Fig. 5, the gain dynamic range is more than 40 dB, and the rejection outside the frequency range of 300–350 MHz is good enough for the anti-aliasing filtering requirement [13].

[Figure 4: see original paper] Analog manipulation circuits. (a) 325 MHz RF signal, (b) MO signal

[Figure 5: see original paper] Simulation results of the analog manipulation circuits for the 325 MHz RF signal.

3.2 Analog-to-Digital Conversion Circuits

As the kernel component of the RFIQUS method, the ADC chip AD9467 with 16-bit resolution and 200 Msps maximum sampling rate is employed. With an input signal frequency up to 300 MHz, its Effective Number of Bits (ENOB) and Spurious Free Dynamic Range (SFDR) parameters are better than 11.9 bits and 91 dBc respectively, rendering it suitable for under-sampling applications [14]. Moreover, the AD9467 output interface is 8-bit wide with Double Data Rate (DDR) technique and Low Voltage Differential Signal (LVDS) standard, which simplifies hardware design.

The analog front-end circuit for the ADC is especially important in high-speed, high-resolution situations. The circuit converts the single-ended signal to differential signals and matches impedance. As shown in Fig. 6(a), a balun transformer TC1-1T+ with center tap on the secondary balanced side [15] is used, which has excellent amplitude and phase balance [16]. To further reduce imbalance caused by parasitic effects, two TC1-1T+s are used in cascade mode [17]. In addition, secondary-side termination is employed for smoother frequency response [18].

To select suitable values for the resistors and capacitors in Fig. 6(a), a series of simulations have been performed based on S-parameter models. Fig. 6(b) shows the S11 simulation results for the 325 MHz RF signal (the S11 parameter is equivalent to the signal reflection ratio of the front-end circuit). By trying different values of resistors and capacitors, an optimal S11 of –62.0 dB is achieved.

With the same method, an optimal S11 of –66.5 dB is obtained for the MO signal.

[Figure 6: see original paper] ADC front-end circuit design and simulation. (a) Block diagram of the ADC front-end circuit, (b) S11 parameter simulation results for the 325 MHz RF signal.

3.3 Clock Generation Circuits

In high-speed, high-resolution A/D conversion, a high-quality clock circuit is indispensable. The sampling clock jitter directly affects the Signal-to-Noise Ratio (SNR), as shown in Eq. (7) [19].

Sampling clocks for A/D conversion can be generated with modern digitally controlled Phase Locked Loop (PLL) circuits. In this system, a cascaded PLL structure is employed for excellent jitter cleaning. As shown in Fig. 7(a), the 162.5 MHz reference clock derived from the MO signal is fed into PLL1 to generate a 100 MHz output signal. PLL1 provides initial jitter cleanup with a narrow-loop bandwidth and a low close-in phase noise VCXO. PLL2 translates the output signal of PLL1 with a low far-end phase noise VCO. With the combination of the two PLL stages, the jitter of the final output signal will be quite low with phase noise suppression in both close-in and far-end regions [20]. A clock generator chip AD9523-1 with excellent jitter performance is employed, which integrates all the circuits in Fig. 7(a) except for the VCXO in PLL1. The S620-LF from KVG co. is selected as the low-noise external VCXO.

To estimate the performance of these clock generation circuits, simulations were performed in ADIsimCLK Ver1.4 software. As shown in Fig. 7(b), the broadband jitter of the output clock is 274 fs. For input frequencies of 325 MHz and 162.5 MHz, the corresponding ENOBs are 10.5 bits and 11.5 bits respectively, well beyond the application requirement.

[Figure 7: see original paper] Clock generation circuits design and simulation. (a) Block diagram of the clock generation circuits, (b) Phase noise simulation results of the clock generation circuits.

3.4 Digital Signal Processing and Data Transfer Interface

The block diagram of the DPB is shown in Fig. 8(a). The main FPGA in the DPB receives the high-speed ADC data from the AFE and calculates the position and phase results, which are stored in an on-board DDR SDRAM. The PXI interface is implemented in the CPLD for communication with the SBC in Slot 0. To enhance system design flexibility, online modification of the FPGA logic is achieved using a 128-Mb FLASH chip to store the configuration data.

The XC5VLX155T device from the Xilinx Virtex-5 family is employed as the main FPGA, where all digital processing is implemented, as shown in Fig. 8(b). The input DDR LVDS data (8-bit, 200 Msps) from the AFE is rearranged to 16-bit 100-Msps data streams through IDDR and IBUFDS primitives in the

Xilinx FPGA. The I and Q arrays are then extracted according to algorithms based on Eqs. (4) and (5) to calculate amplitude and phase. Finally, the X and Y positions and beam current are obtained from the amplitudes of the four 325 MHz RF signals based on Eqs. (1), (2), and (3). The results for beam phase, position, and current are transferred to the PXI interface in the CPLD. The FPGA is also responsible for decoding commands from the PXI bus to control the AFE.

[Figure 8: see original paper] Digital processing board design. (a) Block diagram of the digital processing board, (b) Data processing logic in the FPGA.

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4. Initial Test Results

A series of tests have been conducted to evaluate the system performance. The test platform is shown in Fig. 9. A high-quality signal generator R&S SMA 100A is used to generate a 325 MHz RF signal, which is then split to the four RF channels in the AFE. The ADC data from the AFE is transferred to the DPB through high-speed, high-density flat cables. The SBC in Slot 0 of the PXI chassis is responsible for data readout and system control, as well as offline data analysis.

[Figure 9: see original paper] System under test.

4.1 Tests of Analog Manipulation Circuits

The quality of the analog manipulation circuits in the AFE directly affects the position and phase measurement resolution. We conducted tests using a real-time spectrum analyzer (Tektronix RSA3303B). By comparing the amplitudes of the AFE input and output signals, the actual gain of the circuits can be calculated. A series of gain test results were obtained by tuning the attenuation of the RF channels. Test results indicate that a gain dynamic range of 47 dB is achieved, exceeding the 40 dB requirement. The band-pass filtering performance results are shown in Fig. 10; for the 325 MHz RF signal and 162.5 MHz MO signal, the out-of-band suppression is better than 85 dB and 100 dB respectively.

[Figure 10: see original paper] Band-pass filtering performance. (a) 325 MHz RF signal, (b) 162.5 MHz MO signal.

4.2 Waveforms of the Digitized IF Signals

The waveform of the digitized IF signals in Fig. 11 accords well with the simulation results in Fig. 2, indicating that I and Q arrays can be obtained from both the original 325 MHz RF signal and 162.5 MHz MO signal simultaneously.

[Figure 11: see original paper] Digitized waveforms of the 325 MHz RF signal and 162.5 MHz MO signal. (a) RF signal under-sampled waveform, (b) MO signal under-sampled waveform.

Figure 12(a) shows the histogram of phase measurement results with a –10 dBm input amplitude, which corresponds to a phase resolution of 0.08 degree. As shown in Fig. 12(b), in the input amplitude range of –44 dBm to –4 dBm, the phase resolution is better than 0.2 degree with a bandwidth of 25 MHz, and better than 0.1 degree with the bandwidth reduced to 780 kHz, well beyond the $±$0.5 degree requirement.

[Figure 12: see original paper] Test results of phase measurement. (a) Histogram of phase measurement results (input amplitude: –10 dBm, bandwidth: 780 kHz), (b) Phase resolution with different input signal amplitudes.

Figure 13(a) is the position histogram, and a resolution of 0.398 m is achieved with a –10 dBm input amplitude. Fig. 13(b) shows the position resolution in the amplitude range of –44 dBm to –4 dBm. A position resolution better than 20 m is achieved over this 40 dB dynamic range, which exceeds the requirement of 0.2 mm. When the input amplitude exceeds –40 dBm, the resolution is better than 5 m.

[Figure 13: see original paper] Test results of position measurement. (a) Histogram of position measurement results (input amplitude: –10 dBm, bandwidth: 780 kHz), (b) Position resolution with different input signal amplitudes.

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5. Conclusion

A prototype of beam position and phase measurement electronics for the LINAC in ADS is presented. We designed two modules—the AFE and DPB based on the PXI 6U standard—and conducted initial tests to evaluate performance. The electronics has achieved a phase resolution better than 0.1 degree and a position resolution better than 20 m over an input amplitude range of 40 dB with a bandwidth of 780 kHz.

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Note: Figure translations are in progress. See original paper for figures.