A 16-Channel High-Resolution Time and Charge Measurement Module for the External Target Experiment in the CSR of HIRFL (Postprint)

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Date: 2023-06-18T00:00:00+00:00

Abstract

High precision time measurement is required in the readout of the neutron wall and TOF walls in the external target experiment of the Cooling Storage Ring (CSR) project in the Heavy Ion Research Facility in Lanzhou (HIRFL). Considering the time walk correction, both time and charge are measured in the readout electronics. In this 16-channel measurement module, time and charge information are digitized by TDCs at the same time based on the Time-Over-Threshold (TOT) method; meanwhile, by employing high-density ASIC chips, the electronics complexity is effectively reduced. Test results indicate that this module achieves a time resolution better than 25 ps and a charge resolution better than 5% over the input amplitude range from 50 mV to 3 V.

Full Text

Preamble

NUCLEAR SCIENCE AND TECHNIQUES 25, 010401 (2014)

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(Received July 22, 2013; accepted in revised form December 2, 2013; published online February 20, 2014)

High-precision time measurement is required for the readout of the neutron wall and TOF walls in the external target experiment of the Cooling Storage Ring (CSR) project at the Heavy Ion Research Facility in Lanzhou (HIRFL). To address time walk correction, both time and charge information must be measured in the readout electronics. In this 16-channel measurement module, time and charge information are digitized simultaneously by TDCs based on the Time-Over-Threshold (TOT) method, while high-density ASIC chips are employed to effectively reduce electronic complexity. Test results indicate that this module achieves a time resolution better than 25 ps and a charge resolution better than 5% over an input amplitude range from 50 mV to 3 V.

Keywords: Time and charge measurement, Time-Over-Threshold (TOT), Photomultiplier tube (PMT), Cooling Storage Ring (CSR)

DOI: 10.13538/j.1001-8042/nst.25.010401

INTRODUCTION

The Cooling Storage Ring (CSR) project serves as the post-acceleration system for the Heavy Ion Research Facility in Lanzhou (HIRFL), consisting of a main ring (CSRm) and an experimental ring (CSRe) [1, 2]. The CSR complex hosts both an internal target experiment for hadron physics and an external target experiment for heavy ion collisions. The external target experiment comprises one start time (T0) detector, one γ detector, one large dipole magnet, one neutron wall, six Multi-Wire Drift Chambers (MWDCs), and three Time-of-Flight walls (TOF walls), as illustrated in Fig. 1 [Figure 1: see original paper].

As shown in Fig. 1, the three TOF walls are positioned at different angles to detect the flight time of charged particles from target collisions. Time measurement is also required for the neutron wall readout to determine the energy and emission angle of neutrons produced in collisions. For both the TOF walls and neutron wall, the readout electronics must achieve a time resolution as high as 25 ps [3]. To ensure excellent time resolution, the leading-edge discrimination method is employed, with charge information simultaneously measured for time walk correction. Plastic scintillators coupled with photomultiplier tubes (PMTs) are used in both detector types, with a typical PMT output signal waveform shown in Fig. 2 [Figure 2: see original paper], featuring a leading edge of approximately 3 ns.

A high-resolution Time and Charge Measurement Module (TCMM) has been designed for readout of both the TOF walls and neutron wall. Each module integrates 16 readout channels based on the PXI (PCI eXtensions for Instrumentation) standard [4] to ensure high data transfer rates.

II. ARCHITECTURE OF THE TIME AND CHARGE MEASUREMENT MODULE

The TCMM structure is depicted in Fig. 3 [Figure 3: see original paper]. The PMT signal is buffered and split into two paths: one path feeds into a discriminator for time measurement, while the other is transmitted to an SFE16 chip [5] for charge measurement, which functions as a charge-to-time converter (QTC). The HPTDC chip [6] performs digitization of time information. Based on the Time-Over-Threshold (TOT) method [7, 8], both time and charge information (corresponding to the pulse width from the QTC) can be digitized simultaneously. Multi-channel ASIC chips enable high integration density.

The FPGA handles data accumulation, hardware configuration, and front-end monitoring. To enhance time measurement performance, algorithms for correcting the HPTDC's integral nonlinearity (INL) [9, 10] are also integrated into the FPGA. For data readout, the module implements the PXI-6U standard, with a CPLD chip serving as the interface containing a PCI core.

III. ANALOG FRONT-END CIRCUITS

As previously mentioned, both time and charge information must be measured. To achieve optimal performance, signals are manipulated and transmitted in fully differential mode. As shown in Fig. 4, the input signal is buffered, converted to a differential pair, and then split into two paths: one for charge measurement (Vqp and Vqn) and the other for time measurement (Vtp and Vtn).

The differential operational amplifier THS4500 from Texas Instruments serves as the core of the pre-amplification circuits. Through careful resistor value selection, a gain (VOD/Vin) of approximately 2 can be achieved while maintaining an equivalent input impedance (Rin) of 50 Ω for impedance matching, as expressed in:

$$R_{in} = R_T \parallel \left(\frac{1-K}{2(1+K)} \right)$$

where K is defined as [equation fragment]. Using the resistor values from Fig. 4 [Figure 4: see original paper] and Eq. (1) to Eq. (3), the equivalent input impedance calculates to 50 Ω.

A serial-input 12-bit DAC (AD7394) generates the threshold voltage for leading-edge discrimination, with an operational amplifier used to enhance its drive capability.

The signal waveforms for time discrimination are shown in Fig. 5 [Figure 5: see original paper]. The PMT input signal is a negative pulse; through the analog front-end, a pair of differential signals Vtp and Vtn are generated and AC-coupled as shown. The threshold voltage (VTH) is actually set by the

DAC. Time information (T0) corresponds to the intersection of the Vtp and Vtn curves, occurring at a voltage of VTH/2 above the Vtp baseline. Defining VtD = Vtp - Vtn, T0 corresponds exactly to the VTH threshold. This fully differential process enhances resistance to Electromagnetic Interference (EMI) and other common-mode disturbances.

For charge measurement, an ASIC chip (SFE16) is employed. The front-end circuits for SFE16 are shown in Fig. 6 [Figure 6: see original paper]. The differential signals Vqp and Vqn from the THS4500 in Fig. 4 are converted to a single-ended signal, whose voltage amplitude is converted to a current signal through R12 and fed into the SFE16 chip. As shown in Fig. 6, SFE16 comprises a charge-sensitive amplifier (CSA), pole-zero cancellation (PZC) circuit, shaper, gain stage ($×$20), and discriminator. Based on the TOT method, charge information is converted to a pulse width that is subsequently digitized by an HPTDC.

IV. TIME-TO-DIGITAL CONVERSION

The HPTDC is a high-performance time-to-digital converter (TDC) chip designed by the microelectronics group at CERN (European Organization for Nuclear Research) [10]. It operates in four modes: low resolution (781 ps), medium resolution (195 ps), high resolution (98 ps), and very high resolution (24 ps). In this design, two HPTDC chips (HPTDC #1 and #3 in Fig. 7) operate in very high resolution mode to provide eight measurement channels with 25 ps resolution, while one HPTDC (HPTDC #2) digitizes the SFE16 output pulse width using high resolution mode (100 ps).

To simplify control and readout of the three HPTDCs, the chips are organized in a chain to receive configuration data via a common JTAG (Joint Test Action Group) port, as shown in Fig. 7 [Figure 7: see original paper]. They also share a parallel readout interface, transferring data blocks sequentially by passing a token signal in a ring [11].

An FPGA chip (EP2C20F484 from Altera's Cyclone II family) processes HPTDC data and serves as the module controller. As shown in Fig. 8 [Figure 8: see original paper], the SFE16 and three HPTDCs are configured by the FPGA using parameters stored in registers, whose content can be modified by a remote PC. Since the TOT method is employed, the final measurement results consist of time information from the HPTDCs. Input data streams are processed by INL calibration logic and buffered in external SDRAM (MT48LC4M32). Two FIFOs, "FIFO1" and "FIFO2," serve as data bridges between different blocks.

V. LOGIC DESIGN

For the data transfer interface, a CPLD chip is employed with a PCI core (pci_{mt32} from Altera) [12]. A DMA engine implements burst transfer. Test

results demonstrate data transfer speeds exceeding 40 MBps, including the time cost of writing data to disks on the remote PC.

VI. TEST RESULTS

Module performance was evaluated through both laboratory tests and detector commissioning.

A. Laboratory Test Results

Figure 9 [Figure 9: see original paper] shows the test system configuration. A signal generator (AFG3252) produced input signals matching the waveform in Fig. 2. A clock module provided 40 MHz clock signals to multiple measurement modules. Output data from the 16-channel TCMM were transferred to a remote PC for analysis.

1. Time Measurement Tests

In very high resolution mode, HPTDC nonlinearity directly affects overall time measurement performance. This design implements INL calibration to address this issue. Figure 10(a) [Figure 10: see original paper] shows INL test results before and after calibration, demonstrating significant improvement.

Time resolution was evaluated before and after calibration using the "cable delay test" method. The signal generator produced two output signals with a known time delay, and the RMS value of the delay was analyzed from numerous samples. Assuming uncorrelated results from the two channels, single-channel time resolution was obtained by dividing the RMS value by $\sqrt{2}$. As shown in Fig. 10(b) [Figure 10: see original paper], INL calibration enhances time resolution to better than 25 ps.

Figure 11(a) [Figure 11: see original paper] shows a typical histogram of time measurement results with INL calibration applied, yielding a typical time resolution (RMS) of 20.6 ps. All 16 channels were tested, with typical results shown in Fig. 11(b) [Figure 11: see original paper]. Test results confirm the module achieves time resolution better than 25 ps.

2. Charge Measurement Tests

Charge measurement resolution was also evaluated. Using the TOT method, pulse width is obtained by subtracting the leading-edge time from the trailing-edge time of the SFE16 output pulse. Charge information is then calculated using the relationship between input charge and SFE16 output pulse width.

Tests varied the signal source amplitude to obtain a series of results. Figure 12(a) [Figure 12: see original paper] shows TOT output widths for different input signal amplitudes, while Fig. 12(b) [Figure 12: see original paper] shows charge resolution from 50 mV to 3 V. Across this input amplitude range, charge resolution is better than 5%, exceeding requirements.

B. Initial Commissioning Test Results

Following laboratory tests, initial commissioning tests with detectors were conducted at HIRFL using BC408 plastic scintillators (Saint-Gobain Industrial Ceramics, Inc.) and R7527 PMTs (Hamamatsu). Cosmic rays served as scintillator inputs, with PMT output signals measured by the TCMM.

Figure 13(a) [Figure 13: see original paper] shows time measurement results, while Fig. 13(b) [Figure 13: see original paper] displays TOT output signal widths (corresponding to charge information). Figure 13(c) [Figure 13: see original paper] illustrates the relationship between time results and TOT widths, and Fig. 13(d) [Figure 13: see original paper] shows time measurement results after time-walk correction, demonstrating improvement compared to Fig. 13(a). Initial test results agree well with expectations, and further commissioning tests are planned.

VII. CONCLUSION

A 16-channel high-resolution time and charge measurement module has been designed for readout of the TOF walls and neutron wall in the CSR external target experiment at HIRFL. Employing the TOT method, both time and charge information are digitized by HPTDC chips. Test results demonstrate time resolution better than 25 ps and charge resolution better than 5% across an input amplitude range of 50 mV to 3 V.

ACKNOWLEDGMENTS

The authors thank XU Hu-Shan, YU Yu-Hong, and all CSR collaborators who contributed to this work.

REFERENCES

[1] Zheng C, Xiao Z, Xu H, et al. High Energ Phys Nuc, 2007, 31(12): 1177–1180.
[2] Xia J, Zhan W, Wei B, et al. Nucl Instrum Meth A, 2002, 488: 11–25.
[3] Zhou J. Ph.D. Thesis, University of Science and Technology of China, 2012.
[4] PXI Hardware Specification Revision 2.2, Sept. 2004. http://www.pxisa.org/userfiles/files/Specifications/PX
[5] Delagnes E, Abbon P, Bedfer Y, et al. IEEE T Nucl Sci, 2000, 47(4): 1447–1453.
[6] Liu S, Guo J, Zhang Y, et al. Nucl Tech, 2006, 29(1): 72–76.
[7] Manfredi P, Leona A, Mandelli E, et al. Nuclear Instruments and Methods in Physics Research A, 2000, 439: 361–367.
[8] Liu X, Liu S, An Q. Nucl Sci Tech, 2007, 18(3): 164–171.
[9] Liu S, Feng C, Yan H, et al. Nucl Sci Tech, 2010, 21: 49–53.
[10] Zhou J, Liu S, Yin C, et al. Nucl Sci Tech, 2011, 22(6): 372–376.
[11] Kang L, Zhao L, Zhou J, et al. Metrol Meas Syst (in press), DOI:

10.2478/mms-2013-0024.
[12] PCI Compiler User Guide, 2005. http://www.altera.com/literature/ug/ug_{pci}.pdf.

Note: Figure translations are in progress. See original paper for figures.