Radiation tolerance studies on the VA32 ASIC for DAMPE BGO calorimeter (Postprint)

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Abstract

The Dark Matter Particle Explorer (DAMPE) is being constructed as a scientific satellite to observe high energy cosmic rays in space. As a crucial detector of DAMPE, the BGO calorimeter consists of 1848 PMT dynode signals which bring difficulties in front-end electronics on the space-limited and power-limited satellite platform. To overcome the challenge, a low-noise, low-power and high-integration ASIC chip, named VA32HDR14.2, is taken into account. In order to evaluate the radiation tolerance of the chip in space radiation environment, both single event effect (SEE) and total ionizing dose (TID) tests were performed. The SEE test result shows that the effective linear energy transfer (LET) threshold of single event latch-up (SEL) of the chip is around 23.0 MeV-cm2/mg, which is relatively sensitive, thus protection methods must be taken in the electronics design. The TID test result shows that the TID performance of the chip is higher than 25 Krad(Si), which satisfies the design specification.

Full Text

Preamble

Radiation Tolerance Studies on the VA32 ASIC for DAMPE BGO Calorimeter

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The Dark Matter Particle Explorer (DAMPE) is being constructed as a scientific satellite to observe high-energy cosmic rays in space. As a crucial detector component of DAMPE, the BGO calorimeter comprises 1848 PMT dynode signals, which present significant challenges for front-end electronics design given the space- and power-constrained satellite platform. To address this challenge, a low-noise, low-power, highly integrated ASIC chip named VA32HDR14.2 is under consideration. To evaluate the chip's radiation tolerance in the space radiation environment, both single event effect (SEE) and total ionizing dose (TID) tests were performed. The SEE test results demonstrate that the effective linear energy transfer (LET) threshold for single event latch-up (SEL) in the chip is approximately 23.0 MeV $\cdot$ cm^2/mg, indicating relatively high sensitivity that necessitates protective measures in the electronics design. The TID test results show that the chip's TID performance exceeds 25 krad(Si), satisfying the design specification.

Keywords: Radiation effects, SEE, TID, ASIC, VA32HDR14.2
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Introduction

Radiation effects in semiconductor devices, induced by particles and rays in the harsh space radiation environment, can cause damage to satellites [1]. Numerous types of radiation effects have been identified and studied, with single event effects (SEE) and total ionizing dose (TID) being the primary focus of attention [2,3]. These effects are primarily contributed by protons and electrons in the Van Allen belts, as well as protons and heavy ions from cosmic rays and solar flares.

DAMPE is a scientific satellite designed for cosmic ray studies, gamma-ray astronomy, and dark matter particle detection through investigation of the composition and energy spectra of primary cosmic rays [4,5]. The satellite is designed to operate in a near-Earth orbit at an altitude of 500 km with a 97-degree inclination for a mission duration of at least three years. A critical payload is the BGO calorimeter, which consists of 308 BGO crystals and 616 photomultiplier tubes (PMTs). The need to measure 1848 PMT dynode signals presents difficulties in front-end electronics design [6]. To overcome this challenge, a 32-channel charge measurement application-specific integrated circuit (ASIC) named VA32HDR14.2 (VA32) is being considered for the DAMPE prototype [7,8]. According to design specifications, the SEL threshold for the calorimeter electronics should exceed 37.0 MeV $\cdot$ cm^2/mg, while TID performance should exceed 20 krad(Si); otherwise, protection methods must be implemented. To evaluate VA32's radiation tolerance, comprehensive SEE and TID testing is required.

II. Device Characteristics

The VA32HDR14.2 is designed by IDEAS in Norway and manufactured using 0.35 µm CMOS technology processed on epitaxial silicon wafer [9]. As shown in Fig. 1 [Figure 1: see original paper], each VA32 chip contains 32 independent charge-sensitive preamplifiers (CSA). Each preamplifier output connects to a shaper with adjustable shaping time (approximately 2 µs). All shaper outputs are sampled simultaneously, and the pulse heights are multiplexed sequentially to the analog output buffer under control of a 32-bit shift register. The chip can measure positive charges ranging from 0 pC to 13.0 pC with less than 2% linearity error. Additionally, each channel can be tested using an external calibration pulse. Another 32-bit shift register configures the analog demultiplexer to select the specified channel for connection to the calibration signal. The typical power dissipation is 105 mW.

III. Test Setup

A daughterboard-motherboard-host PC architecture was adopted for the test setup. The daughterboard contains passive components and an IC socket for VA32. As shown in Fig. 2 [Figure 2: see original paper], a motherboard controls the daughterboard and communicates with the host PC. For VA32 functional testing, the motherboard incorporates a calibration charge generator module (CAL), analog readout module (ANA), analog-to-digital conversion module (ADC), level conversion module (LCM), and control module (FPGA). The pedestal and RMS noise of VA32 are measured in normal mode, while linearity and dynamic range are measured in calibration mode. The shift-out signal of the chip is monitored to detect single event upset (SEU) in the 32-bit output shift register. The setup also provides four independent power supplies with current measurement (CM) capability for monitoring chip power dissipation. A LabVIEW program on the host PC calculates pedestal and linearity, records SEU events, and monitors chip current in real time.

This flexible architecture enables use in both SEE and TID tests. Except for the VA32 under test, all components on the daughterboard are insensitive to radiation effects. To keep the motherboard away from irradiation, a flat cable and four coaxial cables connect the daughterboard and motherboard. Testing confirmed the setup functions properly even with eight-meter cables, making it practical to place only the daughterboard inside the vacuum chamber for SEE tests, which simplifies motherboard thermal design. The long cables also benefit TID testing by allowing the motherboard to be adequately shielded and positioned away from the radiation source, enabling the use of commercial devices rather than expensive radiation-hardened components.

IV. SEE Test and Results

As shown in Fig. 3 [Figure 3: see original paper], SEE testing was performed at the Heavy Ion Research Facility in Lanzhou (HIRFL) cyclotrons using krypton

ions with initial energy of 25 MeV/nucleon. Irradiations were conducted in air at ambient room temperature, with heavy ions passing through a vacuum/air transition foil. By varying the air thickness, ion LET values could be adjusted from 22.7 MeV · cm^2/mg to 38.5 MeV · cm^2/mg with at least 30 µm range in silicon. Six LET values were selected to characterize VA32 susceptibility to heavy-ion SEL and SEU, as listed in Table 1 .

Five VA32 chips with package lids removed were prepared. Functional testing was conducted prior to radiation exposure. VA32 operating current was monitored during irradiation. A SEL event was identified when current suddenly increased to an abnormal value. When SEL occurred, the ion beam was turned off and the daughterboard was promptly powered down to prevent permanent chip failure. The chip was then powered on again after approximately one minute and testing resumed. Tests with different flux or LET values were performed following self-check procedures before each radiation exposure [10,11].

No latch-up events were observed below an effective LET of 22.7 MeV · cm^2/mg with total fluence exceeding 1×10^7 ions/cm^2. Three chips were used to confirm this phenomenon, leading to the conclusion that the LET threshold lies between 22.7 MeV · cm^2/mg and 24.7 MeV · cm^2/mg. A Weibull curve fitted in Fig. 4 [Figure 4: see original paper] indicates a saturated cross-section approaching 2.0×10^{-4} cm^2/device.

When latch-up occurred, currents for DVDD, DVSS, and AVSS increased suddenly, while AVDD and GND currents remained nearly stable. The increase in DVDD current equaled the sum of increases in DVSS and AVSS currents. Additionally, without powering off the chip during irradiation, a phenomenon of stepwise SEL current increase was observed, suggesting that multiple local latch-up events were triggered.

SEU monitoring was continuous during power-up operation. Throughout the entire irradiation experiment, no SEU events were observed prior to SEL occurrence.

V. TID Test and Results

Two ^{60}Co gamma sources with activity on the order of 10^4 Curie were used for TID testing. To minimize dose enhancement effects from low-energy scattered radiation, the daughterboard was enclosed in a Pb/Al container (2.0 mm Pb with 1.0 mm Al inner lining), and in-situ radiation testing was performed [12,13]. To ensure test setup insensitivity and stability, the daughterboard was tested before and after each irradiation exposure using a golden chip kept away from radiation, while the motherboard was placed 4 meters from the radiation source behind a 1-meter-thick concrete wall.

Three VA32 chips were irradiated to 25 krad(Si) at a dose rate of 5.6 rad/s. Annealing at 100°C for 168 hours was performed after irradiation exposure. Results showed no evident degradation. Since different dose rates may produce different

effects, further study investigated the relationship between VA32 electrical characteristics and accumulated dose. Three additional chips were irradiated to 370 krad(Si) at a dose rate of 12.9 rad/s, followed by room temperature annealing for 168 hours and 100°C annealing for 168 hours in succession.

Figure 5 [Figure 5: see original paper] shows VA32 operating currents as a function of TID. When ionizing dose exceeded 55 krad(Si), IDVDD and IDVSS began rising slowly. After 12 hours of room temperature annealing, IDVDD and IDVSS returned to normal values. IAVDD and IAVSS changed little throughout the entire process.

The gain of VA32 was measured using calibration charge in the range of -2.0 pC to 16.0 pC. Gain was linearly fitted in the range of 0 pC to 12.0 pC. As shown in Fig. 7 [Figure 7: see original paper], gain decreased with accumulating dose, characterized by slope reduction, though the linear interval range increased. Figure 8 [Figure 8: see original paper] shows chip gain degradation. After room temperature annealing and accelerated aging, gain was slightly greater than pre-irradiation values.

Pedestals of all 32 analog channels were measured during testing. Since the 32 analog channel circuits on a single chip are identical, they exhibit similar radiation response trends. Fig. 6 [Figure 6: see original paper] shows pedestal degradation for the 4th, 12th, 20th, and 28th channels. The measured RMS pedestal noise, which represents the sum of VA32 and setup contributions, remained below 3 fC throughout testing, indicating no evident noise level degradation.

VI. Discussion

The BGO calorimeter requires nearly one hundred VA32 chips, necessitating serious consideration of radiation tolerance. The VA32 is relatively sensitive to SEL, with an LET threshold around 23.0 MeV $\cdot$ cm^2/mg that falls below design specification. Therefore, a current measurement and power protection circuit with fast response is recommended. At most six chips are mounted on each front-end electronics board of the calorimeter. As observed in heavy-ion SEE testing, VA32 current ranged from approximately 80 mA to 170 mA when the first SEL occurred—about 3 to 6 times the normal operating current—making it feasible for up to six devices to share a current measurement and power protection circuit to simplify design.

The 32-bit output shift register values monitored for SEU detection were shifted out during readout operations in irradiation. No SEU events were observed. The primary reason is that the chip reset signal was activated before each readout operation, which would reset the 32-bit registers regardless of whether an SEU occurred. Additionally, each readout operation took less than 50 μs and was executed once per second during heavy-ion testing, making ion hits on sensitive areas rare events. This leads to the conclusion that the output shift register is insensitive to SEU.

Since reset prevents SEU event accumulation, even if SEU were to occur during front-end electronics readout operations, only one data packet would be affected as each packet is independent. Therefore, no additional mitigation methods are necessary. Since testing at space environment dose rates (a few mrad/s to hundreds of mrad/s) is impractical, the testing strategy employed high dose rates for convenience. Results demonstrated that VA32 electrical characteristics remained stable above 25 krad(Si), exceeding requirements. Chip functionality did not fail even at doses exceeding 350 krad(Si), and electrical parameters nearly recovered after room temperature annealing. This can likely be attributed to time-dependent effects, where degradation from radiation-induced trapped charge growth during high dose rate irradiation is reversible.

VII. Conclusion

The VA32HDR14.2 ASIC was experimentally validated to meet the radiation tolerance levels required by the DAMPE project. Both SEE and TID irradiation tests were successfully performed. The chip is considered relatively sensitive to SEL, requiring protective measures, while TID radiation results demonstrate satisfactory radiation tolerance.

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Note: Figure translations are in progress. See original paper for figures.