Implementation and integration of a systematic DBPM calibration with PLL frequency synthesis and FPGA (Postprint)

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Abstract

Beam current dependence resulted from nonlinearity and asymmetry of the four channels of digital BPM (Beam Position Monitor) processor deteriorates the BPM performance. A systematic solution based on signal source calibration tactics has been carried out to rectify this defect. It is optimized for implementation in FPGA. Mathematical illustrations of the calibration method, hardware and software design and implementation are presented. A signal source circuit using frequency synthesis technique is designed as calibration standard. Data acquisition system using JAVA web technology and Ethernet is introduced. Integrated FPGA implementation code architecture is presented, and experimental test results show that the method implemented in FPGA is feasible. Compared to other methods, our approach can rectify the nonlinearity and asymmetry simultaneously. The whole solution is integrated into the DBPM processor and can be executed online.

Full Text

Preamble

Implementation and Integration of a Systematic DBPM Calibration with PLL Frequency Synthesis and FPGA

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Beam current dependence resulting from nonlinearity and asymmetry of the four channels of digital BPM (Beam Position Monitor) processor deteriorates BPM performance. A systematic solution based on signal source calibration tactics has been carried out to rectify this defect, optimized for implementation in FPGA. Mathematical illustrations of the calibration method, hardware and software design, and implementation are presented. A signal source circuit using frequency synthesis technique is designed as a calibration standard. A data acquisition system using JAVA web technology and Ethernet is introduced. Integrated FPGA implementation code architecture is presented, and experimental test results show that the method implemented in FPGA is feasible. Compared to other methods, our approach can rectify the nonlinearity and asymmetry simultaneously. The whole solution is integrated into the DBPM processor and can be executed online.

Keywords: Digital Beam Position Monitor (DBPM), Beam current dependence calibration, Frequency synthesis RF circuit, numerical interpolation method, FPGA, Ethernet Java Web data acquisition
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Introduction

Beam Position Monitor (BPM) is a critical instrument for supervisory control of accelerator performance [1]. The digital BPM processor (DBPM) [2, 3] developed in our lab [4] with a software-defined radio architecture [5] moves most of the signal processing module to FPGA and uses the common difference-over-sum ratio method to calculate the beam position [6], as shown in Fig. 1 [Figure 1: see original paper]. However, like other BPM processors, four identical channels are requisite parts, and their asymmetry and nonlinearity can deteriorate beam position measurement. A typical problem of this kind is beam current dependence. As shown in Fig. 2 [Figure 2: see original paper], although the actual beam position remains the same, the measured position depends on the beam current and deviates from its true position; the weaker the beam current, the worse the deviation becomes.

Various calibration methods have been used [7–9] to solve this type of problem, but methods like channel switching cause switching noise which impairs resolution of wide-band beam position information (turn-by-turn, for example). In our solution, rectification on each channel is carried out using a standard signal source as a common reference, which is performed after the digital signal processor (DSP) module in the frequency domain. Compared to other methods [7–9], our approach rectifies the nonlinearity and asymmetry simultaneously. We have optimized the method for easy implementation in FPGA, and the whole calibration is integrated into the DBPM processor.

Methods

Illustration of Calibration Method

To simplify the problem by considering just two channels, the ideal position is calculated by Eq. (1):

$$\text{position} = \frac{A - B}{A + B}$$

where A and B are the respective original signal levels of the pickup at each channel. Nevertheless, practical beam positions are obtained by calculations after the signal processing module on the RF board (Fig. 1), thus the measured position shall be described by Eq. (2):

$$\text{uncalibrated-position} = \frac{aG(A) - bG(B)}{aG(A) + bG(B)}$$

where aG and bG are the transfer functions or response curves of the RF front end of channel A and B, respectively, and A and B are the corresponding original signals at the pickup before follow-up processing. Ideally, both the crude positions at the pickup and the calculated position at the end of processor should depend only on the beam position, which is the goal of position monitoring, but beam current dependence problems occur in real-world situations.

Practically, due to inconsistency and nonlinearity of analog electronic devices, the transfer functions of the four channels of DBPM tend to behave differently and produce distinct outputs from the same input. As shown in Fig. 3 Figure 3: see original paper, with the same inputs, the outputs of four channels are not consistent. Nonlinearity means that at different input power levels, the gain of the channel is not consistent—in other words, a non-linear gain. As shown in Fig. 3(b), the third-order term magnitude is almost 40 times bigger than the linear term. Thus the measured position is blurred by the asymmetry and nonlinearity of respective channels.

Suppose the signal at the processor end is a function of both beam current and position; one has:

$$\text{calculated-position} = \frac{Am(P,I) - Bm(P,I)}{Am(P,I) + Bm(P,I)} = C(P) + \sigma_\alpha c_\alpha I^\alpha$$

where the first term depends solely on position and the second term is the beam dependence factor. The orbit stability shall become worse for a third-generation synchrotron radiation facility if this issue is poorly resolved.

The calibration aims to wipe off this dependence term:

$$\text{calibrated-position} = \frac{ac[aG(A)] - bc[bG(B)]}{ac[aG(A)] + bc[bG(B)]}$$

where ac and bc rectify the corresponding channel to a common ideal channel. By taking ac and bc as the reverse of aG and bG, the gain inconsistency and nonlinearity across the channels will be eliminated; in other words, the accuracy of measured position will not be affected by gain inconsistency and nonlinearity, as shown in Eq. (5):

$$\text{calibrated-position} = \frac{G^{-1}[aG(A)] - G^{-1}[bG(B)]}{G^{-1}[aG(A)] + G^{-1}[bG(B)]} = \frac{A-B}{A+B}$$

To use Eq. (5), the mathematical expression of ac and bc or equivalently aG and bG should be known. In our approach, discrete points of the response curves aG and bG are recorded as control points for interpolation to approximate the response curve.

Interpolation Approximation to the Amplitude Response Curve

If several discrete points of a curve are known to approximate the original curve, a general expression of interpolation with n control points shall be:

$$I_h(x) = \sum f_j l_j(x)$$

where $l_j(x)$ is the jth blending function decided by nearby control points, f_j is the response variable of the corresponding excitation variable x, and $I_h(x)$ is a hybrid of the blending function with weights f_j approximating the original curve.

The next task is to choose a good interpolation blending function $l_j(x)$. Speculated from a zoomed view of Fig. 3, a sole global linear approximation to each channel would poorly represent the behavior of each channel at different input power levels, but at local resolution, a linear approximation would be good enough to depict the behavior. Thus, the piece-wise linear interpolation method can approximate the global behavior of four channels. The whole response curve is divided into several pieces, and a piece can be approximated by Eq. (7):

$$I_{\text{local}}(x) = \frac{x_p - x}{x_p - x_n} f_n + \frac{x - x_n}{x_p - x_n} f_p \quad (x_n \le x \le x_p)$$

where the blending functions are $(x_p - x)/(x_p - x_n)$ and $(x - x_n)/(x_p - x_n)$, and (x_p, f_p) and (x_n, f_n) are control points of the piece. Fig. 4 [Figure 4: see original paper] shows the graphical illustration of the linear blending function for the piece. The blending function is determined by the two control points (x_p, f_p)

and (x_n, f_n), and the interpolation line mixes the two blending functions with weights f_n and f_p.

If the dynamic range is divided into m pieces, there will be a global interpolation function to approximate the response curve, as shown in Fig. 5 [Figure 5: see original paper]. The advantage of this approach is that it can be easily implemented in parallel in FPGA. The control points can be obtained online and stored in FPGA or FLASH memory, and no further parameters are needed.

Signal Source Circuit Design and Frequency Synthesis Criterion

The interpolation method in Sec. II depends on discrete points of the response curve. These discrete points should be taken as control points, which is accomplished by using a standard signal source with programmable output power to traverse the dynamic range of the RF board and record the output of each channel at different input power levels. In Fig. 3, each curve represents the gain of an RF channel at different input power levels at the same frequency.

A frequency synthesis circuit is designed on a separate board for performance evaluation of the calibration solution. It is also integrated on the DBPM to provide the calibration standard reference. As shown in Fig. 6 [Figure 6: see original paper], embedded IOCs of ARM, FPGA, and CPLD are used to configure the frequency synthesis circuit to generate the desired input to the RF board of the DBPM instrument. A band-pass filter is used to pick out the interested harmonics from the oscillation, assisted by a hybrid of low-pass filter and RF amplification. A digital controllable attenuation module is used to make the signal source traverse the dynamic range of the RF board of the BPM processor. The attenuation is controlled by CPLD, which can also be ultimately configured by ARM.

A PLL frequency synthesis scheme is used. As a feedback loop [11], PLL has prominent performance and high frequency accuracy. Integrated circuit ADF4360 from Analog Devices is chosen as the frequency synthesis module. It has a three-wire interface for crucial parameter programming. A 20 MHz XTL is fed into the chip. With external inductors, the internal VCO of ADF4360 is configured to oscillate at a central frequency of 507 MHz using Eq. (8):

$$f_{\text{center}} = \frac{1}{2\pi \times \sqrt{6.2\text{pF} \times (0.9\text{nH} + L_{\text{ext}})}}$$

The external inductor L_{ext} is set at 15 nH, and nearly 500 MHz output is in the range [12].

A dual modulus prescaler with charge pump approach [12] is used to achieve sufficient frequency resolution (Fig. 7 [Figure 7: see original paper]). For example, to generate a frequency of 499.65 MHz with an XTL oscillating at 20 MHz, a

0.01 MHz resolution or PFD frequency can be chosen, and the R divider should be programmed at 2000 (less than 14 bit). Therefore, the total integer counts needed is 49,965. If the prescaler is configured at 16/17, N should be set to 3122 (less than 13 bit) and A should be set to 13. The critical PLL synthesis parameters are shown in Table 1 . The parameters can be dynamically programmed by ARM through CPLD for easy tuning and optimization (Fig. 6).

FPGA Implementation

FPGA is widely used in digital systems for its flexibility and extensibility in digital signal processing [14]. In this solution, we use FPGA as the signal processing module and the control logic module. Using the calibration method proposed in Secs. II and III, it is essential to record the responses of the four channels at different input power levels as calibrating reference points during the calibration state and calculate the reverse function in normal state. All processes are controlled by FPGA.

Control Logic and Data Flow in FPGA

A global state machine is realized in FPGA with three modes: configure mode, calibration mode, and normal mode. Fig. 8 [Figure 8: see original paper] displays the general operation diagram of calibration logic and data flow. When power is switched on, FPGA is initiated in configure mode. During this stage, ARM transmits configuration parameters to FPGA through the ARM interface logic, such as the attenuation series which decides whether to calibrate or not. The FPGA then goes into calibration mode or normal mode directly. In calibration mode, the FPGA conducts a finite state machine to traverse the dynamic range of the frequency synthesis (signal source) circuit output power level. This is done by setting digital attenuators in the frequency synthesis circuit, with options of 0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, and 16 dB, which can be combined to generate arbitrary attenuation levels with 0.5 dB steps. Two attenuators are cascaded such that the dynamic range of the DBPM instrument can be covered.

At each attenuation level, the response power levels along with the input power of the DBPM instrument are recorded in the FPGA block RAM (the parameters can also be set directly by ARM in configure mode). After all attenuations are traversed, the calibration parameters are stored and ready for calibration calculation. Finally, the FPGA goes into normal mode for beam position measurement. ADC data are manipulated in the DDC module and then fed into the rectification module where the calibration parameters stored during calibration are used to compute the reverse-interpolated signal source value. During normal mode, FPGA can be forced to go to calibration mode or configure mode by ARM command. The state machine diagram of the control logic is shown in Fig. 9 [Figure 9: see original paper].

Calibration Data Flow Inside FPGA

The calibration calculation module is placed after the DSP module in FPGA. The process is parallelized. In the first cascade, a segmentation module is installed for determining the piece of current data. This is done by comparing the calibration data stored in the FPGA block RAM. Consecutively, the control points of this piece together with the current data are fed to the interpolation calculation module which performs the computation of Eq. (6). Fig. 10 [Figure 10: see original paper] shows a brief view of the process.

Evaluation Experiments and Results

Evaluation Method and Hardware Setup

To testify the method' s feasibility, testing hardware and a data acquisition system were developed, and evaluation of the method was carried out in two stages. First, the FPGA is set to calibration mode and calibration parameters are stored in the FPGA block RAM. The architecture shown in Fig. 11 [Figure 11: see original paper] is used to assess the performance of the calibration scheme.

To emulate the central beam signal, a commercial signal source is tuned at 499.6 MHz and fed to a power divider which can generate four almost identical signals input to the four channels of the DBPM processors. After calibration, experimental data are obtained through the Ethernet interface of the DBPM processor and transmitted to a TOMCAT SERVER, then distributed to client PCs through web browsers like IE or Firefox.

Data Acquisition System

A LAN-PC aided data acquisition system is developed with JAVA web technology. The Schwarz signal source is remotely controlled by the Tomcat server machine to traverse the dynamic range of DBPM input, and client PCs on the LAN can capture data for position calculation. After the signal source is ready, the Java Web server tells the DBPM to send packets through the Ethernet interface to the server. Client PCs capture the data through the server, as shown in Fig. 12 [Figure 12: see original paper].

Results

Figure 13 [Figure 13: see original paper] shows the comparison before and after calibration. Since the inputs to the channels of DBPM processors are approximately identical, the correct position calculation result should be zero, corresponding to the centered beam situation. Without calibration, the position calculation results vary with the input power level. When the input power level is high, the position calculation is approximately zero; however, with an attenuated input power level, the position calculation digresses far away from zero. This is a typical beam current dependence problem.

With calibration, the calculated position fluctuates around zero at all levels of input power. From the experiments, it can be speculated that our calibration tactic rectifies the beam current dependence problem quite well.

Conclusion

The problem of beam current dependence of BPM processors is solved by the calibration method we proposed. The experimental results testify to the feasibility of the method. Compared to a similar calibration method implemented on PC [15], FPGA provides equally good results and is well integrated into the DBPM processor, allowing the calibration to be carried out online. Overall, this solution gives a satisfying result.

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