Carry-chain propagation delay impacts on resolution of FPGA-based TDC postprint

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Abstract

The architecture of carry chains in Field-Programmable Gate Array (FPGA) is introduced in this paper. The propagation delay time of the rising and falling edges in the carry chains are calculated according to the architecture and they are predicted not equal in most cases. Tests show that the measuring results of the propagation delay time in EP3C120F484C8N series FPGA of Altera are in line with the inference. The difference of propagation delay time results in different accuracies of Time-to-Digital Converter (TDC). This phenomenon shall be considered in the design of TDC implemented in FPGA. It can ensure better accuracy.

Full Text

Preamble

Carry-Chain Propagation Delay Impacts on Resolution of FPGA-Based TDC

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Abstract: This paper introduces the architecture of carry chains in Field-Programmable Gate Arrays (FPGAs). Based on this architecture, the propagation delay times for rising and falling edges in carry chains are calculated, revealing that they are generally unequal. Experimental measurements of propagation delay time in Altera's EP3C120F484C8N series FPGA confirm this

theoretical prediction. This difference in propagation delay leads to varying accuracies in Time-to-Digital Converters (TDCs), a phenomenon that must be considered in FPGA-based TDC design to ensure optimal accuracy.

Keywords: FPGA Firmware, Carry chains, Propagation delay time, TDC
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Introduction

Time-to-Digital Converters (TDCs) are widely used in scientific applications, with high-resolution TDCs being indispensable in many physics experiments, such as time-of-flight (TOF) systems for target recoil-ion momentum spectroscopy at the Institute of Modern Physics (IMP), Chinese Academy of Sciences [**?**]. Two interpolation methods commonly employed in high-resolution applications—the Vernier method and the tapped delay line (TDL) method—have been successfully implemented in field-programmable gate arrays (FPGAs) [**?**]. Currently, TDCs utilizing the tapped-delay line method in FPGA, which exploit the reduced delays provided by dedicated arithmetic (carry-chain) routing structures, represent an efficient and successful approach for achieving low dead-time measurements.

In this work, we conducted a detailed analysis of carry-chain routing structures for further study of TDC implementation in FPGA. Our analysis revealed that the propagation speeds of rising and falling edges should differ from each other. To verify this prediction, we tested the relationship between propagation speeds and TDC accuracy. The results demonstrate that propagation speed significantly affects TDC accuracy, highlighting the importance of edge selection in TDC design.

II. The Architecture of the Carry Chain

The most common FPGA architecture consists of an array of logic blocks, I/O pads, and routing channels. The array of logic blocks is referred to as a Configurable Logic Block (CLB) or Logic Array Block (LAB) depending on the vendor. In general, each block comprises a few logical cells (called ALM, LE, Slice, etc.) \cite{3–5}. A typical cell contains a 4-input Lookup Table (LUT), a Full Adder (FA), and a D-type flip-flop, as illustrated in Fig. 1 [Figure 1: see original paper]. One tap of the carry chain is marked in the figure. The carry-in signal represents a bit carried in from the next less significant stage, while the carry-out signal represents an overflow into the next digit of a multi-digit addition.

It is possible to construct a logical circuit using multiple full adders to add N-bit numbers. Each full adder receives a carry-in signal that is the carry-out signal from the previous adder. This configuration is called a ripple-carry adder, with a 4-bit ripple-carry adder shown in Fig. 2 [Figure 2: see original paper]. When an N-bit ripple-carry adder is implemented in an FPGA, N-1 taps of carry chain can be obtained. The carry chain is typically used as a tapped-delay line in FPGA-based TDC design.

III. Propagation Times of Rising and Falling Edges in the Carry Chain

As the dedicated arithmetic routing structure in FPGAs, a carry chain consists of a series of full adders. The propagation time through the chain comprises the propagation time within each full adder and the propagation time in the interconnecting wires. Generally, the wires are short and contribute equally to the propagation time for both rising and falling edges. Therefore, we consider only the propagation time within the full adder itself.

Most FPGAs are manufactured using CMOS process technology. By analyzing a full adder circuit, the propagation time can be calculated. For this paper, we analyze a typical CMOS full adder, shown in Fig. 3 [Figure 3: see original paper]. To configure the adder as a delay chain, input A is set to 1 and input B is set to 0. Assuming that Cout is logically equal to Cin, the propagation time through the full adder is the time from Cin to Cout. The circuit analysis proceeds in the manner described in Ref. [**?**].

Fig. 4 [Figure 4: see original paper] shows the circuit with FET resistances and capacitances. For convenience, the circuit is divided into two stages, with the propagation times of Stages 1 and 2 calculated separately.

Figure 5 [Figure 5: see original paper] shows the sub-circuits for the output transients of Stage 1. Rn and Rp represent the parasitic resistances of the NMOS and PMOS transistors, respectively. Cout1 is the output capacitance of Stage 1, Cx is the parasitic capacitance between the NMOS transistors, and Cy is the parasitic capacitance between the PMOS transistors. The propagation time for the falling edge is calculated using the circuit in Fig. 5(a). The output voltage can be expressed as Vout(t) = Vdde^{-t/τn}.

Since input A is set to 1 and input B is set to 0, NMOS1 and PMOS1 remain in a conducting state. Consequently, Cx does not discharge during this event, making the time constant of discharge path idis.2 equal to τn2 = 0. The total time constant is obtained by superposition: τna = τn1 + τn2 = Cout1(2Rn). According to Ref. [**?**], the propagation time of the falling edge in Stage 1 is tpf1 = ln 2τna.

The two discharge paths are shown as idis.1 and idis.2. Using the Elmore formula, the time constant of the main discharge path idis.1 is τn1 = Cout1(2Rn). The rise time is computed using the circuit in Fig. 5(b). The time constant of the main charging path ich.1 is τp1 = Cout1(2Rp). As PMOS1 remains in a conducting state, the time constant of charging path ich.2 is τp2 = 0. The total time constant is τpa = τp1 + τp2 = Cout1(2Rp). Therefore, the propagation time of the rising edge in Stage 1 is tpr1 = ln 2τpa.

Figure 6 [Figure 6: see original paper] shows the sub-circuits for the output transients of Stage 2. The time constant of the discharge path idis is τnb = Cout2Rn, where Cout2 is the output capacitance of Stage 2. The propagation time of the falling edge in Stage 2 is tpr2 = ln 2τnb. The time constant of the charging path ich is τpb = Cout2Rp. Thus, the propagation time of the rising edge in Stage 2 is tpr2 = ln 2τpb.

The propagation time of the rising edge from Cin to Cout is: tpr = tpf1 + tpr2 = ln 2(2Cout1Rn + Cout2Rp).

The propagation time of the falling edge from Cin to Cout is: tpf = tpr1 + tpf2 = ln 2(2Cout1Rp + Cout2Rn).

The values of Rp and Rn can be calculated according to Ref. [**?**]: Rp = 1 / [k'__p(W/L)__p(Vdd - |VTp|)] Rn = 1 / [k'__n(W/L)__n(Vdd - |VTn|)]

where k'__n and k'__p are the nFET and pFET process transconductance parameters, respectively (typically k'__p/k'__n = 2 3); (W/L)__p and (W/L)__n are the width-to-length ratios of the p-channel and n-channel MOSFETs, respectively; and |VTp| and |VTn| are the threshold voltages of the p-channel and n-channel MOSFETs, respectively.

A larger width-to-length ratio for the MOSFETs increases circuit speed but also increases circuit area. Through comprehensive consideration of speed and area, the Rp to Rn ratio should be approximately 1 3. The smaller the Rp/Rn ratio, the larger the circuit area.

Figure 7 [Figure 7: see original paper] shows tpr and tpf as functions of Cout2 at different Rp/Rn ratios, assuming Rn = 300 Ω and Cout1 = 50 fF. The results indicate that a larger Rp/Rn ratio produces a greater difference between tpr and tpf. Except when tpr = tpf at Cout2 = 2Cout1, tpr is generally not equal to tpf, depending on the fabrication processes of the FPGAs.

IV. Measurement of the Propagation Time of Rising and Falling Edges in the Carry Chain

There are at least two approaches to measure propagation time in the carry chain: the double registration approach [**?**] and the statistical approach [**?**]. These are typically used as digital calibration methods for FPGA-based TDCs. The double registration approach measures only the average cell delay. When bin widths differ, requiring bin-by-bin measurement, the statistical approach is preferred [**?**], and this is the method we employ.

We used an FPGA TDC to measure the propagation time in the carry chain. A simplified block diagram of the TDC implemented in FPGA is shown in Fig. 8 [Figure 8: see original paper] [**?**]. The TDC includes two crucial components: the time delay lines (the carry chain) and the coarse time counters. The TDC is based on a counter and interpolating method, with a detailed description provided in Ref. [**?**].

The measurement procedure is as follows [**?**]. After power-up or system reset, the TDC input is fed with calibration hits. The timing of these hits should have no correlation with the clock signal driving the TDC, so the hits are generated from an independent oscillator. A Differential Non-Linearity (DNL) histogram is stored in the FPGA's internal memory. Once all hits are recorded in the histogram, a sequence controller builds a lookup table (LUT) in the FPGA's internal memory. The LUT is integrated from the DNL histogram so that it outputs the actual time at the center of the addressed bin.

The LUTs for rising-edge and falling-edge TDCs are shown in Fig. 9 [Figure 9: see original paper]. The slope can be interpreted as the average bin width for the falling-edge TDC, with approximately half the slope for the rising-edge TDC. The bin width represents the propagation time of the rising or falling edge in one tap of the carry chain. The propagation time of the falling edge is shorter than that of the rising edge due to differences between N and P transistors in CMOS integrated circuits. Experiments were conducted on several FPGA series from Altera and Xilinx.

V. The Relationship Between Propagation Time and TDC Accuracy

It is intuitive that shorter propagation delay time yields higher accuracy in TDC design. Therefore, we tested rising-edge TDC and falling-edge TDC separately. "Rising-edge TDC" refers to a TDC that uses rising-edge information for time-to-digital conversion, while "falling-edge TDC" uses falling-edge information.

The TDC input is a pulse train with a repeating rate generated by an external phase-locked loop, and the TDC is driven by a crystal oscillator. The time between successive rising edges of the pulse train is measured by both the rising-edge TDC and falling-edge TDC, respectively, with digital calibration applied in the measurement [**?**].

The test results for successive rising and falling edges are summarized in Table 1 . The root mean square (RMS) resolutions of the rising-edge TDC and falling-edge TDC are 95 ps and 52 ps, respectively. The falling-edge TDC exhibits shorter average propagation delay time. The test results demonstrate that shorter propagation delay time produces better RMS resolution, while the longer propagation delay time of the rising-edge TDC limits its resolution.

VI. Conclusion

The difference in propagation time in carry chains arises from the fabrication processes of FPGAs. Since SRAM-based FPGAs are fabricated using processes similar to CMOS, this phenomenon is common in SRAM-based FPGAs. Awareness of this situation enables better understanding of FPGA-based TDCs.

The test results show that the impact of this phenomenon on TDC accuracy is significant. This effect is present in TDCs implemented in FPGA using the tapped-delay line method. Understanding this phenomenon allows us to better take advantage of the reduced delays provided by dedicated arithmetic (carry-chain) routing structures.

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