Readout electronics for CSR-ETF silicon strip array detector system (postprint)

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Abstract

A readout electronics system has been developed for the silicon strip array detector system of HIRFL-CSR-ETF. The system comprises 48 front-end electronics (FEE) boards, 12 PXI-DAQ boards, and one trigger board, capable of performing energy and time measurements for 4608 channels. Each FEE board is based on 6 ASIC chips (ATHED), implementing energy and time measurements for 96 channels. The PXI-DAQ board satisfies the requirements for high-speed counting and multi-channel readout, and can process signals from 4 FEE boards. The trigger board is designed to select valid events. The energy linearity of the readout electronics is better than 0.3% over a dynamic range of 0.1–0.7 V. Using a standard triple-alpha source for testing, an energy resolution of 1.8% was achieved at 5.48 MeV. This readout electronics enables the silicon strip array system to identify particles with A 14.

Full Text

Preamble

Readout Electronics for CSR-ETF Silicon Strip Array Detector System

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A readout electronics system has been developed for the silicon strip array detector system of HIRFL-CSR-ETF. The system consists of 48 front-end electronics (FEE) boards, 12 PXI-DAQ boards, and one trigger board, enabling energy and time measurements for 4608 channels. Each FEE board is based on six ASICs (ATHED), which implement energy and time measurements for 96 channels. The PXI-DAQ board meets the requirements for high-speed counting and large channel count, processing signals from four FEE boards. The trigger board is developed to select valid events. The energy linearity of the readout electronics is better than 0.3% across the dynamic range of 0.1–0.7 V. In tests with a standard triple alpha source, the energy resolution was 1.8% at 5.48 MeV. This readout electronics enables the silicon strip array system to identify particles with mass number A $\leq$ 14.

Keywords: Readout electronics, PXI-DAQ, Silicon strip, Front-end electronics, Application-specific integrated circuit
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Introduction

Silicon strip detectors are widely used in nuclear physics, high-energy physics, and astrophysics [**?**]. Over the last 30 years, impressive developments have been made in silicon strip sensors and their readout electronics for high-energy physics [**?**], driven by parallel advances in low-noise electronics and very large-scale integration [**?**]. Many specialized chips have been developed for silicon strip detectors in various experiments, such as the ABCD3TA chip for the ATLAS tracker [**?**], the APV25 chip for the CMS tracker [**?**], and the A128C chip for the ALICE tracker [**?**].

A silicon strip array detector system will be equipped for the external target facility (ETF) of the Cooling Storage Ring on the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR-ETF) [**?**]. The system consists of twelve telescopes, each containing two double-sided silicon strip detectors measuring 49.8 mm $\times$ 49.8 mm with 96 strips on each side.

According to the ETF experimental requirements, a readout electronics system has been developed by the nuclear electronics group for the silicon strip array detector system. This paper describes the readout electronics in detail. An application-specific integrated circuit (ASIC) chip developed at CEA Saclay, France for silicon strip detectors is employed to address the challenge of the large channel count. The readout electronics consists of FEE (front-end electronics) boards, PXI-DAQ boards (PXI: PCI extensions for instrumentation; DAQ: data acquisition), and a trigger board. Each FEE board can implement

energy and time (E and T) measurements for 96 channels. The PXI-DAQ meets the requirements for high-speed counting and large channel count [**?**] and processes signals from four FEE boards. The trigger board is developed to select valid events. Overall, the readout electronics can implement energy and time measurements for 4608 channels.

[Figure 1: see original paper] Block diagram of the readout electronics.

II. Readout Electronics

The readout electronics for the silicon strip array detector system comprises 12 units. As shown in Fig. 1, each unit consists of four identical FEE boards and one PXI-DAQ board, with the trigger board shared among all 12 units. Each unit can implement energy and time measurements for 384 channels, giving the complete readout electronics a total capacity of 4608 channels. Each FEE board contains six ASIC chips (ATHED) connected in a daisy chain, processing 96 channels of energy signals and 96 channels of time signals. This ASIC chip measures the energy and arrival time of particles and generates a trigger when the energy exceeds an adjustable minimum threshold [**?**].

The block diagram of ATHED is shown in Fig. 2 [**?**]. Briefly, ATHED is a 16-channel ASIC chip. Each channel includes a charge-sensitive amplifier (CSA) with dynamic ranges of 11 MeV, 22 MeV, 50 MeV, 100 MeV, and 200 MeV, an energy branch (shaping at 1 and 3 μs with track-and-hold), and a timing branch consisting of fast shaping, a discriminator with slow control, adjustable thresholds, and a time-to-amplitude converter (TAC) with ranges of 300 and 600 ns [**?**, **?**]. The analog energy and time information from 16 channels is transmitted through a voltage-to-current converter (VIC) ($±$2 mA/V) to the PXI-DAQ board. ATHED improves the integration level of FEE boards and enables multichannel data processing while maintaining good performance, with power dissipation of only 28 mW per channel, thus reducing the overall power consumption of the FEE boards.

The PXI-DAQ board implements slow control, analog output signal adaptation, fast timing pulse generation, PXI interface communication, and data acquisition. Each PXI-DAQ board can process signals from four FEE boards. To effectively reduce crosstalk between the FEE and PXI-DAQ boards, flat twisted-pair cables are used to transmit low-voltage differential signals (LVDS) [**?**]. The trigger board makes fast L1 trigger decisions and generates trigger data that are packed and transmitted to a PC via the PXI bus for offline analysis [**?**]. The PXI platform-based readout system can satisfy the requirements for high-speed counting and large channel count [**?**]. The software features a user-friendly GUI (Graphical User Interface) written in C using LabWindows/CVI under the Windows XP operating system [**?**].

A. Front-End Electronics Board

As shown in Fig. 3, the FEE board consists of six ASIC chips, an internal test pulse generator, an LVDS receiver & driver, and an inspection circuit. Each analog unit comprises four FEE boards, processing energy and time signals for 384 channels. The outputs of each board can be carried on either one or two analog differential-pairs, with signals transmitted in current-differential mode through twisted pairs to the PXI-DAQ board.

[Figure 3: see original paper] Block diagram of the analog unit.

On each FEE board, the programmable internal test pulse generator, which drives the analog test input of each ATHED, verifies the functionality of all ASIC chips and implements physical calibration of each channel. The internal test pulse generator is based on a PCA9555 (16-bit I^2C bus I/O port) and a digital-to-analog converter (DAC). Its output injects a current signal into the input of a selected channel. By analyzing the data acquired by the PXI-DAQ with appropriate test signals, the functionality of the ASICs can be verified. A debug signal generated by the ASIC is used to check whether the ASIC chip is operating normally.

To protect against electromagnetic interference (EMI), all fast control signals (stop, hold, start, request, reset, CLK) are transmitted using the LVDS standard. The request signals generated by the ASIC chips are transmitted to the trigger board for trigger signal preprocessing. The readout time of an analog unit is less than 32 µs when data are transmitted on two analog differential-pairs and less than 61 µs when transmitted on a single analog differential-pair. The transfer function for the silicon detector system is 34.22 µA/MeV for each channel on the FEE board.

[Figure 4: see original paper] The timing diagram for data transmitted on an analog differential-pair.

Figure 4 shows the timing diagram for data transmission on an analog differential-pair. The energy information of a channel is transmitted to the VIC at the rising edge of the CLK signal, while the time information is transmitted at the falling edge. The energy and time information for 96 channels, transmitted on a single analog differential-pair, is sent through the VIC to the PXI-DAQ board channel-by-channel using a total of 96 CLK cycles. Since data are transmitted at both the rising and falling edges of the CLK signal, the Sclk signal frequency is double that of the CLK signal. The Stop signal is transmitted to the TAC, and the Hold signal is transmitted to hold the energy signals.

B. PXI-DAQ Board

The PXI plug-in DAQ board (Fig. 5) consists of opto-isolators, a signal receiver & driver, an analog output adaptation unit, ADCs, an FPGA, and a PXI interface. Using four high-speed ADCs (20 MHz), the PXI-DAQ can meet

the requirements for high-speed counting and large channel count. Each PXI-DAQ board processes signals from four FEE boards. To implement remote control, flat twisted-pair cables are used to transmit LVDS signals, effectively reducing crosstalk between the FEE and PXI-DAQ boards. To further reduce crosstalk, high-speed opto-isolators are employed to block high voltages and voltage transients. After I-V conversion, low-pass filtering, and amplification, the analog signals acquired from the FEE boards are fed into the high-speed ADCs (AD9248). Under control of the ADC conversion sequence, digital signals are obtained as 14-bit binary numbers. If judged valid by the FPGA, the digital signals are packed with event identification bits into a 32-bit frame and stored in the FIFO; otherwise, the signals are ignored. When the amount of data stored in the FIFO exceeds the set threshold, an interrupt request signal is sent to the PXI bus for master control, after which the data in the FIFO are transferred to the PC via DMA. Through the I^2C bus interface, the PXI-DAQ board implements parameter setting for the front-end ASICs, the test signal generator, and other I^2C components on the FEE boards.

[Figure 5: see original paper] Block diagram of the PXI-DAQ unit.

C. Trigger Board

The trigger board receives request signals generated by the ASIC chips of the FEE boards and makes fast L1 trigger decisions to select valid events. It generates hold and reset signals and sends them via the trigger bus to the PXI-DAQ boards, which in turn send hold signals to the FEE boards to read out data. The trigger board generates trigger data that are packed and transmitted to the PC via the PXI bus for offline analysis [**?**].

III. Performance of the Readout Electronics

The readout electronics have been measured in the laboratory. Pulses generated by an ORTEC 448 pulser are transmitted to the test input of the FEE board. The PXI-DAQ board sends fast control signals to the FEE board after the trigger board receives the request signals generated by the FEE board, while simultaneously implementing data acquisition. As shown in Fig. 6, the energy linearity of the readout electronics is better than 0.3% across the dynamic range of 0.1–0.7 V. Figure 7(a) shows the energy spectrum measured with the ORTEC 448 under laboratory conditions, demonstrating an energy resolution better than 0.5% (19 MeV). Tested with a precision charge/time generator from Phillips Scientific (Model 7120), the time linearity is better than 0.2% across the dynamic range of 116–536 ns, with time resolution better than 0.24% in the range of 0–600 ns. Figure 7(b) shows the alpha spectrum of a standard triple alpha source (^{238}Pu, ^{241}Am, and ^{244}Cm) measured with a 49.8 mm × 49.8 mm double-sided silicon strip detector system for testing the readout electronics.

[Figure 6: see original paper] Energy linearity of the readout electronics over 0.6 V range.

The energy resolution can be obtained through Gaussian fitting. As shown in Fig. 7(b), the energy resolution is approximately 1.8% at 5.48 MeV. The particle identification capability of the silicon strip detector can be estimated using Eq. (1):

$$\delta A/A = \{[\delta(\Delta E)/\Delta E]^2 + (\delta E/E)^2\}^{1/2}$$

where $\delta(\Delta E)/\Delta E$ is the energy resolution of the silicon strip detector and $\delta E/E$ is the energy resolution of a CsI detector, which is generally better than 3% [**?**]. For a maximum value of $\delta A = 0.5$, particles with $A \leq 14$ can be identified. Since the silicon strip array detector is designed to identify particles with $A \leq 10$, the readout electronics achieves the design goal.

[Figure 7: see original paper] (Color online) Energy spectrum measured with ORTEC 448 (a) and the silicon strip detector system (b).

IV. Summary

A readout electronics system has been developed for the CSR-ETF silicon strip array detector. The system consists of 48 FEE boards, 12 PXI-DAQ boards, and one trigger board. Using ASICs, the FEE achieves high density, large channel count, and low power consumption. Using high-speed ADCs (20 MHz), the PXI-DAQ board enables rapid acquisition of multichannel data. The readout electronics system can implement energy and time measurements for 4608 channels and has proven reliable for nuclear physics experiments on the ETF of HIRFL-CSR, achieving the desired performance goals.

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Note: Figure translations are in progress. See original paper for figures.