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Development of COTS ADC SEE test system for the ATLAS LAr calorimeter upgrade (Postprint)

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Abstract

Commercial off-the-shelf (COTS) ADCs (analog-to-digital converters) that are radiation-tolerant, high speed, high density and low power will be used in upgrading the LAr (liquid argon) calorimeter front end (FE) trigger readout electronics. Total ionization dose (TID) and single event effect (SEE) of the COTS ADCs should be characterized. In our initial TID test, 17 COTS ADCs from different manufacturers with dynamic range and sampling rate meeting requirements of the FE electronics were checked, and the ADS5272 of Texas Instruments (TI) was the best performer of all. Another interesting feature of ADS5272 is its 6.5 clock cycles latency, which is the shortest of all the 17 candidates. Based on the TID performance, we designed an SEE evaluation system for ADS5272, which allows us to further assess its radiation tolerance. In this paper, we present a detailed design of ADS5272 SEE evaluation system and show the effectiveness of this system while evaluating ADS5272 SEE characteristics in multiple irradiation tests. According to TID and SEE test results, ADS5272 was chosen to be implemented in the full-size LAr Trigger Digitizer Board (LTDB) demonstrator, which will be installed on ATLAS calorimeter during the 2014 Long Shutdown 1 (LS1).

Full Text

Preamble

Development of COTS ADC SEE Test System for the ATLAS LAr Calorimeter Upgrade

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Abstract: Commercial off-the-shelf (COTS) ADCs (analog-to-digital converters) that are radiation-tolerant, high speed, high density, and low power will be used in upgrading the LAr (liquid argon) calorimeter front end (FE) trigger readout electronics. Total ionization dose (TID) and single event effect (SEE) of the COTS ADCs should be characterized. In our initial TID test, 17 COTS ADCs from different manufacturers with dynamic range and sampling rate meeting requirements of the FE electronics were checked, and the ADS5272 from Texas Instruments (TI) was the best performer of all. Another interesting feature of ADS5272 is its 6.5 clock cycles latency, which is the shortest of all the 17 candidates. Based on the TID performance, we designed an SEE evaluation system for ADS5272, which allows us to further assess its radiation tolerance. In this paper, we present a detailed design of the ADS5272 SEE evaluation system and demonstrate the effectiveness of this system while evaluating ADS5272 SEE characteristics in multiple irradiation tests. According to TID and SEE test results, ADS5272 was chosen to be implemented in the full-size LAr Trigger Digitizer Board (LTDB) demonstrator, which will be installed on the ATLAS calorimeter during the 2014 Long Shutdown 1 (LS1).

Keywords: COTS ADC, Total ionization dose, Single event effect, Single event upset, Single event functional interrupt
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Introduction

At the LHC (Large Hadron Collider) at CERN, the ATLAS LAr calorimeter upgrade project is proposed to enhance physics experiments in the high-luminosity environment foreseen in the next ten years [**?**]. To provide higher-granularity, higher-resolution, and longitudinal shower information from the calorimeter to level-1 trigger processors in this upgrade, new LAr calorimeter trigger readout electronics must be designed, built, and installed. Compared to the existing readout cell "trigger tower," the new readout element referred to as Super Cell [**?**] provides a 10-fold finer granularity scheme and additional information with more powerful tools for Level-1 trigger feature extraction. Additionally, the digitization precision of the Super Cell signals is improved by at least a factor of 4 compared to the existing Level-1 system by optimizing the quantization scale and dynamic range of the digitizers. These upgrades will be essential to extend the physics potential at higher instantaneous luminosities and more severe

pileup conditions expected after Phase-I and Phase-II upgrades of the LHC.

In the Phase-I upgrade, approximately 40,000 channels of Super Cell signals will be digitized at the front end LTDB, and data will be streamed out to the back end DPS (digital processing system). A radiation-tolerant ADC is required for signal digitization in the front end electronics. The LAr collaboration has prepared two technological routes: custom ASIC (application-specific integrated circuit) ADC development and COTS ADC evaluation. Two custom ASIC ADCs are under different stages of prototyping development. However, given the uncertainty in the development cycle and costs associated with custom chip design, an extensive study has been conducted for a COTS option that meets both electrical and radiation requirements. Previous studies on the radiation sensitivity of many COTS parts can inform component decisions appropriate for our design, with good experience documented in References \cite{2–5}.

In this paper, the TI COTS ADC, ADS5272 [**?**], is chosen as a good candidate for use in the LAr calorimeter electronics upgrade. Its electrical features include: maximum sampling rate of 65 MSPS (million samples per second); dynamic range of 12 bits; resolution of 11.5 ENOB (effective number of bits); latency of 162.5 ns (6.5 clock cycles); and power consumption of 113 mW per channel. These parameters meet the digitization requirements [**?**] of the LAr calorimeter upgrade, and therefore a test program was developed to study the irradiation properties of ADS5272. The outline of this paper is organized as follows. In Section II, we show the TID radiation effects of 17 COTS ADCs. In Section III, we discuss the detailed development of the ADS5272 SEE evaluation system. In Section IV, we use our evaluation system to characterize the ADS5272 SEE radiation tolerance. Finally, we conclude this paper in Section V.

II. Total Ionization Dose (TID) Irradiation

Long-term exposure to ionizing radiation can cause parametric degradation and ultimately functional failure in electronic devices. The damage occurs via electron-hole pair production, transport, and trapping in the dielectric and interface regions. To examine the effect of this issue on the COTS ADC, we performed TID tests using the ^{60}Co gamma irradiation facility for solid-state physics at Brookhaven National Laboratory (BNL). The test flow is shown in Fig. 1 [Figure 1: see original paper] and the results are shown in Table 1 [**?**].

Of the six ADCs which withstood doses of over 1 Mrad (Si) shown in the bottom six rows of Table 1, the ADS5272 is the best performer—surviving up to 88 kGy (Si). See Fig. 2 Figure 2: see original paper for its test results. Additionally, two ADS5272 samples were annealed at approximately 85°C after a 24 kGy (Si) TID test. After annealing, both ADCs recovered to their original characteristics. Fig. 2(b) shows the analog and digital power consumption of Sample 2 before and after annealing.

III. Single Event Radiation Effects

Based on the test results in Section II, an evaluation system for ADS5272 was established to characterize its single event effects. This system consists of three parts: hardware, firmware, and software. An ADS5272 test board (Fig. 3 [Figure 3: see original paper]) is custom-built for SEE testing.

A. Design of ADS5272 Test Board

SMA connectors were chosen as the input connectors for the ADS5272 test board. The output connector is a Samtec FMC (FPGA Mezzanine Card) HPC connector, which makes the ADS5272 test board easy to attach to the ML605. To match the input signals with the differential full-scale input voltage range of ADS5272, an ADC driver was added in the analog signal chain. The ADC driver is ADI AD8138 (Fig. 4 [Figure 4: see original paper]), which was qualified up to 5 kGy TID. The AD8138 output and ADS5272 input are DC coupled with RC low-pass filtering to improve the signal-to-noise ratio (SNR).

The clock scheme for the ADS5272 has three options: SMA input clock, FPGA differential output clock, and on-board oscillator. ADS5272 needs an LVTTL clock, so a Maxim MAX9160 was chosen as the clock fan-out driver for all clock input options, which survived approximately 150 kGy TID.

There are two power supply options: an external supply and an on-board POL (Point-of-Load) DC-DC converter LTM4616 from Linear Technology. The external power supply provides AD8138 power ($±$3.3 V), ADS5272 analog power (+3 V) and digital power (+3 V, contingency), ADS5272 reference voltage REFT (+1.95 V) and REFB (+0.95 V), ADS5272 common-mode voltage (+1.45 V), and LTM4616 input (+5 V). The DC-DC converter LTM4616 can provide analog and digital power to the ADS5272. A detailed block diagram of the ADS5272 test board is depicted in Fig. 5 [Figure 5: see original paper]. As required by the irradiation test, a clearance circle of 3 inches diameter is designated around the ADS5272 (Fig. 4), where no other active component is placed.

B. Development of Firmware in Virtex-6

The firmware of the ADS5272 SEE test system is developed in a Virtex-6 FPGA, which mainly consists of a MicroBlaze (UBLZ) core system and the FPGA fabric logic. The block diagram is illustrated in Fig. 6 [Figure 6: see original paper]. UBLZ is a 32-bit RISC (Reduced Instruction Set Computer) embedded processor soft core, which acquires data from the ADC and compares it with an LUT (Look-Up Table). The data are then buffered to DDR3 SDRAM for readout through Gigabit Ethernet or USB. The FPGA fabric logic comprises five sub-function blocks: ADC logic block, LUT generator block, comparison & SEE detection block, NPI (Native Port Interface) data generator block, and UBLZ IO bus interface block.

The ADC logic block is mainly responsible for the following functions: (1) deserializing ADC raw serial data from serial to parallel (S2P); (2) controlling and programming ADC settings through a serial peripheral interface (SPI); and (3) keeping the ADC bit clock 90° out-of-phase with respect to the data and frame clock through ADC sampling clock alignment (SCA). The SCA function is realized through adjustment of the IODELAYE1 primitive of the FPGA according to associated SNR and noise floor plots.

The LUT generator aims to generate a programmable look-up table via FPGA embedded block RAM resources. This look-up table is aligned and locked with the ADC waveform before the beam test starts, which is critical preparation for the comparison & SEE detection block.

Real-time comparison of ADC data versus LUT is performed in the comparison & SEE detection block. This block continuously checks the difference between the ADC output and the LUT. When the difference exceeds a preset programmable threshold, the case is deemed an SEE event. An error flag is then polled to initiate DDR3 transfer, and an error counter begins counting.

The NPI data generator block composes ADC & LUT data according to PLB (IBM CoreConnect Processor Local Bus) timing and data structure rules. The NPI block sends data to the MPMC (Multi-Port Memory Controller) NPI interface. It also includes a verification function to send user test patterns when enabled by a signal (Verif_{en}) generated from the UBLZ IO bus IF block.

The UBLZ IO bus IF block provides a read-write register interface that serves as a bridge to the UBLZ processor. It leverages a simple user logic bus to decode transactions. Write operations include transporting configuration information and delay tap values from MATLAB to the ADC logic block, updating the LUT according to the mean value of 100 samples calculated by MATLAB, setting the threshold to detect an SEE event, and triggering DDR3 test transfer. Read operations consist of getting values of the ADC registers and SEE error counter, examining SEE error flags, and reviewing test patterns.

C. Software Realized in MATLAB GUIDE

Software is built on the GUI panel (Fig. 7 [Figure 7: see original paper]) with MATLAB GUIDE, which communicates with the UBLZ system via TCP/IP server sockets. MATLAB applications serve three principal functions.

The first function is calculation and analysis. MATLAB calculates the mean value and RMS of the difference between ADC and LUT using 100 samples, sending the mean value back to the firmware “LUT Generator” block to update and match the LUT with ADC data. MATLAB also performs FFT on ADC data to obtain the corresponding noise level and SNR (Signal-to-Noise Ratio) plot. It then rounds the mean value of all working delay taps to determine the most appropriate value for ADC sampling clock alignment.

The second function is a control “keyboard.” All input control information is

manipulated by MATLAB, including issuing ADC hardware reset, sending ADC SPI configuration bits, adjusting the LUT address value and offset value, triggering DDR3 transfer, setting the SEE error threshold, and manually injecting errors into the SEE test system for simulation.

The third function is remote "monitoring." MATLAB can plot ADC data versus LUT in real time and display ADC register values on the GUI. It also monitors the voltage of the power supply and the amplitude of the signal generator through Ethernet, facilitating debugging and testing.

IV. SEE Test Results

The ADS5272 SEE evaluation system has been successfully used in multiple irradiation tests. In October 2012, a test was performed at LANSCE WNR (Los Alamos, NM) with initial neutron beams with maximum energy of about 800 MeV. The neutron spectrum matches what is expected at the position of the ATLAS LAr electronics crate. The second test was conducted at IUCF, Bloomington, IN (see Section IV B) to illustrate the correctness and practicality of the ADS5272 SEE test system. Another test was performed at Mass General Hospital (Boston, MA) with 216 MeV protons. The total SEU (single event upset) cross section observed in these tests is consistent across all facilities.

A. Test Setup

The beam tests described above shared a similar test setup. We used a signal generator to inject a sine wave into ADS5272, which was running at f_{sample} = 40 MSPS. The frequency of the sine wave was about 40 kHz (f_{sample}/2^{10}) to ensure sufficient samples were acquired for each cycle. The FPGA acquired ADC data and compared samples with the LUT in real time. Any deviation larger than a preset threshold was flagged as an SEE event, and a record of approximately 4 k samples was saved for posterior analysis. The system was synchronized by a 10 MHz clock generated by the ML605 board. The test setup diagram is shown in Fig. 8 [Figure 8: see original paper] [**?**].

B. Proton Beam Test at IUCF

One SEE test was performed on November 30, 2012 at IUCF with high-flux proton beams (Fig. 9 [Figure 9: see original paper]). Three ADCs were irradiated with approximately 200 MeV protons to measure SEU and SEFI (Single Event Functional Interrupt) cross sections.

For SEU (bit flip), the ADCs operated in no-external-intervention mode; that is, when a single bit or multiple bits in the data stream flipped, the ADCs continued to operate normally. The impact was examined through cross-section measurements. SEFI was recorded when the ADCs ceased operation: the ADC output remained constant, requiring an external reset to restore normal operation. We note that SEFI is not equivalent to latch-up, as it does not require

a power cycle for the ADC to recover. The ADS5272 could be reset in 200 ns without a power cycle.

Samples 1 and 2 were tested for cross-section measurements without any special test conditions. Sample 3 was tested to evaluate the effectiveness of a mitigation strategy for SEFI, with conditions modified to favor SEFI detection rather than SEU detection. A approximately 1 Hz hardware reset was issued to clear any register that might be corrupted by SEU outside of the data stream. Test results are listed in Table 2 .

The total single event upset (SEU) cross section is $\sigma\{SEU\} = (4.0 \pm 0.7) \times 10^{-12}$ cm^2. *Although statistics are poor, we observe that the upset probability is independent of the bit position in one ADC word (12 bits). Therefore, we specified SEU cross section in units of area per bit:* $\sigma\{\text{SEU}\}/\text{bit} = (3.3 \pm 0.6) \times 10^{-13}$ cm^2. Graphical examples of SEU and SEFI are shown in Fig. 10 [Figure 10: see original paper].

V. Conclusion

In this paper, an evaluation system for ADS5272 has been established and its radiation performance has been characterized. From the irradiation test results, the ADS5272 performs very well up to 3 kGy (Si) TID and up to 5×10^{12} p/cm^2 fluence without significant performance degradation. These characteristics meet the radiation tolerance criteria of the COTS component for the LAr calorimeter front end (FE) electronics [**?**]. Therefore, the ADS5272 has been identified as a good candidate for use in the future LAr calorimeter electronics upgrade, and a demonstrator LTDB is now being designed with this ADC. Valuable experience and information will be obtained from this demonstrator system after installing and running it at the high luminosity of $\text{L} = 10^{34}/(\text{cm}^2 \cdot \text{s})$ on the ATLAS LAr calorimeter.

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