The control and measurement of high power high-gradient acceleration structures (Postprint)

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Abstract

Conditioning an accelerating structure is important, and its performance is limited by breakdown and vacuum degradation, hence the necessity of finding problem in the conditioning. In order to save time, a judging process built in the firmware layer is applied in this paper. The system using the embedded algorithm in the Field Programmable Gate Array (FPGA) locates the position of breakdown and displays the result in the user interface. Also, the system has the functions of automatic conditioning and interlock protection, which are useful during the conditioning process of an S-band accelerating structure.

Full Text

Abstract

Conditioning an accelerating structure is crucial, yet its performance is limited by breakdown events and vacuum degradation, making it essential to identify problems during conditioning. To save time, this paper implements a judging process built into the firmware layer. The system employs an embedded algorithm in a Field Programmable Gate Array (FPGA) to locate the position of breakdown and displays the results in the user interface. Additionally, the system features automatic conditioning and interlock protection functions, which prove useful during the conditioning process of an S-band accelerating structure.

Keywords: Conditioning, Location of breakdown, Automation and Interlock protection, FPGA

Introduction

High-gradient, high-repetition-rate acceleration structures and their control and measurement during high-power tests are vital for developing compact linacs

[1–3]. The RF systems of linac-testing facilities at CLIC, Spring-8, SNS, and others benefit from automatic control. These controllers are typically implemented in hardware for signal acquisition, with data analysis performed using self-developed software in C, C++, JAVA, or other programming languages [4]. However, real-time breakdown location remains challenging. This paper aims to implement collected data waveform processing in Field Programmable Gate Arrays (FPGA) to identify specific breakdown locations in real time. This approach saves time in diagnosing hardware malfunctions in a linac, allowing the conditioning process to be terminated quickly while enhancing safety and accuracy in conditioning high-gradient accelerating structures.

II. Hardware

The PCI eXtensions for Instrumentation (PXI) bus framework, including the ICS-572B board and the RF front-end with LLRF (low-level radio frequency), is illustrated in Fig. 1 [Figure 1: see original paper] [5–7]. This virtual instrument platform, released by National Instruments (NI) in 1997, is well-suited for testing acceleration structures [8].

The ICS-572B board is equipped with two ADCs (AD6645) with sampling frequencies up to 105 MHz, enabling simultaneous sampling of the input and reflected signals from the acceleration structure. It incorporates a high-performance Xilinx Virtex-II FPGA with up to six million logic gates, fully meeting the design requirements. The board also includes a PCI bus interface compliant with PCI2.2 specifications at 66 MHz/64-bit speed, facilitating data communication between the underlying hardware and upper-level software. According to project requirements, two PXI-5122 data acquisition boards with 100 MHz sampling rate have been added.

As shown in Fig. 2 [Figure 2: see original paper], the test platform for high-power S-band accelerating structures consists primarily of a 45 MW klystron and a SLAC accelerating structure [9, 10]. On the ICS-572B, the DAC output signal is 25.6 MHz. The frequency of the downstream RF front-end is 2997.924 MHz, which serves as the amplifier input. The maximum output power of the solid-state amplifier that provides the input signal to the klystron is approximately 1000 W. The output and reflected signals of the klystron, along with the input and output signals of the accelerating structure and the ICT signal, are displayed and stored by the ICS-572B and PXI-5122 boards [11]. The experimental platform' s user interface is built in LABVIEW, allowing experimental parameters to be set and waveforms to be displayed. When reflected power increases suddenly and exceeds the threshold, the DAC module output is reduced to zero to protect the klystron from damage. This protection function is also integrated into the user interface. Additionally, the system can automatically record the reflected signal waveform when breakdown occurs.

III. Software

The software comprises three core modules: automatic conditioning, interlock protection, and breakdown location. As shown in Fig. 3 [Figure 3: see original paper], the I and Q values of the input and reflected signals can be obtained after down-conversion [12], AD sampling, and FIR filtering. Their amplitude is then calculated using the CORDIC algorithm [13, 14].

The interlock protection module detects the power of reflected signal and the vacuum in real time. When the number of breakdowns in the accelerating structure exceeds the threshold and vacuum degradation occurs, the DAC input power is immediately cut off to protect the system from damage. Figure 4 [Figure 4: see original paper] illustrates the algorithm execution procedure [16].

A. The Automatic Conditioning Module

The input amplitude of the accelerating structure can be adjusted automatically based on the number of breakdowns within a specified time period, while the maximum and minimum signal amplitudes can be manually input through the user interface [15]. Within the specified time period, if the breakdown count remains below threshold, the input amplitude is increased; otherwise, it is decreased. The variation is constrained to the maximum and minimum values set by the system.

C. The Location of Breakdown Module

The algorithm locates breakdown position based on the time difference between the falling edges of the incident and reflected signals [17]. When a breakdown occurs, subsequent RF signals cannot propagate effectively through the acceleration structure. The system identifies the falling edges of the incident and reflected signals within the FPGA [18] and calculates the time difference (t) using a counter.

IV. Experiment on Conditioning S-Band Acceleration Structure

The S-band acceleration structure was tested on the platform. In operation, the accelerating gradient is designed to reach 18 MV/m at approximately 10 Hz repetition rate. Before the experiment, the klystron was provided with a 340 W, 3 µs wide RF excitation signal according to design requirements, and the modulator voltage was increased to 5 kV. The klystron output pulse width was set to 0.5 µs by adjusting the solid-state amplifier output. The voltage was increased by 0.5 kV every 10 minutes. The vacuum interlock point was set to 1×10^{-5} Pa and the recovery point to 5×10^{-6} Pa. The output and reflected signals of the klystron, together with the input and output signals of the accelerating structure, were detected by the ICS-572B and PXI-5122 boards.

If power was conditioned to 20 MW, the modulator output should be decreased to zero. In the experiment, power could be conditioned to 20 MW at RF pulse widths of 0.5, 1.0, 1.5, and 3.0 μs. Figure 6 [Figure 6: see original paper] shows the breakdown location distribution for these cases.

Due to limited hardware conditions, the system precision is about four cell lengths, because the sampling frequency (105 MHz) of the ICS-572B board is insufficient to locate breakdown positions to a single cell. While attenuation of the reflected signal along the structure may introduce bias in the analysis, in most cases breakdown occurrence can be confirmed when the reflected signal amplitude exceeds the threshold value despite this attenuation.

The breakdown rates were monitored at output powers of 20, 30, and 36 MW. The resulting data are presented in Table 1 .

The group velocity equation for the S-band accelerating structure is given by Eq. (1):

$$v_g = (\omega/Q)\frac{l-(1-e^{-2\tau})z}{1-e^{-2\tau}}$$

where l and Q are the total length and quality factor of the acceleration tube, respectively; ω is the frequency; z is the displacement distance from the origin; and τ is the attenuation constant. Letting A = ωl/[Q(1 - e^{-2τ})] and B = ω/Q, Eq. (1) can be transformed into Eq. (2):

$$z = At/(2+Bt)$$

During conditioning of an S-band acceleration structure, with known values of z and Q, the group velocity can be easily calculated. Using Eq. (2), a lookup table can be created to establish the relationship between the microwave arrival time at each cell and the distance z. The actual breakdown position in the accelerating structure can then be located by referencing this lookup table with the known time value (t). Figure 5 [Figure 5: see original paper] shows the principle diagram for breakdown location.

The breakdown rate is higher at an output power of 36 MW. According to the breakdown distribution in Fig. 7 [Figure 7: see original paper], most breakdowns occurred in cells numbered 80–90. Upon inspection of those cells, cell 89 was found to be damaged.

V. Conclusion

The testing platform achieves detection of breakdown position through a real-time, fast, and accurate Field Programmable Gate Array (FPGA) implementation. The system not only locates breakdown positions but also displays results in real time. When breakdowns occur continuously at the same position,

problems can be easily identified and analyzed immediately, helping to protect accelerating structures from damage.

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Note: Figure translations are in progress. See original paper for figures.