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Magnetic flux leakage analysis and compensation of high-frequency planar insulated core transformer (Postprint)

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Abstract

A novel high-frequency and high power density planar insulated core transformer (PICT) applied to high voltage direct current (DC) generator is introduced. PICT' s operating principle and fundamental configuration are described, and preliminary experimental results in self-designed PICT apparatus are presented. Emphatically, magnetic leakage flux (MFL) giving rise to the output voltage drop is analyzed in detail both theoretically and by finite element method (FEM). Showing good consistency with experimental result, FEM simulation is considered to be practicable in physical design of PICT. To cancel out leakage inductance and improve the voltage uniformity, compensation capacitor is adopted and experimental verification is also presented. All shows satisfactory results.

Full Text

Preamble

Magnetic Flux Leakage Analysis and Compensation of High-Frequency Planar Insulated Core Transformer

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Abstract

This paper introduces a novel high-frequency, high power-density planar insulated core transformer (PICT) for high-voltage DC generator applications. The operating principle and fundamental configuration of the PICT are described, along with preliminary experimental results from a self-designed prototype. The analysis focuses particularly on magnetic leakage flux (MFL) as a critical factor causing output voltage drop, examining this phenomenon through both theoretical modeling and finite element method (FEM) simulations. The FEM results show good consistency with experimental measurements, demonstrating its practicality for PICT physical design. To cancel leakage inductance and improve voltage uniformity, compensation capacitors are implemented and experimentally verified, yielding satisfactory performance.

Keywords: Planar insulated core transformer, Load operation, Magnetic flux leakage, Leakage inductance, Finite element analysis, Flux compensation

Introduction

The planar insulated core transformer (PICT) represents a novel high-voltage, high-power DC generator that combines the characteristics of insulated core transformers (ICT) [1–3] and planar transformers [4,5]. Compared to conventional line-frequency transformers [6,7], the PICT offers significant advantages including compact structure, low stored energy, excellent transient response, high efficiency, good fault tolerance, and high reliability, making it promising for DC power supplies below 1 MV.

Driven by a switching power supply, the PICT typically employs ferrite magnetic cores. Secondary windings are configured as conductive tracks on printed circuit boards (PCB), with multiple PCB stacks connected in series to generate DC output voltages exceeding 100 kV and currents of 50–200 mA.

Figure 1 Figure 1: see original paper schematically illustrates our experimental PICT prototype. Energized by a 33 kHz AC signal from a pulse-width-modulated inverter, the transformer features 5 turns in the primary winding and comprises 27 PCB stacks. Each PCB circuit contains 32 identical secondary modules, with each module consisting of 2 turns of secondary coil and a full-wave bridge rectifier (Fig. 1(b)).

Assuming ideal conditions with no losses, when excited by a signal of amplitude UP, the output DC voltage UDC is given by UDC = 2 UP = 2 32 × 27n2, where N1 and N2 represent the number of turns in primary and secondary windings respectively, and n2 denotes the number of turns per secondary module. The PICT, sized at just Φ500 mm × 600 mm, operates at UP = 520 V in an SF6-filled tank. According to this relationship, it should deliver a DC output exceeding 300 kV. However, open-loop experiments yielded UP = 400 V and UDC = 220 kV under no-load conditions; under loaded conditions with an output current of 15 mA, measurements showed UP = 200 V and UDC = 100 kV, limited by

the front-end power supply capacity.

II. Theoretical Analysis of Magnetic Flux Leakage in PICT

The measured DC output exhibited a severe drop compared to theoretical predictions, with magnetic leakage flux (MFL) identified as the primary cause. To isolate adjacent ferrite tiles from neighboring magnetic core sections, insulating films with low magnetic permeability μ were inserted between PCB stacks, creating gaps in the magnetic circuit. MFL manifests as "by-pass" flux at these gap fringes, resulting in reduced flux through the upper sections of the magnetic core. Figure 2 [Figure 2: see original paper] schematically illustrates the insulating film configuration and by-pass flux phenomenon.

The 27 PCB stacks are numbered m1, m2, $\cdots$, mN, $\cdots$, m27 from bottom to top. The 28 magnetic gaps introduced by 27 isolation layers produce flux leakage $\Delta\Phi$, which is proportional to the main flux Φ at each position [8,9], i.e., $\Delta\Phi \quad \Phi$. This leakage reduces the magnetic coupling efficiency KN to less than unity in the Nth PCB. Consequently, the output voltage UN = U0KN ($0 <$ KN < 1, $0 <$ N < 28) decreases along the vertical axis, where KN depends primarily on gap width—specifically, the thickness of insulating films. Thus, MFL causes voltage loss by reducing KN in upper stages.

The leakage inductance resulting from MFL is represented in the equivalent circuit shown in Fig. 3 [Figure 3: see original paper], where T = 5:2 represents the coupling inductance ratio; subscripts L, P, and S denote load resistance, primary coil, and secondary coil respectively; Lkp and Lks represent leakage inductance; and CP and CS represent stray capacitance. Under no-load conditions, the RL branch presents high impedance, allowing Lkp and Lks to form a series resonant circuit with CS that does not reduce voltage across RL. When load current reaches the mA level, this electrical resonance disappears, causing voltage division between leakage inductance and RL, thereby reducing output voltage.

MFL represents a critical performance-limiting factor in PICTs, causing not only voltage drop but also degradation of voltage uniformity across PCB stacks. Determining KN values and developing compensation strategies is therefore essential. Our earlier studies [10,11] using preliminary no-load tests on a primitive 5-PCB PICT showed different characteristics from actual loaded operation. To investigate MFL behavior under realistic load conditions, we conducted finite element simulations and experimental validation.

III. Magnetic Field Analysis Using CST

While magnetic field energy analysis in transformer windings [12,13] can theoretically calculate leakage flux, this approach is suitable only for qualitative analysis. Finite element analysis provides superior capability for numerical evaluation. Using CST FEM Studio, we performed magnetic field simulation of the PICT with the following parameters: primary winding with 5 turns, excitation current of 50 A, magnetic core cross-section of 0.01 m^2, relative permeability μr = 2400, gap width of 0.15 mm, mesh count of 6×10^5, and computational accuracy of 10^{-6}.

CST simulation yields magnetic flux density B throughout the model space, with results shown in Fig. 4 [Figure 4: see original paper]. The by-pass flux constitutes the primary source of leakage flux. By integrating B across the 27 PCB sections to obtain magnetic flux Φ, we derived flux data for PCB stacks with 0.15 mm gaps, as presented in Fig. 5 [Figure 5: see original paper]. The Φ distribution approximates an exponential decay, with $\Phi_1 = 7.791 \times 10^{-4}$ Wb at the bottom plane and $\Phi_{27} = 6.672 \times 10^{-4}$ Wb at the top plane. With simulated B = 800 Gs, the theoretical Φ should be 8.0×10^{-4} Wb, yielding $K_1 = 0.974$ and $K_{27} = 0.834$. Figure 5 also shows simulation results for 0.1 mm and 0.3 mm gap widths: at 0.1 mm, $K_1 = 0.980$ and $K_{27} = 0.887$; at 0.3 mm, $K_1 = 0.944$ and $K_{27} = 0.740$. These results confirm that gap width is the most significant factor affecting leakage flux, and that thinner insulating films effectively reduce MFL.

IV. Experimental Phenomenon

We performed no-load and loaded tests to measure DC output voltage across all PCB stacks. In each PCB, input terminals were grounded while output ports were connected to load resistance RL. The insulating film thickness was 0.15 mm. For loaded tests, RL = 120 kΩ with 7 mA load current; for no-load tests, RL = 1000 MΩ.

Figure 6 Figure 6: see original paper presents the measured voltage distribution. Under load, bottom PCB output was 824 V while top PCB output was 704 V, representing a 14.6% drop. In contrast, no-load outputs were nearly uniform. The significant difference between these curves confirms theoretical predictions. Repeated tests showed voltage drops between bottom and top PCBs ranging from 13% to 17%, demonstrating good agreement with CST simulation results. Figure 6(b) compares experimental data with CST simulation.

In conclusion, MFL during loaded PICT operation causes progressively lower voltage generation in upper PCB stacks, reducing overall voltage efficiency. Accurate CST magnetic field calculations provide a numerical foundation for PICT design optimization.

V. Compensation of Flux Leakage

After quantifying leakage flux and its manifestation as leakage inductance in the equivalent circuit, we implemented compensation measures. The method of adding secondary windings proposed in Ref. [3] is unsuitable for PICTs. A more practical approach involves connecting appropriate compensation capacitors across secondary coils [10,11,14–16].

We calculated and optimized compensation capacitor values using Multisim. To equalize DC voltage across PCB stacks with varying KN, our PICT required 33 nF capacitors. Notably, the required capacitance values were nearly identical across different PCB stacks.

To evaluate compensation performance, Multisim simulations were conducted on three individual secondary modules with different KN values. The simulation circuit matched that shown in Fig. 2, with coupling inductances T1, T2, and T3 representing efficiencies of 0.8 (top PCB), 0.9 (intermediate PCB), and 0.98 (bottom PCB) respectively. Compensation capacitors of 33 nF were connected across secondary coils. Figure 7 [Figure 7: see original paper] shows output voltages before and after compensation: the red, green, and blue lines represent T1, T2, and T3 outputs respectively. Before compensation, the three outputs differed significantly; after compensation, they became nearly identical and achieved higher voltage values.

To verify the simulation, 2.2 nF and 33 nF capacitors were installed on the topmost PCB and DC voltages were measured. Table 1 presents the results. The 33 nF capacitor achieved uniform voltage distribution across PCB stacks, while other values did not. These results demonstrate that proper selection of compensation capacitance effectively mitigates magnetic leakage in PICTs.

VI. Conclusion

This study investigates MFL in PICTs and confirms it as a significant factor causing voltage drop. CST simulation is introduced for quantitative MFL analysis, and comparison with experimental results validates its accuracy. Compensation capacitors are successfully employed to minimize leakage inductance under load, with experimental verification achieving the desired performance. This research provides both scientific insight and practical significance for developing new high-power DC sources.

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