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Abstract

Single event effects (SEEs) induced by radiations become a significant reliability challenge for modern electronic systems. To evaluate SEEs susceptibility for microelectronic devices and integrated circuits (ICs), an SEE testing system with flexibility and robustness was developed at Heavy Ion Research Facility in Lanzhou (HIRFL). The system is compatible with various types of microelectronic devices and ICs, and supports plenty of complex and high-speed test schemes and plans for the irradiated devices under test (DUTs). Thanks to the combination of meticulous circuit design and the hardened logic design, the system has additional performances to avoid an overheated situation and irradiations by stray radiations. The system has been tested and verified by experiments for irradiating devices at HIRFL.

Full Text

A Flexible and Robust Soft-Error Testing System for Microelectronic Devices and Integrated Circuits

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Abstract: Radiation-induced single event effects (SEEs) pose a significant reliability challenge for modern electronic systems. To evaluate SEE susceptibility in microelectronic devices and integrated circuits (ICs), a flexible and robust SEE testing system was developed at the Heavy Ion Research Facility in Lanzhou (HIRFL). The system is compatible with various types of microelectronic devices and ICs, and supports numerous complex, high-speed test schemes for irradiated devices under test (DUTs). Through meticulous circuit design and hardened logic implementation, the system provides additional capabilities to prevent overheating and mitigate irradiation from stray radiation. The system has been experimentally tested and verified for device irradiation at HIRFL.

Keywords: SEE testing, Testing system, Single Event Effects, Soft errors, HIRFL
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INTRODUCTION

Radiation-induced single event effects (SEEs) are considered a primary challenge to the reliability of microelectronic devices and integrated circuits (ICs) [1, 2], as highly energetic particles traversing sensitive regions of devices under test (DUTs) induce charge collection [1, 3–5]. To indirectly assess SEE sensitivity in DUTs—particularly non-destructive effects including single event upset (SEU), single event transient (SET), single event functional interrupt (SEFI), and single event latch-up (SEL) [1, 6]—ground tests on accelerators are generally performed as a critical approach for exposing DUTs to radiation environments [5, 7]. Consequently, an effective and accurate testing system is an indispensable tool for characterizing SEEs.

This paper presents the design and construction of a robust, flexible system developed primarily for soft-error testing at the Heavy Ion Research Facility in Lanzhou (HIRFL). The primary design objective is to support multiple I/O standards for physical compatibility with diverse digital devices, such as static random access memories (SRAMs), dynamic random access memories (DRAMs), flash memories, and field programmable gate arrays (FPGAs). As a testing system composed of programmable logic devices combined with extensible control software, it can logically support extensive SEE experiments while enabling smooth management.

Additionally, the system provides high access speeds (up to 200 Msps) and real-time monitoring for DUTs, enabling effective detection and recording of soft errors during experiments at HIRFL. Using this testing system, SEE characterization experiments have been successfully performed on various devices. Notably, one type of FPGA intended for satellite applications and its reinforced logic design have been tested and verified.

II. DESIGN OF THE TESTING SYSTEM

Based on established guidelines and standards for SEE testing procedures [1, 5–11] and prior SEE testing system designs [12–23], a block diagram of the soft-error testing system was developed (Fig. 1 [Figure 1: see original paper]). The system is divided into two main parts. The primary component consists of a circuital subsystem, programmable power supplies, an RS485-to-USB adapter, and a control computer, all located in the irradiation laboratory where DUTs are exposed. The secondary component is a monitoring computer in the operators' room, connected to the control computer via remote desktop protocol, which controls the testing system. These two parts are separated by bioshielding to protect personnel from radiation.

The circuital subsystem is architected to detect soft errors in DUTs using a motherboard-daughterboard structure. Daughterboards are designed to mount DUTs, while the motherboard implements required functions. This structure offers cost reduction through motherboard reuse and facilitates experiments in vacuum chambers due to the circuital subsystem' s robustness.

To mitigate unexpected effects from stray radiation, the remaining testing system equipment in the irradiation laboratory is positioned away from the circuital subsystem, connected via long cables that inevitably introduce some signal degradation. To supply appropriate voltages to the circuital subsystem, a closed control loop for power networks is implemented. This loop involves the circuital subsystem, programmable power supplies, control computer, and software. The workflow proceeds as follows: (1) programmable power supplies provide required voltage to the circuital subsystem; (2) the circuital subsystem feeds actual voltage values back to the control computer; and (3) the control computer instructs the programmable power supplies to modulate their output voltage.

Furthermore, to ensure reliable data transfer over long cables between the circuital subsystem and control computer, a derived industrial RS-485 communication standard is employed, utilizing checking techniques at both the byte and frame layers.

A. Design of the Circuital Subsystem

The structure of the circuital subsystem is illustrated in Fig. 2 [Figure 2: see original paper]. Daughterboards carrying DUTs are discrete from the motherboard. When characterizing a specific device or IC type, the corresponding daughterboard attaches to the motherboard. The motherboard provides operating conditions for DUTs and detects soft errors occurring during irradiation. Functionally, the motherboard can be grouped into three modules: the interface module, monitoring module, and testing module.

1. The Interface Module The interface module imports power sources and communicates with the control computer through four DB-9 connectors. Two

connectors import power sources, with each serving two channels (Fig. 2). One channel supplies the motherboard, while the other three channels supply DUTs. The remaining two DB-9 connectors communicate with the control computer, transferring commands from the control computer and sending status information and test results back. Four pairs of communication channels implement a variation of the RS-485 standard at the physical and electrical layers. Three pairs are duplex, while the fourth is a bidirectional, configurable channel. This configuration enables various modes for different applications. For example, combining one duplex pair with one pair configured as input (relative to the circuital subsystem) can form a joint test action group (JTAG) channel, facilitating dynamic configuration/reconfiguration of the FPGA (the core of the testing module) or accessing DUTs that support JTAG interface (e.g., programmable logic devices, memory ICs, and application-specific ICs).

2. The Monitoring Module The monitoring module ensures proper operation of the circuital subsystem, centered on the motherboard monitoring and control unit (MMCU)—a circuit based on a complex programmable logic device (CPLD). The CPLD logic design is shown in Fig. 3 [Figure 3: see original paper]. The MMCU is powered directly by a low dropout regulator (LDO) and operates continuously throughout SEE testing. During testing, it samples temperatures from six thermal sensors distributed across the motherboard twice per second. If any sampled temperature exceeds a predetermined threshold, the MMCU drives the motherboard into a low-power mode, such as decreasing the testing module's operating speed (or even pausing) or turning off all other motherboard parts, depending on the temperature rise rate. Once temperatures drop below acceptable values, the monitoring and control unit continues or restarts the test cycle.

The monitoring module also manages power supplies for the testing module by switching and monitoring their status. When a test cycle begins, the MMCU activates the relay and simultaneously monitors its output. Sampled voltage values feed back into the closed control loop of the power networks described above, compensating the motherboard power supply into a suitable range without IR-drop effects from long power cables. Subsequently, four DC-DC power modules are enabled. These modules feature high integration, performance, and conversion efficiency, helping mitigate thermal emission. Following the DC-DC power modules, four overcurrent detectors are installed. If SELs occur in the testing module due to stray radiation, the overcurrent detectors trigger and disable the associated DC-DC power modules to protect the motherboard.

3. The Testing Module The testing module detects soft errors in DUTs, centered on the testing control unit (TCU)—a circuit based on an FPGA. The FPGA logic design is shown in Fig. 4 [Figure 4: see original paper]. Since each test plan for DUTs requires a specific configuration file, the FPGA must be reconfigured when the test plan changes. To simplify this process, two FPGA configuration modes are implemented: local mode and online mode. Local mode

uses a flash memory capable of storing up to four configuration file revisions, selectable either manually or under MMCU control. Online mode is implemented in two ways: (1) introducing a JTAG channel from the communication interface to the configuration management circuit, where the JTAG chain interface cascades the FPGA; and (2) downloading configuration files from the computer into the FPGA via JTAG interface using the MMCU.

Once an experiment begins, the testing module provides operating conditions for DUTs. Up to three channels of adjustable power supplies can be imported to the daughterboard, sufficient for most DUT types in both normal and bias modes. The power supply control and compensation mechanism is identical to that described in the monitoring module. Power source currents are measured to detect whether SELs occur in DUTs.

For DUT data access, the testing module provides up to 120 channels of single-ended signals and 40 pairs of differential signals through two high-speed, high-density board-to-board connectors. Each connector has 180 pins, with 60 single-ended channels and 20 differential pairs assigned. Signals are alternately isolated with ground to decrease crosstalk. Moreover, signal traces on the printed circuit board (PCB) are spaced at least five times the trace width apart, further reducing interference. Traces are wired to connectors in equal length to ensure timing alignment, resulting in connection throughput of no less than 200 Mbps. Since the TCU supports various I/O standards at four voltage levels (1.2, 1.8, 2.5, and 3.3 V), most DUTs can be accessed directly. DUT temperatures are monitored by sampling sensors inside the DUTs or assembled nearby. Combined with appropriate heating methods, temperature-biased experiments can be performed, which also helps protect DUTs from overheating during normal testing.

The testing module performs soft-error detection when DUTs are ready. It initializes DUTs differently depending on DUT type or test plan, then detects soft errors by accessing DUTs and monitoring their currents. Once a soft error is detected, the TCU packs associated information and a timestamp into a frame, which is pushed into a first-in-first-out (FIFO) queue for automatic transmission to the computer. For complex test plans, SRAM and double data rate (DDR) synchronous dynamic random access memory (SDRAM) can serve multiple purposes, such as storing initial testing data, acting as mirrors of memory ICs, and caching detected error information. Additionally, a JTAG signal path from the control computer to DUTs can be introduced for specific test plans, with both MMCU and TCU passing JTAG signals directly to DUTs.

4. The Daughterboards Daughterboards are dedicated to carrying DUTs. Benefiting from the number and throughput of connections between daughterboard and TCU, DUTs can be assembled variously. Multiple DUTs of the same type can be placed on one daughterboard to save preparation or changeover time. Multiple DUTs of different types can also be placed on one daughterboard for comparative testing.

5. Layout of the Circuital Subsystem The PCB layout of the circuital subsystem is carefully designed. In the area where DUTs are exposed to radiation, no devices are placed on the motherboard. All active devices and ICs on the motherboard are placed on the back side. The 2.5-mm-thick PCB board effectively blocks stray heavy ions from the accelerator from reaching active devices and ICs on the motherboard. This design also facilitates motherboard cooling, as nearly all active devices and ICs can be attached to a metal heat sink.

B. Design of the Control Software

Control software manages the testing system and test procedures. While the testing system is compatible with various DUT types, different DUTs have different parameters: power supply voltages, temperature ranges, access modes, and supported test plans. Consequently, initialization and SEE testing methods vary, and data processing methods for soft errors differ across test plans. To create general software for different DUTs, systematic approaches were adopted. DUT parameters and supported test plans are abstracted and stored in databases and profiles, with associated configuration files packed into folders. Data processing subprograms are compiled as dynamic link libraries (DLLs). A simple flow chart of the software is shown in Fig. 5 [Figure 5: see original paper].

III. APPLICATIONS IN EXPERIMENTS

A series of hardness assurance tests for space applications were performed using this testing system. Several SRAMs fabricated in different processes were tested, irradiated with heavy ion beams of ^{129}Xe, ^{12}C, or ^{209}Bi [24]. Bit-flipping events and real-time DUT current variations were detected and logged, each with a timestamp. A synchronous 40-bit counter generated 10 ns timestamps over a long range exceeding three hours, enabling calculation of SEE rates and supporting additional deep analyses.

Figure 6 [Figure 6: see original paper] shows a portion of raw items logging bit-flipping events, where timestamps help distinguish possible multiple cell upsets (MCUs). With a DUT access interval of 50 ns, the first three items occur in the same polling cycle. The addresses of the second and third items differ by only one bit from the first item, suggesting that bit flips in two or three of these items may be caused by an MCU. Whether this represents a true MCU event depends on the DUT die layout and additional analysis.

Based on experimental data from ISSI SRAMs using this testing system, interesting phenomena were observed [25]. Results show that error correcting code (ECC) utilizing Hamming code dramatically improves device radiation tolerance, though accumulated bit-flips can render ECC ineffective.

Temperature dependence of SEU in commercial bulk and SOI (silicon on insulator) SRAMs was investigated using this system [26]. Results demonstrate that SEU cross-section is affected by temperature, particularly around the linear energy transfer threshold for SEU occurrence [26].

Specifically, a flash-based FPGA proposed for satellite application was assessed, and its internal logic design verified. The FPGA' s primary inherent blocks —programmable logic elements and embedded RAMs—were tested separately. Programmable logic elements were configured as shifting register chains and inverter chains before exposure, with outputs continuously read at 200 million times per second. Figure 7 [Figure 7: see original paper] shows the raw item data format logging bit-flipping events in the shifting register chains. The test method for embedded RAMs is similar to that for normal RAM ICs. During FPGA testing, no SEL events were observed even when linear energy transfer (LET) exceeded 90 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$, substantially higher than the specified threshold for space applications.

Based on preliminary assessments of the FPGA' s radiation sensitivity, the internal logic designs were hardened through several methods, including modular redundant design and ECC. The FPGA with final logic design was then exposed to heavy ion irradiation, and acquired data were analyzed to verify the logic design' s suitability for satellite application.

Recently, two FPGA types—an advanced flash-based FPGA and an SRAM-based FPGA—were preliminarily tested as candidates for space applications. Experiments showed they were immune to SEL at least at LET of 37.6 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$, with the advanced flash-based FPGA' s soft error rate approximately 10^{-8} $\mathrm{cm}^2/\mathrm{bit}$ at LET of 20-40 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$. These results agree with manufacturer reports, though additional detailed experiments are required.

IV. CONCLUSION

The foregoing experiments demonstrate that the testing system is robust and flexible. The system can protect itself from inefficient heat sinking and tolerate stray radiation. Additionally, sufficient hardware resources make it flexible enough to be compatible with multiple DUTs. The logic design and software design for the testing system are modular, making it easy to migrate to new testing tasks simply by adding or replacing several modules. This accelerates the design process for new and more complicated DUTs and saves time in preparing testing experiments. Furthermore, evaluations and verifications of hardened algorithms and logic designs can be performed using this testing system.

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